ECE 697J – Advanced Topics in Computer Networks

The Intel Internet Exchange Architecture

10/30/03
Overview

• We have looked at
  – Network processor concepts
  – Different NP architectures
  – Commercial examples

• Next few weeks
  – In-depth look at one particular architecture
  – Intel Internet Exchange Architecture
  – Intel IXP1200 network processors

• Looking at details of platform will bring up some issues that we have ignored so far

• Good opportunity to discuss some software concepts
Intel IXA

- Intel Internet eXchange Architecture (IXA)
  - Intel’s offering of network processors
  - Combination of NP hardware and software environment

- IXA Hardware:
  - Intel offers several network processors
  - We’ll discuss IXP1200 (Internet eXchange Processor)
  - IXP1200 is one of the most widely used NPs in research

- IXA Software:
  - Software Development Environment (SDK 2.0) for packet processors and control processor
  - Allows detailed simulation without hardware
  - Controls hardware

- We’ll start with hardware
Intel IXP NPs

- Intel offers variety of network processors
- IXP1200
  - OC-3 to OC-12
  - Diverse applications, one of the first NPs
- IXP420, IXP421, IXP422, IXP425
  - Low-end, access points, home office
  - VPN, VoIP, firewall, wireless
- IXP2400
  - OC-12 to OC-48
  - Network access and edge
- IXP2800
  - OC-48 to OC-192
  - Network edge and core
- IXP2850
  - Added encryption coprocessors
  - VPNs, SANs
IXP1200
IXP1200 Features

• Single chip with
  – One embedded RISC processor
  – Six programmable packet processors
  – Multiple, independent onboard buses
  – Processor synchronization mechanisms
  – Small amount of onboard memory
  – One low-speed serial line interface
  – Multiple interfaces for external memories
  – Multiple interfaces for external I/O buses
  – A coprocessor for hash computation
  – Other functional units
System Architecture

- Two memory buses
- One PCI bus
- One IX bus for network interfaces
- Serial line interface
- SRAM bus also for FlashROM
IXP1200 Bus Speeds

• Bandwidth for buses:

<table>
<thead>
<tr>
<th>Type</th>
<th>Bus Width</th>
<th>Clock Rate</th>
<th>Data Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>Serial line</td>
<td>(NA)</td>
<td>(NA)</td>
<td>38.4 Kbps</td>
</tr>
<tr>
<td>PCI bus</td>
<td>32 bits</td>
<td>33-66 MHz</td>
<td>2.2 Gbps</td>
</tr>
<tr>
<td>IX bus</td>
<td>64 bits</td>
<td>66-104 MHz</td>
<td>4.4 Gbps</td>
</tr>
<tr>
<td>SDRAM bus</td>
<td>64 bits</td>
<td>≤ 232 MHz</td>
<td>928.0 MBps†</td>
</tr>
<tr>
<td>SRAM bus</td>
<td>16 or 32 bits</td>
<td>≤ 232 MHz</td>
<td>464.0 MBps</td>
</tr>
</tbody>
</table>

• IX bus provides more bandwidth than PCI (as expected)
  – Connection to network interfaces
  – Connection to other IXPs for multi-chip architectures

• SDRAM provides more bandwidth than SRAM
## Internal IXP1200 Components

<table>
<thead>
<tr>
<th>Quantity</th>
<th>Component</th>
<th>Purpose</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Embedded RISC processor</td>
<td>Control, higher layer protocols, and exceptions</td>
</tr>
<tr>
<td>6</td>
<td>Packet processing engines</td>
<td>I/O and basic packet processing</td>
</tr>
<tr>
<td>1</td>
<td>SRAM access unit</td>
<td>Coordinate access to the external SRAM bus</td>
</tr>
<tr>
<td>1</td>
<td>SDRAM access unit</td>
<td>Coordinate access to the external SDRAM bus</td>
</tr>
<tr>
<td>1</td>
<td>IX bus access unit</td>
<td>Coordinate access to the external IX bus</td>
</tr>
<tr>
<td>1</td>
<td>PCI bus access unit</td>
<td>Coordinate access to the external PCI bus</td>
</tr>
<tr>
<td>several</td>
<td>Onboard buses</td>
<td>Internal control and data transfer</td>
</tr>
</tbody>
</table>
IXP1200 Organization

The diagram illustrates the organization of the IXP1200 chip. It includes:
- SRAM bus and SRAM access
- FLASH
- Memory Mapped I/O
- SDRAM and SDRAM bus
- Optional host connection
- PCI bus
- IX bus
- IX access
- Multiple, independent internal buses
- Embedded RISC processor (StrongARM)
- Microengines 1 to 6

The diagram also shows the connections and flow of data, emphasizing the integration of various components within the IXP1200 architecture.
IXP1200 Processor Hierarchy

- Different processors:
  - General-Purpose Processor
    - CPU of host system on which IXP resides
    - High-level functions, like routing
  - Embedded RISC Processor (StrongARM)
    - Runs conventional operating system (e.g., Linux)
    - Manages Microengines, configures system, processes exceptions
  - I/O Processors (Microengines)
    - Fast path, main packet processors

<table>
<thead>
<tr>
<th>Processor Type</th>
<th>Onboard?</th>
<th>Programmable?</th>
</tr>
</thead>
<tbody>
<tr>
<td>General-Purpose Processor</td>
<td>no</td>
<td>yes</td>
</tr>
<tr>
<td>Embedded RISC Processor</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>I/O Processors</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>Coprocessors</td>
<td>yes</td>
<td>no</td>
</tr>
<tr>
<td>Physical Interfaces</td>
<td>no</td>
<td>no</td>
</tr>
</tbody>
</table>
IXP1200 Coprocessors

- Hash Unit
  - Computes 48-bit or 64-bit hash in hardware
  - Adaptive polynomial hash function
  - Anybody have any idea why this could be useful?? 😊
- Four timers
- Real-time clock
- JTAG interface for testing
- IX bus controller
- FBI (FIFO Bus Interface) unit
### IXP1200 Memory Hierarchy

- **Different Memories:**

<table>
<thead>
<tr>
<th>Memory Type</th>
<th>Maximum Size</th>
<th>On Chip?</th>
<th>Typical Use</th>
</tr>
</thead>
<tbody>
<tr>
<td>GP Registers</td>
<td>128 regs.</td>
<td>yes</td>
<td>Intermediate computation</td>
</tr>
<tr>
<td>Inst. Cache</td>
<td>16 Kbytes</td>
<td>yes</td>
<td>Recently used instructions</td>
</tr>
<tr>
<td>Data Cache</td>
<td>8 Kbytes</td>
<td>yes</td>
<td>Recently used data</td>
</tr>
<tr>
<td>Mini Cache</td>
<td>512 bytes</td>
<td>yes</td>
<td>Data that is reused once</td>
</tr>
<tr>
<td>Write buffer</td>
<td>unspecified</td>
<td>yes</td>
<td>Write operation buffer</td>
</tr>
<tr>
<td>Scratchpad</td>
<td>4 Kbytes</td>
<td>yes</td>
<td>IPC and synchronization</td>
</tr>
<tr>
<td>Inst. Store</td>
<td>64 Kbytes</td>
<td>yes</td>
<td>Microengine instructions</td>
</tr>
<tr>
<td>FlashROM</td>
<td>8 Mbytes</td>
<td>no</td>
<td>Bootstrap</td>
</tr>
<tr>
<td>SRAM</td>
<td>8 Mbytes</td>
<td>no</td>
<td>Tables or packet headers</td>
</tr>
<tr>
<td>SDRAM</td>
<td>256 Mbytes</td>
<td>no</td>
<td>Packet storage</td>
</tr>
</tbody>
</table>
IXP1200 Memories

- Caches are transparent to programmer
- Memories that programmer focuses on:
  - SRAM, SDRAM, Scratch (Scratchpad)
- Other memory features:

<table>
<thead>
<tr>
<th>Memory Type</th>
<th>Addressable Data Unit (bytes)</th>
<th>Relative Access Time</th>
<th>Special Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>Scratch</td>
<td>4</td>
<td>12 - 14</td>
<td>synchronization via test-and-set and other bit manipulation, atomic increment</td>
</tr>
<tr>
<td>SRAM</td>
<td>4</td>
<td>16 - 20</td>
<td>stack manipulation, bit manipulation, read/write locks</td>
</tr>
<tr>
<td>SDRAM</td>
<td>8</td>
<td>32 - 40</td>
<td>direct transfer path to I/O devices</td>
</tr>
</tbody>
</table>
Synchronization

• How to implement synchronization between processors/threads?
• Example: shared packet counter
• Problem: increment requires read and write
  – Write after write (WAW) causes problems
• Solution?
  – Semaphore: atomic test and set operation
• Other problems
  – Deadlocks
Memory Addressing

• Addressable data units vary with memory type
  – Smallest addressable unit

• Typical units:
  – Word (16 bits)
  – Longword/long (32 bits)
  – Quadword (64 bits)

• Programmer needs to carefully plan memory layout
  – Address needs to be adapted to addressable units
  – Data structures that cross boundaries require multiple accesses
Complexity

- Each unit has many components
- Example: SRAM access unit
Next Class

- More details on IXP1200 will be covered
  - Embedded RISC Processor (StrongARM core) – Chapter 19
  - Packet Processing Hardware (Microengines, FBI) – Chapter 20
- Read Chapters 19 and 20