CommBench
--- A Telecommunications Benchmark For Network Processors

ECE 697J Active Networks
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Outline

- Motivation
- CommBench
- Data & Tools
- Characteristics
- Examples
- Summary
Motivation

- New requirements push network processors
- How to evaluate and select chips
- SPEC is designed for workstations/PCs
  - not focusing on defined I/O
  - not considering packet size
  - not considering performance
- CommBench
  - streaming data flow
  - packet-based processing task
CommBench

- Benchmark Applications
  - HPA (Header-Processing Applications)
    - per-packet basis
    - independent of size and type of the packet payload
    - RTR, FRAG, DRR, TCP
  - PPA (Payload-Processing Applications)
    - access/modify the content of a packet
    - typically executed on a stream of packets
    - CAST, ZIP, REED, JPEG
Data & Tools

- All benchmark programs
  - Run on SUN UltraSparc II under SunOS 5.7
  - Compiler is gcc 2.8.1 (O2)
- Tools
  - Shade and SpixTools for instruction mix
  - Dinero for cache simulation
- Data types for different applications
  - HTML data (plain text)
  - Binary program code
  - JPEG coded image data
Benchmark Characteristics

- Compare to SPEC
  - Code and kernel size
  - Computational complexity
  - Instruction frequency
  - Cache performance
Characteristics --- Code and Kernel Size

- Static code size
  - an order of magnitude smaller than SPEC

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Code Size C lines</th>
<th>Code size object bytes</th>
</tr>
</thead>
<tbody>
<tr>
<td>CommBench</td>
<td>5,750</td>
<td>97,000</td>
</tr>
<tr>
<td>SPEC</td>
<td>48,700</td>
<td>678,000</td>
</tr>
</tbody>
</table>

- Dynamic kernel
  - much smaller than SPEC

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Instr. at least once</th>
<th>Instr. for 99%</th>
<th>Instr. for 90%</th>
</tr>
</thead>
<tbody>
<tr>
<td>CommBench</td>
<td>3,430</td>
<td>500</td>
<td>275</td>
</tr>
<tr>
<td>SPEC</td>
<td>35,700</td>
<td>9,700</td>
<td>3,390</td>
</tr>
</tbody>
</table>
Characteristics --- Computational Complexity

- Computational Complexity
  - Respect to the number and size of processed packets
  - Based on the # of instructions

- Definition of $N_{\alpha,l}$
  - # of instructions per byte for application $\alpha$ on a packet of length $l$

<table>
<thead>
<tr>
<th>HPA $\alpha$</th>
<th>$N_{\alpha,64}$</th>
<th>$N_{\alpha,576}$</th>
<th>$N_{\alpha,1536}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>TCP</td>
<td>10.3</td>
<td>1.2</td>
<td>0.4</td>
</tr>
<tr>
<td>FRAG</td>
<td>7.7</td>
<td>0.9</td>
<td>0.3</td>
</tr>
<tr>
<td>DRR</td>
<td>4.1</td>
<td>0.5</td>
<td>0.2</td>
</tr>
<tr>
<td>RTR</td>
<td>2.1</td>
<td>0.2</td>
<td>0.1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>PPA $\alpha$</th>
<th>$N_{\alpha,\infty}$ (enc)</th>
<th>$N_{\alpha,\infty}$ (dec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>REED</td>
<td>603</td>
<td>1052</td>
</tr>
<tr>
<td>ZIP</td>
<td>226</td>
<td>35</td>
</tr>
<tr>
<td>CAST</td>
<td>104</td>
<td>104</td>
</tr>
<tr>
<td>JPEG</td>
<td>81</td>
<td>60</td>
</tr>
</tbody>
</table>
### Characteristics

--- Instruction Frequency

- **Instruction Frequency**
  - Almost the same as SPEC (not shown here)

<table>
<thead>
<tr>
<th>Instruction</th>
<th>HPA (%)</th>
<th>PPA (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>load</td>
<td>27</td>
<td>add/sub</td>
</tr>
<tr>
<td>cond. branch</td>
<td>18</td>
<td>load</td>
</tr>
<tr>
<td>compare</td>
<td>18</td>
<td>cond. branch</td>
</tr>
<tr>
<td>add/sub</td>
<td>13</td>
<td>shift</td>
</tr>
<tr>
<td>store</td>
<td>6</td>
<td>compare</td>
</tr>
<tr>
<td>logic</td>
<td>6</td>
<td>logic</td>
</tr>
<tr>
<td>shift</td>
<td>4</td>
<td>store</td>
</tr>
<tr>
<td>load imm.</td>
<td>2</td>
<td>load imm.</td>
</tr>
<tr>
<td>jmpl</td>
<td>1</td>
<td>save/restore</td>
</tr>
</tbody>
</table>

- For CommBench only
  - Instruction mixes are different for HPA & PPA
  - Indicate that network processors must deal with both streaming and header processing applications
Characteristics --- Cache Performance

- **Cache Performance**
  - Differences are minor (2-way, 4-way, 8-way associative caches)
  - Miss rates are different on each HPA/PPA applications
  - Miss rates decrease with increasing cache size

(a) Instruction Cache Average  
(b) Data Cache Average
Design Implications

- Computational Complexity
  - Estimate the computational power of CPU
- Instruction Set Design
  - Optimize the instruction sets
- I/O Requirements for Multi-Processor ASIC
  - Estimate the memory bandwidth
Example 1 --- Computation Complexity

- Requirements of RTR and DRR
  - Link bit rate 1.2Gb/s
  - Packet size is 576 bytes
  - So, computation requirement is
    \[ M = (N_{RTR, 576} + N_{DRR, 576}) \times R_{Lnk} \]
    \[ = (0.2+0.5) \text{ instr/byte} \times 1.2G/8 \text{ bytes/sec} \]
    \[ = 105 \text{ MIPS} \]

- Requirements of on-the-fly CAST encryption
  - Link bit rate 1.2Gb/s
  - Ignore header processing overhead
  - So, computation requirement is
    \[ M = N_{\text{CAST, } \infty} \times R_{Lnk} \]
    \[ = 104 \text{ instr./byte} \times 1.2G/8 \text{ bytes/sec} \]
    \[ = 15,600 \text{ MIPS} \]
Example 2 --- Instruction Set Design

- Optimization instruction sets
- Special non-standard instructions

<table>
<thead>
<tr>
<th>Instr. Pairs</th>
<th>Avg. occurrence</th>
<th>Max. occurrence</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADD-SUBCC</td>
<td>3.55%</td>
<td>11.6%</td>
</tr>
<tr>
<td>LD-SUBCC</td>
<td>3.03%</td>
<td>13.0%</td>
</tr>
<tr>
<td>LD-LD</td>
<td>2.36%</td>
<td>20.2%</td>
</tr>
<tr>
<td>ADD-LDUB</td>
<td>2.07%</td>
<td>4.84%</td>
</tr>
<tr>
<td>SLL-LD</td>
<td>2.05%</td>
<td>6.82%</td>
</tr>
<tr>
<td>STB-ADD</td>
<td>2.05%</td>
<td>4.65%</td>
</tr>
<tr>
<td>LD-ADD</td>
<td>1.85%</td>
<td>5.35%</td>
</tr>
<tr>
<td>ADD-Add</td>
<td>1.84%</td>
<td>5.85%</td>
</tr>
</tbody>
</table>
Example 3 --- I/O Requirements

- Multiple network processors
- Estimate the average memory bandwidth for application $\alpha$ and cache size $c$
  \[ mbw_{\alpha,c} = (I_{\text{miss rate}_{\alpha,c}} + (D_{\text{miss rate}_{\alpha,c}} \times \% \text{load}_{\alpha}) + \% \text{store}_{\alpha}) \times \text{clock} \times \text{line size} \]

- For $\alpha = \text{CAST}$ and $c = 8k$, 400MHz ASIC, the memory bandwidth is
  \[ mbw_{\text{CAST},8k} = (0.0385 + (0.0076 \times 0.1985) + 0.0722) \times 400 \times 10^6 \times 32 \text{ bit/sec} = 1.4 \text{ Gbit/sec} \]
Summary

- CommBench supports evaluation and design of telecommunications network processors
- Various characteristics
  - Code and kernel size
  - Computational complexity
  - Instruction frequency
  - Cache performance
- Defined I/O and computational complexity