Technology Trends and Developments

ECE 697J
November 7th, 2002
Parallelism is Key

- Workstation processor workloads:
  - Few complex tasks
  - Hard to parallelize (ILP)
  - Limited speedup possible

- Network processor workloads:
  - Many parallel processing tasks
  - More opportunities for parallelism (CMP, multithreading, ILP)
  - Much speedup possible

- Why?
  - Packets can be processed independently (because of IP)
  - Maybe some intra-flow dependencies
Exploiting Parallelism

- Multiple processors in parallel:

- Plus pipelining:
Architecture Implications

- Many parallel processors
- Many processors for functional pipelining
- What are the limitations?
Limitations

- Number of parallel flows
- Overhead for communication between processors
  - Interconnect that distributes packets
- Centralized components
  - Packet classifier
  - Queuing system
- Shared data structures
  - Routing tables
- Chip size
  - Cost
  - Power consumption
- Technical feasibility
Technology Trends

• Relevant technologies for network processors
  – Link speed
  – CMOS feature size (density)
  – Maximum chip size
  – Clock speed
  – Memory technologies
  – Application complexity

• Moore’s Law:
  – “Number of components on chip doubles every 18 months”
Moore’s Law 1965

The experts look ahead

Cramming more components onto integrated circuits

With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65,000 components on a single silicon chip

By Gordon E. Moore

Director, Research and Development Laboratories, Fairchild Semiconductor division of Fairchild Camera and Instrument Corp.
Humor in Moore’s Paper
Long-Term Trends

- Moore’s Law is pretty “stable”
  - Of course it’s not a “law”
- Will probably continue until end of decade
  - Semiconductor Industry Association’s roadmap
- Let’s look at individual metrics
Workstation Processor Size

The graph shows the trend of processor size in transistors over the years. The x-axis represents the year, ranging from 1975 to 2010. The y-axis represents the processor size in transistors, ranging from 10,000 to 100 mio.

Key points:
- Intel
- PowerPC
- MIPS
- Sparc
- Alpha
- Trend

The trend line indicates a consistent increase in processor size over time.
Processor Clock Rate

![Graph showing the trend of processor clock rates over time, with labels for different manufacturers like Intel, PowerPC, MIPS, Sparc, and Alpha. The graph includes a trend line indicating a consistent increase in clock rates from 1975 to 2010.](image)
Performance vs. Size

![Graph showing performance vs. size for different processors](image-url)
Link Speed

The diagram shows the historical development of communication link speeds from 1975 to 2010. The x-axis represents the year, ranging from 1975 to 2010, while the y-axis represents communication link speed in Mbps. Two lines are plotted: one for optical and one for electronic. The optical line consistently surpasses the electronic line, indicating that optical technology has led the advancement in link speed over time.
Comparison of Trends

performance in year $x = a_{t_0} \cdot e^{b(x-t_0)}$

Table 2.1: Growth Parameters of Key Technologies. The values for $a$ are normalized to the year 2000. Sizes are given in million transistors (Mtx) and million gates (Mgates) (1 gate $\approx$ 4 transistors).

<table>
<thead>
<tr>
<th>Technology</th>
<th></th>
<th>$a$</th>
<th>$b$</th>
<th>Time to double</th>
</tr>
</thead>
<tbody>
<tr>
<td>Communication</td>
<td>electronic links</td>
<td>6.8 Gbps</td>
<td>0.44</td>
<td>18 months</td>
</tr>
<tr>
<td></td>
<td>optical links</td>
<td>175 Gbps</td>
<td>0.42</td>
<td>19 months</td>
</tr>
<tr>
<td>Processor</td>
<td>SPEC performance</td>
<td>2400</td>
<td>0.44</td>
<td>18 months</td>
</tr>
<tr>
<td></td>
<td>clock</td>
<td>630 MHz</td>
<td>0.23</td>
<td>36 months</td>
</tr>
<tr>
<td></td>
<td>size</td>
<td>22 Mtx</td>
<td>0.32</td>
<td>26 months</td>
</tr>
<tr>
<td>ASIC</td>
<td>size</td>
<td>55 Mgates</td>
<td>0.63</td>
<td>8 months</td>
</tr>
</tbody>
</table>
Comparison of Trends
What about Network Processors?

• How can we use these trends for scalable designs?
Possible Architectures

- Arch 1: single CPU
- Arch 2: CMP with high-performance processors
- Arch 3: CMP with low-performance processors

What is the performance criteria?
- How much processing for each packet
- Measured in SPEC per byte of link data
Architecture Performance Trends

![Graph showing trends in processing power per byte of link data over years 2000 to 2010 for simple multiprocessor, complex multiprocessor, and single processor systems.](image_url)
Limitations

- What are the limits to these trends?
  - Bottleneck in centralized components
  - Memory gap
  - Power consumption
  - Power density
Power Density

by Fred Pollack
Summary

• Networking workloads are highly parallelizable
• NPs can leverage technology trends
  – CMP with simple RISC cores
• Challenge:
  – Design architecture that can scale to use parallelism
Next Lecture

- Network processors
  - Intel IXP1200
  - IBM PowerNP

- Change class organization
  - Shorter presentations (20-25 minutes)
  - More discussion
  - What to do to ensure people are prepared?
    - Write essay on papers
    - Write down three discussion questions