Overview

• Anti-fuse and EEPROM-based devices
• Contemporary SRAM devices
  - Wiring
  - Embedded
• New trends
  - Single-driver wiring
  - Power optimization
22V10 PAL

- Combinational logic elements (SoP)
- Sequential logic elements (D-FFs)
- Up to 10 outputs
- Up to 10 FFs
- Up to 22 inputs
Antifuse Switch

- Anti-fuses are one-time programmable.
  - Pulse eliminates dielectric
  - Only need to program once.
Anti-Fuse FPGA

- Negligible programming overhead
- Low capacitance routing (fast)
- Security
- Tolerant of firm errors
- Resistance of about 100 $\Omega$
Anti-fuse Interconnect

Interconnection Fabric

Logic Module

Anti-fuse

Horizontal Track

Vertical Track
Anti-fuse Security

° Very good for design security
  • No bitstream can be intercepted in the field (no bitstream transfer, no external configuration device)
  • Need a Scanning Electron Microscope (SEM) to try to know the antifuse states (an Actel AX2000 antifuse FPGA contains 53 million antifuses with only 2-5% programmed in an average design)

Courtesy: Burleson/Gogniat
EEPROM Programming Technology

- Control programming transistor to allow for new value (Actel ProASIC devices)
- Control gate allows for programming
  - Widely deployed technology
FLASH-Memory Switch

SEL 1  SEL 2

PRG/SEN  SWITCH

WORD LINE
Flash/EEPROM Trends

- Logic elements (LUTs and flip flops)
- Segmented routing
- Low logic to register ratio
- Future?

Altera Max II
**SRAM-based FPGA**

- SRAM bits can be programmed many times
- Each programming bit takes up five transistors
- Larger device area reduces speed versus EPROM and antifuse.

![2-Input LUT Diagram](image)
Field Programmable Gate Array

Diagram showing components of Field Programmable Gate Arrays (FPGAs), including LUTs (Look-Up Tables) and CLBs (Configurable Logic Blocks).
Design Tradeoffs

• Some logic clusters are large (>10 LUTs per cluster)
• Three important issues:
  - Logic elements per cluster
  - Cluster connectivity to interconnect – wires \(F_C\) – connection flexibility
  - Switchbox flexibility \(F_s\)
Issue 1: The Logic Cluster

Question: How many BLE should there be per cluster?
Logic Cluster Size

- Interestingly, small block cluster more efficient (Betz – CICC’99)
- Includes area needed for routing.
- Small clusters (e.g. one BLE per cluster) not “CAD friendly"
- Situation changes as VLSI feature size is reduced
Number of Inputs per Cluster

- Lots of opportunities for input sharing in large clusters (Betz – CICC’99)
- Reducing inputs reduces the size of the device and makes it faster.
- Most FPGA devices include more inputs than needed to provide for flexibility
Connection Box Flexibility

- \( F_c \) -> How many tracks does an input pin connect to?
- If logic cluster is small, \( F_c \) is large \( F_c = W \)
- If logic cluster is large, \( F_c \) can be less.
  - Approximately 0.2\( W \) or less for many current FPGAs
Switchbox Flexibility

- Switch box provides optimized interconnection area.
- Flexibility found to be not as important as $F_C$
- Connections typically made with multiplexers
Switchbox Issues

Lecture 2: Field Programmable Gate Arrays I

September 8, 2016
Switchbox Issues
Buffering

- FPGAs need to buffer to isolate large RC networks
- Architects must decide where to place buffers.
Segmentation

• Segmentation distribution: how many of each length?

• Longer length
  - Better performance? 😊
  - Reduced routability? 😞
More recent CLB (V5): Slices

Figure 5-1: Arrangement of Slices within the CLB

- More hierarchy in current devices
- Slices are complex. Multiple slices communicate with switch matrix

Source: Brad Hutchings, BYU
Virtex 5 Slice

More complex LUT (6 input)

Source: Brad Hutchings, BYU
Implementing Memory on FPGAs

- For 4-input LUTs 16 bits of information available
- Can be chained together through programmable network.
- Decoder and multiplexer an issue.
- Flexibility is a key aspect.
Coarse-grained Memory

- Special large blocks of SRAM found in FPGA array
- Allow for efficient implementation of memory – predictable performance
- Six transistor SRAM cell.
Figure 2–1. Stratix IV LAB Structure

Courtesy: Brad Hutchings
Figure 2–5. High-Level Block Diagram of the Stratix IV ALM

Combinational/Memory ALUT0

6-Input LUT

adder0

Combinational/Memory ALUT1

6-Input LUT

adder1

reg0

D Q

reg1

D Q

To general or local routing

To general or local routing

To general or local routing

To general or local routing

shared_arith_in

carry_in

reg_chain_in

labclk

dataf0

dataf1

datae0

data1

dataa

dataab

datac

dataad

datae1

dataa1

shared_arith_out

carry_out

reg_chain_out

 Courtesy: Brad Hutchings
Inside the EAB - Altera

- Embedded array highly optimized
- Address and data can be latched for fast performance.
- Scalable to even larger sizes.
Inside the ESB

- Embedded System Blocks can be configured as either memory or PLA.
- Multiple levels of hierarchy.

Figure 20. ESB in Read/Write Clock Mode  Note (1)
Growth Rate of Memory

- Approximately 2400 transistors per CLB
  - (1200 per LUT) for XC4000-like implementation (32x1 SRAM)
- Six transistors per cell for Altera SRAM (2K per EAB)

<table>
<thead>
<tr>
<th>Size</th>
<th>Altera 10K</th>
<th>Xilinx 4000E</th>
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<tbody>
<tr>
<td></td>
<td>EABs</td>
<td>trans</td>
</tr>
<tr>
<td>32x1</td>
<td>1</td>
<td>12288</td>
</tr>
<tr>
<td>32x8</td>
<td>1</td>
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</tr>
<tr>
<td>128x8</td>
<td>1</td>
<td>12288</td>
</tr>
<tr>
<td>512x8</td>
<td>2</td>
<td>24576</td>
</tr>
</tbody>
</table>

For 512x8 fine-grained requires 10X more size
Stratix V – More Recent ALM (Lewis – FPGA’13)

- Note use of full adder for each LUT
- More flip flops per LUT
- Some LUT inputs can be shared
Stratix V – More Recent ALM (Lewis – FPGA’13)

• Different LUT sizes can accommodate different functions

• Software determines appropriate mapping

• Most functions map well to four-LUTs
Stratix V – More Recent Memory (Lewis – FPGA’13)

- Increasing amounts of memory per device
- Results below that a single uniform memory block size is better (20 kb)
- Evaluation over various ratios of logic to memory

![Graph](image-url)
Stratix 10 – New Features (Lewis FPGA’16)

- Insert latched in interconnect to help delay

- Latches must be low overhead

- Limited impact on signals which do not use the latch

- Also requires computer-aided design software
Stratix 10 – New Features (Lewis FPGA’16)

- Select clocks from rows
- Relatively small number of clock choices needed
- Multiplexers allow for clock selection
- $N = 8$ or $9$ is sufficient
Stratix 10 – New Features (Lewis FPGA’16)

- Distributing the flip flops from the user design into the interconnect improves performance by 10%
- Retiming the design (moving the design flip flops around) improves performance by 53%
Summary

- Three basic types of FPGA devices
  - Antifuse
  - EEPROM
  - SRAM

- Key issues for SRAM FPGA are logic cluster, connection box, and switch box.

- Latest advances examine performance and routability.

- Newer FPGAs require large amounts of RAM.
  - Trends indicate uniform blocks
  - Experimentation over many benchmarks is key