Why Analog?

- Real-world signals are Analog.
- Signals generated by sensors are analog
- Digital signal processing of signals requires Analog-to-Digital Conversion.
- Analog signal needs to be amplified and filtered before A/D.
- Amplifiers and Filters are Analog Circuits.
- A/D is a Mixed-Signal Circuit.
Digital signals in a digital communication system behave as analog signals at certain stages of transmission, receive and processing.

**Ex 1. Lossy Cable**

**Ex 2. Disc Drive**

**Ex 3. Wireless Receiver**

**Ex 3. Optical Receiver**

Signal **Attenuation**, **Noise** and **Distortion** incurred in the propagation channel require that the received signal be **Amplified**, **Filtered** and **Equalized** using **Analog** circuits.
• **Why Integrated?**

  • Larger integration → larger complexity
  
  • Lower parasitics → Higher speed
  
  • Lower cost

  • Moore’s Law: Number of transistors doubles every 18 months:
    
    • 1960: 25 μm Gate length
    
    • Today: 90 nm and 65 nm in production
    
    • 45 nm and 32 nm are in lab. 22nm and 16nm on roadmap.

• **Why CMOS?**

  • **Digital (Main Driver)**
    
    • Low Power, Simplicity, Scaling, Low cost

  • **Analog**
    
    • Integration with digital
    
    • Improved speed over years
Chapter 1

Analog Design

Levels of Abstraction

System Level

Circuit Level

Component Level

Don't Forget Variations

What is Analog Design?
CAD TOOLS FOR CIRCUIT DESIGN

• **Two Dominant Suppliers:**
  - Cadence  80% market share ✔️
  - Mentor Graphics  20% market share

• **Simulation:**
  - System Level: Matlab, SPW
  - High-Level (Behavioral): Verilog, Verilog_A, Verilog AMS
  - Low-Level (Electrical): SPICE, SPECTRE, ADS, Proprietary Tools

• **Cadence and Mentor Graphics Include tools for**
  - Schematic Capture
  - Simulation
  - Layout
Analog Design Space

Tradeoffs

- Analog Design is a Multi-Dimensional Optimization Problem.
- Improving one parameter always results in degradation of some others.
Basic MOS Device Physics

- Understanding Device Physics is Essential to Analog Design.

- MOS device is symmetric.

\[ L_{\text{eff}} = L_{\text{drawn}} - 2L_D \]

<table>
<thead>
<tr>
<th>( L_{\text{drawn}} )</th>
<th>( T_{\text{ox}} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.25 ( \mu \text{m} )</td>
<td>5 nm</td>
</tr>
<tr>
<td>0.18 ( \mu \text{m} )</td>
<td>3.5 nm</td>
</tr>
<tr>
<td>0.13 ( \mu \text{m} )</td>
<td>2.2 nm</td>
</tr>
</tbody>
</table>
MOS is a four-terminal device.

Substrate (bulk) of an NMOS is connected to the lowest potential.

Substrate (bulk) of a PMOS is connected to the highest potential.

All p-n junctions are reverse biased.

Conduction takes place beneath gate, between source and drain.
Complementary MOS Process (CMOS):
MOS CHANNEL FORMATION

- **Cut Off**
  - $V_G \text{ GND}$

- **Depletion**
  - $V_G \text{ GND}$

- **Inversion**
  - $V_G \text{ } V_{TH} \text{ GND}$

Chapter 2
• Device turn-on is a gradual phenomenon.

• There exists several definitions for $V_{TH}$.

• One definition: when $V_G = V_{TH}$:

  density of electrons on the interfaced equals density of holes in the substrate

• $V_{TH}$ increases with increasing the substrate doping.

Adjusting $V_{TH}$ by ion implantation:

• $P^+$ layer increases $V_{TH}$
PMOS IN INVERSION STATE

- PMOS: Holes flow from Source to Drain.
- NMOS: Electrons flow from Source to Drain.
- Electrons have a higher Mobility. \( \rightarrow \) NMOS is faster than PMOS (~ 3 times).
MOS Symbols

Arrow indicates current flow from positive voltage to negative voltage polarity.
I-V CHARACTERISTICS

• Larger $V_{DS} \rightarrow$ Larger Longitudinal Field
• Larger $V_{GS} \rightarrow$ More Charge Carriers

More Current
I/V Characteristics (cont.)

\[ I_D = -W C_{ox} [V_{GS} - V_{TH} - V(x)] \nu \]

Given \( \nu = \mu E \) and \( E(x) = -\frac{dV(x)}{dx} \)

\[ I_D = W C_{ox} [V_{GS} - V_{TH} - V(x)] \mu_n \frac{dV(x)}{dx} \]

\[
\int_{x=0}^{L} I_D dx = \int_{V=0}^{V_{DS}} W C_{ox} \mu_n [V_{GS} - V_{TH} - V(x)] dV
\]

\[ I_D = \mu_n C_{ox} \frac{W}{L} [(V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2] \]
I-V CHARACTERISTICS: Triode Region

Triode Region:

\[ V_{DS} < V_{GS} - V_{TH} \]

Almost Linear

\[ I_D \approx \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) V_{DS} \]

\[
I_D = \mu_n C_{ox} \frac{W}{L} \left[ (V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2 \right]
\]

- \( \mu_n \) [cm²/V·s] Electrons Mobility
- \( W \) [µm] Device Width
- \( L \) [µm] Device Length
- \( V_{DS} \)
- \( V_{GS} \)
- \( V_{TH} \)
- \( I_D \)
- \( C_{ox} \) Oxide Capacitance
- \( \varepsilon_{si} \) Oxide Permittivity
- \( t_{ox} \) Oxide Thickness

Chapter 2

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I-V CHARACTERISTICS: Saturation Region

\[ V_{DS} = V_{GS} - V_{TH} \quad \text{(Pinch-off)} \]

\[ V_{DS} > V_{GS} - V_{TH} \]

\[ I_D = \frac{\mu_n C_{ox} W}{2} \left( V_{GS} - V_{TH} \right)^2 \]

\[ L' \approx L \]
MOS OPERATION REGIMES

Both PMOS and NMOS:

- Triode Region: \[ |V_{DS}| < |V_{GS} - V_{TH}| \]
- Pinch-Off: \[ |V_{DS}| = |V_{GS} - V_{TH}| \]
- Saturation Region: \[ |V_{DS}| > |V_{GS} - V_{TH}| \]

- In saturation, MOS behaves as a current source.
Transconductance in Saturation Region

\[ I_D = \frac{\mu_n C_{ox} W}{2L} (V_{GS} - V_{TH})^2 \]

\[ g_m = \left. \frac{\partial I_D}{\partial V_{GS}} \right|_{V_{DS} \text{ constant}} = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) \]

\[ g_m = \sqrt{2 \mu_n C_{ox} \frac{W}{L}} I_D = \frac{2I_D}{V_{GS} - V_{TH}} \]
DRAIN-SOURCE RESISTANCE IN TRIODE REGION

\[ I_D = \mu_n C_{ox} \frac{W}{L} \left( V_{GS} - V_{TH} \right) V_{DS} - \frac{1}{2} V_{DS}^2 \]

\[ I_D = \mu_n C_{ox} \frac{W}{L} \left( V_{GS} - V_{TH} \right) V_{DS}, \quad V_{DS} \ll 2(V_{GS} - V_{TH}) \]

Voltage-Controlled Resistance

\[ \partial V_{DS} \quad 1 \quad \partial I_{DS} \]

\[ R_{ON} = \frac{1}{\mu_n C_{ox} \frac{W}{L} \left( V_{GS} - V_{TH} \right)} \]
THRESHOLD VOLTAGE AND BODY EFFECT

$V_B < 0$ attracts holes and widens depletion region

→ Larger $V_G > 0$ to put opposite charge on gate
→ Larger $V_G > 0$ to create inversion
→ Higher $V_{TH}$

$$V_{TH} = V_{TH0} + \gamma \left( \sqrt{2\Phi_F + V_{SB}} - \sqrt{2\Phi_F} \right)$$

$0.3 < \gamma < 0.4$ Body effect coefficient

$\Phi_F$ Fermi level

Source-Bulk voltage
CHANNEL LENGTH MODULATION: SATURATION REGION

\[ L' = L - \Delta L \]

\[ \frac{1}{L'} = \frac{1}{L} \left(1 + \frac{\Delta L}{L}\right) = \frac{1}{L} \left(1 + \lambda V_{DS}\right) \]

\[ I_D = \frac{\mu_n C_{ox} W}{2} \frac{V_{GS} - V_{TH}}{L} (V_{GS} - V_{TH})^2 \left(1 + \lambda V_{DS}\right) \]

\[ g_{ds} = \frac{\partial I_{DS}}{\partial V_{DS}} = \lambda \frac{\mu_n C_{ox} W}{2} \frac{V_{GS} - V_{TH}}{L} (V_{GS} - V_{TH})^2 \approx \lambda I_{DS}, \quad \lambda \propto \frac{1}{L} \quad \Rightarrow \quad g_{ds} \propto \frac{I_{DS}}{L} \]
Key Units and Constants for MOS Transistors

\[ 1 \ \mu \text{m} = 10^{-4} \ \text{cm} = 10^{4} \ \text{Å} \]
\[ 1 \ \text{mil} = 25.4 \ \mu \text{m} = 0.0254 \ \text{mm} \]

Electron charge (magnitude): \( q = 1.6 \times 10^{-19} \ \text{C} \)
Permittivity of free space: \( \varepsilon_0 = 8.86 \times 10^{-14} \ \text{F/cm} \)
Permittivity of silicon: \( \varepsilon_\text{s} = \varepsilon_0 K_\text{s} = 1.04 \times 10^{-12} \ \text{F/cm} \); \( K_\text{s} = 11.7 \)
Permittivity of silicon dioxide: \( \varepsilon_\text{ox} = \varepsilon_0 K_\text{ox} = 3.5 \times 10^{-13} \ \text{F/cm} \); \( K_\text{ox} = \)
Oxide capacitance: \( C_\text{ox} = \varepsilon_\text{ox}/\mu_\text{ox} = 3.5 \times 10^{-13} \mu_\text{ox} \ \text{F/cm}^2 \)
Intrinsic carrier concentration: \( n_i = 1.5 \times 10^{10} \ \text{cm}^{-3} \), \( T = 300 \ \text{K} \)
Boltzmann’s constant: \( k = 1.38 \times 10^{-23} \ \text{J/K} \); \( kT/q \) (at \( T = 300 \ \text{K} \)) = 0.6
Electron mobility in Si (\( N_\text{imp} = 10^{17} \ \text{cm}^{-3} \), \( T = 300 \ \text{K} \)): 670 cm²/V · s
Hole mobility in Si (\( N_\text{imp} = 10^{17} \ \text{cm}^{-3} \), \( T = 300 \ \text{K} \)): 220 cm²/V · s

Body-effect coefficient: \( \gamma = \sqrt{2qK_\text{s}/N_\text{imp}} \)

\[ \frac{f_\text{ox}^{\text{cm}}}{K_\text{ox}} = 1.67 \times 10^{-3} \gamma \sqrt{N_\text{imp}} \]

Bulk potential: \( \phi_p = -\frac{kT}{q} \ln \frac{N_\text{imp}}{n_i} = 0.026 \ln (0.67 \times 10^{-10} N_\text{imp}) \)

Drain–Current Relations for MOSFETs in Large-Signal Low-Frequency Operation

<table>
<thead>
<tr>
<th>Region of Operation</th>
<th>NMOS</th>
<th>PMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Triode region:</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
| \(|v_\text{GS}| > |V_T|; \)
| \(|v_\text{DS}| < |v_\text{GS}| - |V_T|\) |
| \(i_D = \mu_n C_\text{ox} \frac{W}{L} (v_\text{GS} - V_T - \frac{v_\text{DS}}{2}) v_\text{DS}\) | \(-i_D = \mu_p C_\text{ox} \frac{W}{L} (v_\text{GS} - V_T - \frac{v_\text{DS}}{2}) v_\text{DS}\) |

| Saturation region   |      |      |
| \(|v_\text{GS}| > |V_T|; \)
| \(|v_\text{DS}| > |v_\text{GS}| - |V_T|\) |
| \(V_T = (V_T)_{v_{gs}=0} + \gamma (\sqrt{2|\phi_p|} + v_{SB} - \sqrt{2|\phi_p|})\) | \(V_T = (V_T)_{v_{gs}=0} - \gamma (\sqrt{2|\phi_p|} - v_{SB} - \sqrt{2|\phi_p|})\) |

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SUBTHRESHOLD CONDUCTION

\[ I_D = I_0 \exp \left( \frac{V_{GS}}{\zeta V_T} \right) \]

- For \( V_{GS} < V_{TH} \), there exists a weak inversion layer causing a small diffusion current.
- This “leakage” current causes increased power dissipation in digital circuits.
- To operate in weak inversion, transistor must be wide → low speed.
- Application: Ultra Low-Power design.
MOS LAYOUT

Contacts (Poly)

Gate (Metal)

Gate

Shared

Gate Contact
PARASITIC CAPACITANCES

- Junction capacitance increases **non-linearly** with reverse bias.
GAT-SOURCE AND GATE DRAIN CAPCITANCES

\[ Q_{ch} \propto W C_{ox} [V_{GS} - V_{TH} - V(x)] \]

- \( C_{gs} \) is maximum in the saturation region
- Device is symmetric in the triode region

\[ C_{GS} \approx \frac{2}{3} W L C_{ox} \]

\[ C_{GS} = C_{GD} \approx \frac{1}{2} W L C_{ox} \]
LOW-FREQUENCY MOS SMALL-SIGNAL MODEL

\[ V_{SB} = 0 \quad \text{and} \quad V_{SB} \neq 0 \]

\[ r_o = \frac{1}{\lambda I_D} \quad : \text{Drain-source resistance} \]

\[ g_{mb} = \frac{\partial I_D}{\partial V_{BS}} = g_m \frac{\gamma}{2\sqrt{2\Phi_F} + V_{SB}} \quad : \text{Bulk transconductance} \]

saturation
HIGH-FREQUENCY SMALL-SIGNAL MODEL

Saturation

Triode

Cut Off
Small-Signal Parameters of MOSFETS in Saturation

<table>
<thead>
<tr>
<th>Parameter</th>
<th>NMOS</th>
<th>PMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transconductance:</td>
<td>$g_m \triangleq \frac{\partial i_D}{\partial v_{GS}}$</td>
<td>$g_m \triangleq \frac{\partial i_D}{\partial v_{GS}}$</td>
</tr>
<tr>
<td>$g_m \triangleq \frac{\partial i_D}{\partial v_{GS}}$</td>
<td>$\frac{\mu_n C_{ox} W}{L} (v_{GS}^0 - V_T) = \sqrt{\frac{2 \mu_n C_{ox} W v_{DS}^0}{L}}$</td>
<td>$- \frac{\mu_p C_{ox} W}{L} (v_{DS}^0 - V_T) = - \sqrt{\frac{2 \mu_p C_{ox} W (-i_D^0)}{L}}$</td>
</tr>
<tr>
<td>Body-effect transconductance:</td>
<td>$g_{mb} \triangleq \frac{\partial i_D}{\partial v_{SB}}$</td>
<td>$g_{mb} \triangleq \frac{\partial i_D}{\partial v_{SB}}$</td>
</tr>
<tr>
<td>$g_{mb} \triangleq \frac{\partial i_D}{\partial v_{SB}}$</td>
<td>$- \frac{\gamma/2}{\sqrt{2 \phi_p + v_{SB}^0}} g_m$</td>
<td>$- \frac{\gamma/2}{\sqrt{2 \phi_p - v_{SB}^0}} g_m$</td>
</tr>
<tr>
<td>Drain conductance:</td>
<td>$g_D \triangleq \frac{\partial i_D}{\partial v_{DS}}$</td>
<td>$g_D \triangleq \frac{\partial i_D}{\partial v_{DS}}$</td>
</tr>
<tr>
<td>$g_D \triangleq \frac{\partial i_D}{\partial v_{DS}}$</td>
<td>$\frac{\lambda i_D^0}{1 + \lambda v_{DS}^0}$</td>
<td>$\frac{\lambda i_D^0}{1 - \lambda v_{DS}^0}$</td>
</tr>
<tr>
<td>Gate-to-source capacitance $C_{gs}$</td>
<td>$\frac{2}{3} W L C_{ox}$</td>
<td>$\frac{2}{3} W L C_{ox}$</td>
</tr>
<tr>
<td>Gate-to-drain capacitance $C_{gd}$</td>
<td>$C_{gd}$ overlap</td>
<td>$C_{gd}$ overlap</td>
</tr>
<tr>
<td>Source (or drain)-to-bulk capacitance $C_{sb} (C_{db})$</td>
<td>$\frac{C_{sb0}}{\sqrt{1 + v_{SB}^0/2 \phi_p}} \cdot \frac{C_{db0}}{\sqrt{1 + v_{DB}^0/2 \phi_p}}$</td>
<td>$\frac{C_{sb0}}{\sqrt{1 - v_{SB}^0/2 \phi_p}} \cdot \frac{C_{db0}}{\sqrt{1 - v_{DB}^0/2 \phi_p}}$</td>
</tr>
</tbody>
</table>
### Terminal Capacitances of a MOSFET in the Three Main Regions of Operation

<table>
<thead>
<tr>
<th>Region of Operation</th>
<th>( C_{gs} )</th>
<th>( C_{gd} )</th>
<th>Capacitance</th>
<th>( C_{gb} )</th>
<th>( C_{sb} )</th>
<th>( C_{db} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cutoff region</td>
<td>( WL_{ov}C_{ox} )</td>
<td>( WL_{ov}C_{ox} )</td>
<td>( WL'C_{ox} )</td>
<td>( A_sC_{pn}(V_{sb}) )</td>
<td>( A_dC_{pn}(V_{db}) )</td>
<td></td>
</tr>
<tr>
<td>Saturation region</td>
<td>( WC_{ox}(L_{ov} + \frac{3}{2}L') )</td>
<td>( WL_{ov}C_{ox} )</td>
<td>( \frac{1}{3}WL'C_{ox}C_{pn}(V_{db}) )</td>
<td>( \frac{1}{3}WL'C_{pn}(V_{sb}) )</td>
<td>( A_dC_{pn}(V_{db}) )</td>
<td></td>
</tr>
<tr>
<td>Nonsaturated (triode)</td>
<td>( WL_{ov}C_{ox} + )</td>
<td>( WC_{ox}(L_{ov} + \frac{1}{2}L') )</td>
<td>( 0 )</td>
<td>( A_sC_{pn}(V_{sb}) ) + ( \frac{2}{3}WL'C_{pn}(V_{sb}) )</td>
<td>( A_dC_{pn}(V_{db}) ) + ( \frac{2}{3}WL'C_{pn}(V_{db}) )</td>
<td></td>
</tr>
</tbody>
</table>

1. \( C_{gd} \): *Gate-to-Drain Capacitance*. This is due to the overlap of the gate and the drain diffusion. It is a thin-oxide capacitance, and hence to a good approximation can be regarded as being voltage independent.

2. \( C_{gs} \): *Gate-to-Source Capacitance*. This capacitance has two components: \( C_{gs_{ov}} \), the gate-to-source thin-oxide overlap capacitance, and \( C_{gs}^* \), the gate-to-channel capacitance. The latter (in the saturation region) is around \( 2/3C_{ox} \), where \( C_{ox} \) is the total thin-oxide capacitance between the gate and the surface of the substrate. In the triode region, \( C_{gs} = C_{ox} \). \( C_{gs} \) is nearly voltage independent in the saturation region.

3. \( C_{sb} \): *Source-to-Substrate Capacitance*. This capacitance also has two components: \( C_{sb_{ps}} \), the \( pn \) junction capacitance between the source diffusion and the substrate, and \( C_{sb}^* \), which can be estimated as two-thirds of the capacitance of the depletion region under the channel. The overall capacitance \( C_{sb} \) has a voltage dependence which is similar to that of an abrupt \( pn \) junction.

4. \( C_{db} \): *Drain-to-Substrate Capacitance*. This is a \( pn \) junction capacitance and is thus voltage dependent.

5. \( C_{gb} \): *Gate-to-Substrate Capacitance*. This capacitance is usually small in the saturation region; its value is around \( 0.1C_{ox} \).
GATE ACCESS RESISTANCE

- Gate resistance effect is significant at RF.
COMMON-SOURCE with RESISTIVE LOAD

\[ A_v = -g_m R_D \]
COMMON-SOURCE with RESISTIVE LOAD: Model

\[ A_v = -g_m \, r_o \parallel R_D \]

\[ R_D \rightarrow \infty \]

\[ A_v = -g_m \, r_o \]
DIODE-CONNECTED MOS

\[(g_m + g_{mb})V_x + \frac{V_x}{r_o} = I_x\]

\[\frac{V_x}{I_x} = \frac{1}{g_m + g_{mb}} \parallel r_o \approx \frac{1}{g_m + g_{mb}}\]
COMMON-SOURCE STAGE with DIODE-CONNECTED LOAD

\[ A_v = -g_{m1} \frac{1}{g_{m2} + g_{mb2}} = -\frac{g_{m1}}{g_{m2}} \frac{1}{1 + \eta} \]

\[ A_v = -\sqrt{\frac{(W / L)_1}{(W / L)_2}} \frac{1}{1 + \eta} \]

- Gain independent of bias current
- Good gain accuracy: good matching

PMOS Diode-Connected Load

\[ A_v = -\sqrt{\frac{u_n (W / L)_1}{u_p (W / L)_2}} \]

- Gain independent of bias current
- Gain set by two different types of transistor
COMMON-SOURCE with CURRENT SOURCE LOAD

Saturation

- Large Output Voltage Compared with Resistive Load
- All Transistors Need to be in Saturation for High Gain
- M1 sets the Minimum Output Voltage
- M2 Sets the Maximum Output Voltage

\[ A_v = -g_m r_{o1} \parallel r_{o2} \]

High-Resistance Node

Triode

\[ A_v = -g_m R_{ON2} \]

\[ R_{ON2} = \frac{1}{\mu_n C_{ox} \left(\frac{W}{L}\right)^2 (V_{DD} - V_b - |V_{THP}|)} \]
COMMON-SOURCE WITH SOURCE DEGENERATIONS

\[ G_m = \frac{g_m}{1 + g_m R_S} \]

\[ A_v = -G_m R_D \]

\[ A_v = \frac{-g_m R_D}{1 + g_m R_S} \]

Including Second-Order Effects

\[ G_m = \frac{g_m r_o}{R_S + [1 + (g_m + g_{mb}) R_S] r_o} \]

\[ A_v = -G_m R_D \parallel R_{OUT} \]
COMMON-SOURCE OUTPUT RESISTANCE

\[ R_{OUT} = [1 + (g_m + g_{mb})r_o]R_S + r_o \]

\[ R_{OUT} = r'_o \approx r_o [1 + (g_m + g_{mb})R_S] \]

\[ A_v = -G_m R_D \parallel r'_o \]

Simplified Model

\[ A_v = \frac{-g_m R_D}{1 + g_m R_S} = -\frac{R_D}{1/g_m + R_S} \]
SOURCE FOLLOWER

Small-Signal Model

Output Resistance

\[ V_{out} = \frac{g_m R_S}{1 + (g_m + g_{mb}) R_S} \]

\[ R_{out} = \frac{1}{g_m + g_{mb}} R_S \approx R_S \frac{1}{g_m} \]

- Source Follower Exhibits a high input resistance and a low output resistance.

Chapter 3
SOURCE FOLLOWER WITH FIXED BIAS CURRENT

- \( I_{d1} \), thus, \( V_{gs1} - V_{th1} \), are independent of \( V_{in} \).

Load Effect on Gain

Application: Buffering a High-Gain Stage

\[
A_v = \frac{1}{g_{mb}} \parallel \frac{1}{r_{o1} \parallel r_{o2} \parallel R_L} \frac{1}{g_m}
\]
**COMMON-GATE**

**Gain**

\[ A_v = \frac{(g_m + g_{mb})r_o + 1}{r_o + (g_m + g_{mb})r_o R_S + R_S + R_D} \quad R_D \approx (g_m + g_{mb})R_D \]

**Output Resistance**

\[ R_{out} = \left\{ \left[ 1 + (g_m + g_{mb})r_o \right] R_S + r_o \right\} \parallel R_D \]

**Input Resistance**

\[ R_{in} = r_o \parallel \frac{1}{g_m} \parallel \frac{1}{g_{mb}} \]
CASCODE AMPLIFIER

\[ A_V \approx g_{m1} \left[ \left( r_{o1} r_{o2} (g_{m2} + g_{mb2}) \right) \parallel R_D \right] \]

\[ Rout = \left\{ \left[ 1 + (g_{m2} + g_{mb2}) r_{o2} \right] r_{o1} + r_{o2} \right\} \parallel R_D \]

\[ \approx \left[ r_{o1} r_{o2} (g_{m2} + g_{mb2}) \right] \parallel R_D \]

Shielding Effect of Cascode

\[ A_V \approx g_{m1} \left[ (r_{o1} r_{o2} g_{m2}) \parallel (r_{o3} r_{o4} g_{m3}) \right] \]
DIFFERENTIAL VERSUS SINGLE-ENDED

Single-Ended Source

Differential Sources

Advantage: Reduced Sensitivity to Supply Noise

Supply Noise

Clock Noise
PSEUDO-DIFFERENTIAL AMPLIFIER

Disadvantage: Sensitive to Input Common-Mode Voltage
DIFFERENTIAL AMPLIFIER

Tail current: Rejects input common mode

Differential-Mode Gain

\[ A_{\text{diff}} = \frac{V_{\text{out1}} - V_{\text{out2}}}{V_{\text{in1}} - V_{\text{in2}}} = g_m R_D \]

Common-Mode Gain

\[ A_c = 0 \]
SMALL-SIGNAL ANALYSIS

Differential-Mode

\[ A_d = -g_m R_D \]

Virtual ground

Common-Mode

\[ A_c = -\frac{R_D / 2}{1/(2g_m) + R_{SS}} \]
$$\frac{V_x - V_y}{V_{in,CM}} = \frac{g_m R_D}{1 + 2g_m R_{SS}}$$

$$\frac{V_x - V_y}{V_{in,CM}} = \frac{(g_m - g_{m2}) R_D}{(g_m + g_{m2}) R_{SS} + 1}$$
DIFF. AMP WITH ACTIVE LOAD

\[ A_d = -g_{mN} \left( g_{mP}^{-1} \parallel r_{oN} \parallel r_{oP} \right) \approx -\frac{g_{mN}}{g_{mP}} \]

\[ A_d = -g_{mN} \left( r_{oN} \parallel r_{oP} \right) \]

\[ A_d \approx g_{m1} \left[ \left( g_{m3} r_{o3} r_{o1} \right) \parallel \left( g_{m5} r_{o5} r_{o7} \right) \right] \]
CURRENT MIRRORS

Reference Current

\[ I_{\text{OUT}} \approx \frac{\mu_n C_{\text{ox}} W}{2L} \left( \frac{R_2}{R_2 + R_1} V_{\text{DD}} - V_{\text{TH}} \right)^2 \]

Sensitive to \( V_{\text{DD}}, V_{\text{th}}, W, L \)
CURRENT-BIASED DIFFERENTIAL AMPLIFIER
CASCODE CURRENT MIRROR

Low-Voltage Cascode
DIFFERENTIAL AMPLIFIER WITH ACTIVE CURRENT MIRROR

Large-Signal Operation

Chapter 5
DIFFERENTIAL AMPLIFIER WITH ACTIVE LOAD

Small-Signal Analysis

\[ I_{D1} = I_{D3} = I_{D4} = g_{m1,2} \frac{V_{in}}{2} \]
\[ I_{D2} = -g_{m1,2} \frac{V_{in}}{2} \]

\[ I_{out} = I_{D2} - I_{D4} = -g_{m1,2} V_{in} \]
\[ \Rightarrow G_m = g_{m1,2} \]

\[ A_v \approx G_m R_{out} \]

\[ R_{out} \approx r_{o2} \parallel r_{o4}, \quad (2r_{o1,2} >> \frac{1}{g_{m3}} \parallel r_{o3}) \]
COMMON-MODE ANALYSIS

Common-Mode Gain

\[ A_{CM} \approx \frac{-1}{1 + 2g_{m1,2}R_{SS} g_{m3,4}} \]

Common-Mode Rejection Ratio

\[ CMRR = \frac{A_{DM}}{A_{CM}} = g_{m3,4}(r_{o1,2} \parallel r_{o3,4})(1 + 2g_{m1,2}R_{SS}) \]
FREQUENCY RESPONSE OF AMPLIFIERS

Single-Pole Passive RC

\[
\frac{V_o(s)}{V_i(s)} = \frac{1/sC}{R + 1/sC} = \frac{1}{1 + RCS} = \frac{1}{1 + s/\omega_p}
\]

\[\omega_p = \frac{1}{2\pi RC} \quad : \text{pole frequency}\]

\[s = j\omega \quad \Rightarrow \quad \frac{V_o(\omega)}{V_i(\omega)} = \frac{1}{1 + jRC\omega} \quad \Rightarrow \quad \left|\frac{V_o(\omega)}{V_i(\omega)}\right|^2 = \frac{1}{1 + (RC\omega)^2}\]

Miller’s Theorem

\[A_v = \frac{V_y}{V_x} \quad \Rightarrow \quad Z_1 = \frac{Z}{1 - A_v} \quad Z_2 = \frac{Z}{1 - A_v^{-1}}\]
AMPLIFIER FREQUENCY RESPONSE ANALYSIS

Capacitance Multiplication

\[ C_1 = C_F (1 - A_v) \quad C_2 = C_F (1 - A^{-1}_v) \approx C_F \]

Association of Poles and Nodes

\[
\frac{V_{out}(s)}{V_{in}(s)} = \frac{A_1}{1 + R_s C_{in} \omega} \frac{A_2}{1 + R_1 C_N \omega} \frac{1}{1 + R_2 C_p \omega}
\]
COMMON-SOURCE FREQUENCY RESPONSE

Approximate Analysis (Miller)

\[
f_{p,\text{in}} = \frac{1}{2\pi R_S \left[ C_{GS} + (1 + g_m R_D) C_{GD} \right]}
\]

\[
f_{p,\text{out}} = \frac{1}{2\pi \left[ (C_{GD} + C_{DB}) R_D \right]}
\]

Exact Analysis

\[
\frac{V_o}{V_i} = \frac{(sC_{GD} - g_m) R_D}{s^2 R_S R_D (C_{GS} C_{GD} + C_{GS} C_{SB} + C_{GD} C_{DB}) + s \left[ R_S (1 + g_m R_D) C_{GD} + R_S C_{GS} + R_D (C_{GD} + C_{DB}) \right] + 1}
\]

\[\omega_z = \frac{g_m}{C_{GD}}\]
SOURCE FOLLOWER OR COMMON DRAIN

\[
\frac{v_O}{v_i} = \frac{g_m + sC_{GS}}{s^2 R_S (C_{GS} C_L + C_{GS} C_{GD} + C_{GD} C_L) + s(g_m R_S C_{GD} + C_{GD} + C_{GS}) + g_m}
\]

\[
f_{p1} \approx \frac{g_m}{2\pi(g_m R_S C_{GD} + C_L + C_{GS})}, \text{ assuming } f_{p2} >> f_{p1}
\]

\[
= \frac{1}{2\pi \left(R_S C_{GD} + \frac{C_L + C_{GS}}{g_m}\right)}
\]
SOURCE FOLLOWER INPUT IMPEDANCE

At low frequencies, \( g_{mb} \gg |sC_L| \)

\[
Z_{in} \approx \frac{1}{sC_{GS}} \left(1 + \frac{g_m}{sC_{GS}}\right) \frac{1}{g_{mb} + sC_L}
\]

\[
\therefore \ C_{in} = C_{GS}g_{mb} / (g_m + g_{mb}) + C_{GD} \quad (\text{same as Miller})
\]

At high frequencies, \( g_{mb} \ll |sC_L| \)

\[
Z_{in} \approx \frac{1}{sC_{GS}} + \frac{1}{sC_L} + \frac{g_m}{s^2C_{GS}C_L}
\]
SOURCE FOLLOWER OUTPUT IMPEDANCE

\[ Z_{OUT} = \frac{V_X}{I_X} = \frac{sR_S C_{GS} + 1}{g_m + sC_{GS}} \]

\[ \approx \frac{1}{g_m}, \text{ at low frequencies} \]
\[ \approx R_S, \text{ at high frequencies} \]

\[ R_2 = \frac{1}{g_m}, \quad R_1 = R_S - \frac{1}{g_m}, \quad L = \frac{C_{GS}}{g_m} \left( R_S - \frac{1}{g_m} \right) \]

Output ringing due to \( C_L \) and inductive component of output impedance.
CASCODE STAGE

\[ f_{pA} = \frac{1}{2\pi R_S \left[ C_{GS1} + C_{GD1} \left( 1 + \frac{g_{m1}}{g_{m2} + g_{mb2}} \right) \right]} \]

\[ f_{pX} = \frac{g_{m2} + g_{mb2}}{2\pi \left( C_{GD1} + C_{DB1} + C_{SB2} + C_{GS2} \right)} \]

\[ f_{pY} = \frac{1}{2\pi R_D \left( C_{DB2} + C_L + C_{GD2} \right)} \]
DIFFERENTIAL PAIR

\[ f_{p1} \approx \frac{1}{2\pi (r_{oN} \parallel r_{oP}) C_L} \]

\[ f_{p2} = \frac{g_{mP}}{2\pi C_E} \]

\[ f_Z = 2f_{p2} = \frac{2g_{mP}}{2\pi C_E} \]
FEEDBACK PRINCIPLES

\[ Y(s) = H(s) [X(s) - G(s)Y(s)] \]
\[ \frac{Y(s)}{X(s)} = \frac{H(s)}{1 + G(s)H(s)} \]

- Gain Desensitization

\[ A_{CL} = \frac{Y}{X} = \frac{A}{1 + A\beta} = \frac{1}{\beta} \cdot \frac{A\beta}{1 + A\beta} \approx \frac{1}{\beta} \]

- Example

\[ A_{CL} = \frac{1}{\beta} \cdot \frac{A\beta}{1 + A\beta} \]
\[ \frac{1}{\beta} = \frac{R_1 + R_2}{R_2} \]

\[ A_{CL} \approx 1 + \frac{R_2}{R_1} \]
FEEDBACK EFFECT ON BANDWIDTH

\[
A_{cl} = \frac{A_0}{1 + j \frac{f}{f_p}}
\]

\[
A_{CL} = \frac{1}{\beta} \frac{A_0 \beta}{(1 + A_0 \beta)(1 + j \frac{f}{f_p})(1 + A_0 \beta)}
\]
FEEDBACK EFFECT ON OUTPUT IMPEDANCE

• Output Impedance

\[ I_X = \frac{V_X - V_M}{R_{out}} = \frac{V_X - (-\beta A_0 V_X)}{R_{out}} \]

\[ \frac{V_X}{I_X} = R_{out,CL} = \frac{R_{out}}{1 + \beta A_0} \]

• Input Impedance

\[ \frac{V_X}{I_X} = R_{in,CL} = R_{in} (1 + \beta A_0) \]
AMPLIFIER TYPES
OP-AMP

Single-Ended Output

Differential Output

Ideal Op-Amp

\[ A_v \rightarrow \infty \]

\[ R_{in} \rightarrow \infty \]

\[ R_{out} = 0 \]
SINGLE-STAGE OP-AMP

- OP-AMP as a voltage buffer
CASCODE OP-AMP: SINGLE-STAGE

Telescopic Cascode

- Higher Gain
- Reduced Output Swing
- Output swing dependent on input swing
IMPROVED SINGLE-ENDED CASCODE OP-AMP

Low-Voltage Cascode Current Mirror
TRIPLE CASCODE

- $A_v \text{ app. } (g_m r_o)^{3/2}$
- Severely Limited Output Swing
- Complex biasing
FOLDED-CASCODE AMPLIFIER

PMOS Input

+ High Gain
+ Output Swing Decoupled from Input Swing
- Reduced Speed

NMOS Input
FOLDED-CASCODE OP-AMP

\[ |A_v| \approx g_{m1} \left[ (g_{m3} + g_{mb3}) r_{o3} \right] r_{o1} \]

Cascode Gain
FOLDED-CASCODE OP-AMP

\[ |A_v| \approx g_{m1} \left\{ \left[ \left( g_{m3} + g_{mb3} \right) r_o3 \left( r_o1 \parallel r_o5 \right) \right] \left[ \left( g_{m7} + g_{mb7} \right) r_o7 r_o9 \right] \right\} \]
TELESCOPIC VERSUS FOLDED CASCODE

Non-dominant Pole

Non-dominant Pole
FOLDED-CASCODE OP-AMP IMPLEMENTATION

Devices in Signal Path

Current-Mirror

signal
SINGLE-ENDED TWO-STAGE OP-AMPS

+ Large Voltage Swing
- Reduced Speed

Single-Ended Output Two-Stage Op Amp

Active Current Mirror
FULLY-DIFFERENTIAL TWO-STAGE OP-AMPS

+ Larger Voltage Swing
+ Better Noise Performance

Ex.1

Ex.2
OUTPUT IMPEDANCE ENHANCEMENT USING FEEDBACK

\[ R_{out} = A_1 g_m 2 r_{o2} r_{o1} \]

Disadvantage: Low swing or Large Supply Voltage
DIFFERENTIAL GAIN BOOSTING

High-Supply

Low-Supply
OP-AMP USING DIFFERENTIAL GAIN BOOSTING

Enhanced Telescopic Cascode

Enhanced Folded Cascode
## COMPARISON

### Performance Comparison of OP-AMP Topologies

<table>
<thead>
<tr>
<th>Gain</th>
<th>Output Swing</th>
<th>Speed</th>
<th>Power Dissipation</th>
<th>Noise</th>
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<tr>
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<td>Highest</td>
<td>Low</td>
<td>Low</td>
</tr>
<tr>
<td>Folded-Cascode</td>
<td>Medium</td>
<td>High</td>
<td>Medium</td>
<td>Medium</td>
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<td>Two-Stage</td>
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<td>Low</td>
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<tr>
<td>Gain-Boosted</td>
<td>High</td>
<td>Medium</td>
<td>Medium</td>
<td>Medium</td>
</tr>
</tbody>
</table>
COMMON-MODE FEEDBACK

Low-Gain Amplifier

High-Gain Amplifier

- Output common-mode voltage in a low-gain diff-pair is well-defined.
- Output common-mode voltage in a low-gain diff-pair is ill-defined.
COMMON-MODE FEEDBACK PRINCIPLE

Auxiliary amplifier sets the output common-mode.

\[ \frac{V_{o1} + V_{o2}}{2} = V_{\text{ref}} = V_{CM} \]

\[ V_{CM} = V_{\text{ref}} \]
COMMON-MODE SENSING METHODS

Resistive

Buffered-Resistive
FOLDED-CASCADE WITH COMMON-MODE CONTROL

(a)

(b)
SIMPLIFIED CMFB

- $M_7$ and $M_8$ in Triode.

- Advantages:
  - Simple, low power

- Disadvantages:
  - Low Accuracy
  - Reduced Output Swing due to $M_7$ and $M_8$
  - Increased Output Parasitic Capacitance

- CMFB with improved output swing:
IMPROVED CMFB

Through Symmetry:

\[ V_{\text{ref}} = V_{\text{CM}} \]

Complete Implementation
TRANSPARENT LARGE-SIGNAL: SLEWING

Slew rate:

\[ SR = \frac{dV_{out}(t)}{dt} = \frac{I_{SS}}{C_L} \]
SLEWING IN TELESCOPIC OP-AMP

Fully-Differential:

\[ SR = \frac{dV_{out}(t)}{dt} = \frac{2I_{SS}}{C_L} \]
FOLDED-CASCODE SLEWING

Fully-Differential:

\[ SR = \frac{dV_{out}(t)}{dt} = \frac{2I_{SS}}{C_L} \]