Why Analog?

• Real-world signals are Analog.
• Signals generated by sensors are analog.
• Digital signal processing of signals requires Analog-to-Digital Conversion.
• Analog signal needs to be amplified and filtered before A/D.
• Amplifiers and Filters are Analog Circuits.
• A/D is a Mixed-Signal Circuit.
Digital signals in a digital communication system behave as analog signals at certain stages of transmission, receive and processing.

Ex 1. Lossy Cable

Ex 2. Disc Drive

Ex 3. Wireless Receiver

Ex 3. Optical Receiver

Signal Attenuation, Noise and Distortion incurred in the propagation channel require that the received signal be Amplified, Filtered and Equalized using Analog circuits.

Why Integrated?

• Larger integration ⇒ larger complexity
• Lower parasitics ⇒ Higher speed
• Lower cost

Moore’s Law: Number of transistors doubles every 18 months:
• 1960: 25 µm Gate length
• Today: 90 nm and 65 nm in production
• 45 nm and 32 nm are in lab. 22nm and 16nm on roadmap.

Why CMOS?

• Digital (Main Driver)
  • Low Power, Simplicity, Scaling, Low cost

• Analog
  • Integration with digital
  • Improved speed over years
Chapter 1

What is Analog Design?

Don't Forget Variations

Performance

Schematic

Layout

Test

Levels of Abstraction

- System Level
- Circuit Level
- Component Level

CAD TOOLS FOR CIRCUIT DESIGN

- Two Dominant Suppliers:
  - Cadence 80% market share
  - Mentor Graphics 20% market share

- Simulation:
  - System Level: Matlab, SPW
  - High-Level (Behavioral): Verilog, Verilog_A, Verilog AMS
  - Low-Level (Electrical): SPICE, SPECTRE, ADS, Proprietary Tools

- Cadence and Mentor Graphics Include tools for
  - Schematic Capture
  - Simulation
  - Layout
Analog Design Space

Tradeoffs

- Analog Design is a Multi-Dimensional Optimization Problem.
- Improving one parameter always results in degradation of some others.
Basic MOS Device Physics

- Understanding Device Physics is Essential to Analog Design.

- MOS device is symmetric.

\[ L_{\text{eff}} = L_{\text{drawn}} - 2L_D \]

<table>
<thead>
<tr>
<th>( L_{\text{drawn}} )</th>
<th>( T_{\text{ox}} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.25 ( \mu \text{m} )</td>
<td>5 nm</td>
</tr>
<tr>
<td>0.18 ( \mu \text{m} )</td>
<td>3.5 nm</td>
</tr>
<tr>
<td>0.13 ( \mu \text{m} )</td>
<td>2.2 nm</td>
</tr>
</tbody>
</table>

- MOS is a four-terminal device.
  - Substrate (bulk) of an NMOS is connected to the lowest potential.
  - Substrate (bulk) of a PMOS is connected to the highest potential.
  - All p-n junctions are reverse biased.
  - Conduction takes place beneath gate, between source and drain.
Complementary MOS Process (CMOS):

**PMOS**

**NMOS**

**MOS CHANNEL FORMATION**

1. **Cut Off**
   - $V_G$ at GND
   - Channel not formed

2. **Depletion**
   - $V_G$ at a positive voltage
   - Channel begins to form

3. **Inversion**
   - $V_G$ at $V_{TH}$
   - Channel fully formed
• Device turn-on is a gradual phenomenon.

• There exists several definitions for $V_{TH}$.

• One definition: when $V_G = V_{TH}$:
  
  \[ \text{density of electrons on the interfaced equals density of holes in the substrate} \]

• $V_{TH}$ increases with increasing the substrate doping.

Adjusting $V_{TH}$ by ion implantation:

• $P^+$ layer increases $V_{TH}$

PMOS in Inversion State

• PMOS: Holes flow from Source to Drain.

• NMOS: Electrons flow from Source to Drain.

• Electrons have a higher Mobility. $\rightarrow$ NMOS is faster than PMOS ($\sim 3$ times).
MOS Symbols

Arrow indicates current flow from positive voltage to negative voltage polarity.

I-V CHARACTERISTICS

- Larger $V_{DS}$ → Larger Longitudinal Field
- Larger $V_{GS}$ → More Charge Carriers
I/V Characteristics (cont.)

\[ I_D = -WC_{ox}[V_{GS} - V_{TH} - V(x)]V \]

Given \( v = \mu E \) and \( E(x) = -\frac{dV(x)}{dx} \)

\[ I_D = WC_{ox}[V_{GS} - V_{TH} - V(x)]L_{ox} \frac{dV(x)}{dx} \]

\[ \int_{x=0}^{L} I_D dx = \int_{V=0}^{V_{DS}} WC_{ox}L_{ox}[V_{GS} - V_{TH} - V(x)]dV \]

\[ I_D = \mu C_{ox} \frac{W}{L} [(V_{GS} - V_{TH})V_{DS} - \frac{1}{2} V_{DS}^2] \]
I-V CHARACTERISTICS: Saturation Region

\[ V_{DS} = V_{GS} - V_{TH} \quad (\text{Pinch-off}) \]

\[ V_{DS} > V_{GS} - V_{TH} \]

\[ I_D = \frac{\mu n C_{ox} W}{2} \frac{V_{GS} - V_{TH}}{L} \left( V_{GS} - V_{TH} \right)^2 \]

\[ L' \approx L \]

MOS OPERATION REGIMES

Both PMOS and NMOS:

- Triode Region \( |V_{DS}| < |V_{GS} - V_{TH}| \)
- Pinch-Off \( |V_{DS}| = |V_{GS} - V_{TH}| \)
- Saturation Region \( |V_{DS}| > |V_{GS} - V_{TH}| \)

• In saturation, MOS behaves as a current source.
Transconductance in Saturation Region

\[ I_D = \frac{\mu_n C_{ox} W}{2L} (V_{GS} - V_{TH})^2 \]

\[ g_m = \frac{\partial I_D}{\partial V_{GS}} \text{constant} \]

\[ = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) \]

\[ g_m = \sqrt{2 \frac{\mu_n C_{ox}}{L} I_D} \]

\[ V_{DS} \text{ constant} \]

DRAIN-SOURCE RESISTANCE IN TRIODE REGION

\[ I_D = \mu_n C_{ox} \frac{W}{L} [(V_{GS} - V_{TH})V_{DS} - \frac{1}{2} V_{DS}^2] \]

\[ R_{ON} = \frac{\partial V_{DS}}{\partial I_{DS}} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})} \]

Voltage-Controlled Resistance
THRESHOLD VOLTAGE AND BODY EFFECT

\[ V_{TH} = V_{TH0} + \gamma \left( \sqrt{2\Phi_F + V_{SB}} - \sqrt{2\Phi_F} \right) \]

\[ 0.3 < \gamma < 0.4 \quad \text{Body effect coefficient} \]

\[ \Phi_F \quad \text{Fermi level} \]

\[ V_B < 0 \text{ attracts holes and widens depletion region} \]
\[ \rightarrow \text{Larger} \ V_G > 0 \ \text{to put opposite charge on gate} \]
\[ \rightarrow \text{Larger} \ V_G > 0 \ \text{to create inversion} \]
\[ \rightarrow \text{Higher} \ V_{TH} \]

\[ V_B < 0 \text{ attracts holes and widens depletion region} \]
\[ \rightarrow \text{Larger} \ V_G > 0 \ \text{to put opposite charge on gate} \]
\[ \rightarrow \text{Larger} \ V_G > 0 \ \text{to create inversion} \]
\[ \rightarrow \text{Higher} \ V_{TH} \]

\[ 4.0 \quad \text{Body effect coefficient} \]

Source-Bulk voltage

CHANNEL LENGTH MODULATION: SATURATION REGION

\[ 1/ L' = \frac{1}{L} + (1 + \Delta L / L) = \frac{1}{L} + \lambda \delta \]

\[ I_D = \frac{\mu F C_{ox}}{2} W \left( V_{GS} - V_{TH} \right)^2 \left( 1 + \lambda \delta \right) \]

\[ g_m = \frac{\partial I_D}{\partial V_{DS}} = \lambda \frac{\mu F C_{ox}}{2} W \left( V_{GS} - V_{TH} \right)^2 \approx \lambda I_{DS}, \ \lambda \propto \frac{1}{L}, \ \Rightarrow \ g_m \propto \frac{I_{DS}}{L} \]

\[ V_{GS2} \quad V_{DS} \]

\[ V_{GS1} \quad V_{DS} \]
Key Units and Constants for MOS Transistors

1. \( \mu m = 10^{-6} \text{cm} = 10^6 \text{Å} \)
2. 1 mil = 25.4 \( \mu m = 0.0254 \text{mm} \)

Electron charge (magnitude): \( q = 1.6 \times 10^{-19} \text{C} \)

Permittivity of free space: \( \varepsilon_0 = 8.86 \times 10^{-12} \text{F/cm} \)

Permittivity of silicon: \( \varepsilon_r = 12 \times 10^{-12} \text{F/cm}, K = 11.7 \)

Permittivity of silicon dioxide: \( \varepsilon_{ox} = 3.9 \times 10^{-12} \text{F/cm} \)

Oxide capacitance: \( C_{ox} = \varepsilon_{ox}/\varepsilon_0 = 3.3 \times 10^{-8} \text{F/cm}^2 \)

Intrinsic carrier concentration: \( n_i = 1.5 \times 10^{10} \text{cm}^{-3} \), \( T = 300 \text{K} \)

Boltzmann’s constant: \( k_B = 1.38 \times 10^{-23} \text{J/K} \), \( e = 4.8 \times 10^{-10} \text{cm}^2/\text{V-s} \)

Electron mobility in Si \( (\mu_n) = 1000 \text{cm}^2/\text{V-s} \), \( T = 300 \text{K} \)

 Hole mobility in Si \( (\mu_p) = 6.2 \times 10^5 \text{cm}^2/\text{V-s} \), \( T = 300 \text{K} \)

Body-effect coefficient: \( \gamma = \frac{\mu_n \sqrt{K}}{K} \), \( \gamma = 1.67 \times 10^{-3} \text{cm}^2/\text{V-s}^2 \)

Bulk potential: \( \phi_b = \frac{8\pi}{3} \ln\left( \frac{N_{ox}}{n_i} \right) = 0.026 \text{ln} (0.67 \times 10^{-18} N_{ox}) \)

SUBTHRESHOLD CONDUCTION

- For \( V_{GS} < V_{TH} \), there exists a weak inversion layer causing a small diffusion current.
- This “leakage” current causes increased power dissipation in digital circuits.
- To operate in weak inversion, transistor must be wide \( \rightarrow \) low speed.
- Application: Ultra Low-Power design.
MOS LAYOUT

- Gate (Poly)
- Contacts (Metal)

PARASITIC CAPACITANCES

- Junction capacitance increases non-linearly with reverse bias.

University of Massachusetts Amherst
GAT-SOURCE AND GATE DRAIN CAPCITANCES

- $C_{gs}$ is maximum in the saturation region
- Device is symmetric in the triode region

\[ Q_{ch} \propto W C_{ox} [V_{GS} - V_{TH} - V(x)] \]

- $C_{gs}$

LOW-FREQUENCY MOS SMALL-SIGNAL MODEL

\[ r_o = \frac{1}{\lambda D} \quad : \text{Drain-source resistance} \]

\[ g_{mb} = g_m \frac{\gamma}{2 \sqrt{2 \Phi F + V_{SB}}} \quad : \text{Bulk transconductance} \]

\[ V_{SB} = 0 \quad V_{SB} \neq 0 \]
Chapter 2

High-Frequency Small-Signal Model

Saturation

\[ g_s = \frac{\partial I_d}{\partial V_{gs}} \]

\[ g_{ds} = \frac{\partial I_d}{\partial V_{ds}} \]

\[ V_d = \frac{g_m}{g_{ds}} \]

\[ r_o = \frac{1}{g_{ds}} \]

\[ C_{gd} = \frac{1}{g_{ds}} \]

\[ C_{gs} = \frac{1}{g_m} \]

\[ C_{gs} = \frac{1}{g_m} \]

\[ C_{db} = C_{db} \]

\[ C_{db} = C_{db} \]

\[ C_{db} = C_{db} \]

\[ \text{Cut Off} \]

\[ \text{Triode} \]

Small-Signal Parameters of MOSFETs in Saturation:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>NMOS</th>
<th>PMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transconductance:</td>
<td>[ g_m = \frac{W}{L} ] [ g_m = \frac{W}{L} ]</td>
<td>[ g_m = \frac{W}{L} ] [ g_m = \frac{W}{L} ]</td>
</tr>
<tr>
<td>Body-effect transconductance:</td>
<td>[ g_{ds} = \frac{1}{T} ] [ g_{ds} = \frac{1}{T} ]</td>
<td>[ g_{ds} = \frac{1}{T} ] [ g_{ds} = \frac{1}{T} ]</td>
</tr>
<tr>
<td>Drain conductance:</td>
<td>[ g_d = \frac{1}{T} ] [ g_d = \frac{1}{T} ]</td>
<td>[ g_d = \frac{1}{T} ] [ g_d = \frac{1}{T} ]</td>
</tr>
<tr>
<td>Gate-to-source capacitance ( C_{gs} ):</td>
<td>[ C_{gs} = \frac{W}{L} ] [ C_{gs} = \frac{W}{L} ]</td>
<td>[ C_{gs} = \frac{W}{L} ] [ C_{gs} = \frac{W}{L} ]</td>
</tr>
<tr>
<td>Gate-to-drain capacitance ( C_{gd} ):</td>
<td>[ C_{gd} = \frac{1}{T} ] [ C_{gd} = \frac{1}{T} ]</td>
<td>[ C_{gd} = \frac{1}{T} ] [ C_{gd} = \frac{1}{T} ]</td>
</tr>
<tr>
<td>Source (or drain) to bulk capacitance ( C_{ds} ):</td>
<td>[ C_{ds} = \frac{1}{T} ] [ C_{ds} = \frac{1}{T} ]</td>
<td>[ C_{ds} = \frac{1}{T} ] [ C_{ds} = \frac{1}{T} ]</td>
</tr>
</tbody>
</table>

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Terminal Capacitances of a MOSFET in the Three Main Regions of Operation

<table>
<thead>
<tr>
<th>Region of Operation</th>
<th>( C_{gs} )</th>
<th>( C_{gd} )</th>
<th>( C_{gd} )</th>
<th>( C_{ds} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>OFF region</td>
<td>( W_{os}C_{ox} )</td>
<td>( W_{os}C_{ox} )</td>
<td>( W_{os}C_{ox} )</td>
<td>( A_{os}C_{ox}(V_{th}) )</td>
</tr>
<tr>
<td>SATuration region</td>
<td>( W_{os}(L_{on} + \frac{W}{2}) )</td>
<td>( W_{os}C_{ox} )</td>
<td>( \frac{W_{os}C_{ox}A_{os}(V_{th})}{C_{ox} + C_{ox}(V_{th})} )</td>
<td>( A_{os}C_{ox}(V_{th}) )</td>
</tr>
<tr>
<td>Nonlinear region</td>
<td>( \frac{W_{os}C_{ox}}{\sqrt{w/C_{ox}}} )</td>
<td>( \frac{W_{os}(L_{on} + \frac{W}{2})}{\sqrt{w/C_{ox}}} )</td>
<td>0</td>
<td>( A_{os}C_{ox}(V_{th}) ) + ( \frac{W_{os}C_{ox}A_{os}(V_{th})}{\sqrt{w/C_{ox}}} )</td>
</tr>
</tbody>
</table>

1. \( C_{gs} \): Gate-to-Source Capacitance. This is due to the overlap of the gate and the drain diffusion. It is a thin-oxide capacitance, and hence is a good approximation can be regarded as being voltage independent.

2. \( C_{gd} \): Gate-to-Drain Capacitance. This capacitance has two components: \( C_{gd} \), the gate-to-source thin-oxide overlap capacitance, and \( C_{gd} \), the gate-to-channel capacitance. The latter (in the saturation region) is around \( 2\Delta C_{ox} \), where \( C_{ox} \) is the total thin-oxide capacitance between the gate and the surface of the substrate. In the linear region, \( C_{gd} \) is nearly voltage independent in the saturation region.

3. \( C_{ds} \): Source-to-Substrate Capacitance. This capacitance also has two components: \( C_{ds} \), the pn junction capacitance between the source diffusion and the substrate, and \( C_{ds} \), which can be estimated as two-thirds of the capacitance of the depletion region under the channel. The overall capacitance \( C_{ds} \) has a voltage dependence which is similar to that of an abrupt pn junction.

4. \( C_{os} \): Drain-to-Substrate Capacitance. This is a pn junction capacitance and is thus voltage dependent.

5. \( C_{ps} \): Gate-to-Source Capacitance. This capacitance is usually small in the saturation region, its value is around \( 0.1\Delta C_{ox} \).

---

**GATE ACCESS RESISTANCE**

- Gate resistance effect is significant at RF.

---

Chapter 2

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COMMON-SOURCE with RESISTIVE LOAD

A\_v = -g\_m R\_D

COMMON-SOURCE with RESISTIVE LOAD: Model

A\_v = -g\_m r\_o \parallel R\_D

R\_D \rightarrow \infty

A\_v = -g\_m r\_o
DIODE-CONNECTED MOS

\[(g_m + g_{mb})V_x + \frac{V_x}{r_o} = I_x\]

\[\frac{V_x}{I_x} = \frac{1}{g_m + g_{mb}} \approx \frac{1}{g_m + g_{mb}}\]

Chapter 3

COMMON-SOURCE STAGE with DIODE-CONNECTED LOAD

\[A_v = -g_m \frac{1}{1 + \eta} = -g_{m2} \frac{1}{g_{m2} 1 + \eta}\]

\[A_v = -\sqrt{\frac{(W/L)_1}{(W/L)_2}} \frac{1}{1 + \eta}\]

- Gain independent of bias current
- Good gain accuracy: good matching

PMOS Diode-Connected Load

\[A_v = -\sqrt{\frac{t_n (W/L)_1}{t_p (W/L)_2}}\]

- Gain independent of bias current
- Gain set by two different types of transistor
COMMON-SOURCE with CURRENT SOURCE LOAD

**Saturation**
- Large Output Voltage Compared with Resistive Load
- All Transistors Need to be in Saturation for High Gain
- M1 sets the Minimum Output Voltage
- M2 Sets the Maximum Output Voltage

\[ A_v = -g_m \frac{r_{o1}}{r_{o2}} \]

**Triode**

\[ A_v = -g_m R_{ON2} \]
\[ R_{ON2} = \frac{1}{\mu \omega C_0 \left( \frac{W}{L} \right) \left( V_{DD} - V_b - |V_{THP}| \right)} \]

Including Second-Order Effects

**COMMON-SOURCE WITH SOURCE DEGENERATIONS**

\[ G_m = \frac{g_m}{1 + g_m R_S} \]
\[ A_v = -G_m R_D \]
\[ A_v = -\frac{g_m R_D}{1 + g_m R_S} \]

\[ G_m = \frac{g_m r_o}{R_S + [1 + (g_m + g_{mob}) R_S] r_o} \]
\[ A_v = -G_m R_D \| R_{OUT} \]

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COMMON-SOURCE OUTPUT RESISTANCE

\[ R_{\text{OUT}} = [1 + (g_m + g_{mb} \cdot r_o)] R_S + r_o \]

\[ R_{\text{OUT}} = r_o' \approx r_o \cdot [1 + (g_m + g_{mb} \cdot R_S)] \]

\[ A_v = -G_m \cdot R_D \parallel r_o' \]

Simplified Model

\[ A_v = \frac{-g_m \cdot R_D}{1 + g_m \cdot R_S} = -\frac{R_D}{1/g_m + R_S} \]

SOURCE FOLLOWER

Small-Signal Model

\[ A_v = \frac{g_m \cdot R_S}{1 + (g_m + g_{mb}) \cdot R_S} = \frac{R_S}{1/g_m + (g_m + g_{mb}) R_S} \approx \frac{R_S}{1/g_m + R_S} \]

Output Resistance

\[ R_{\text{out}} = \frac{1}{g_m} \parallel \frac{1}{g_{mb}} = \frac{1}{g_m + g_{mb}} \]

* Source Follower Exhibits a high input resistance and a low output resistance.*
**SOURCE FOLLOWER WITH FIXED BIAS CURRENT**

- $I_{d1}$, thus, $V_{gs1} = V_{th1}$, are independent of $V_{in}$.

- **Load Effect on Gain**

- **Application: Buffering a High-Gain Stage**

**COMMON-GATE**

- **Gain**

\[
A_v = \frac{(g_m + g_{mb})r_o + 1}{r_o + (g_m + g_{mb})r_o R_s + R_{S} + R_D} R_D \approx (g_m + g_{mb}) R_D
\]

- **Output Resistance**

\[
R_{out} = \{[1 + (g_m + g_{mb})r_o]R_S + r_o\} \ | | \ R_D
\]

- **Input Resistance**

\[
R_{in} = r_o \ | | \ \frac{1}{g_m} \ | | \ \frac{1}{g_{mb}}
\]
**CASCODE AMPLIFIER**

\[
A_v \approx g_m \left\{ \left[ r_{o1} (g_{m2} + g_{mb2}) \right] \parallel R_D \right\} \\
R_{out} = \left\{ \left[ 1 + (g_{m2} + g_{mb2}) r_{o1} + r_{o2} \right] \parallel R_D \right\} \\
\approx \left[ r_{o1} (g_{m2} + g_{mb2}) \right] \parallel R_D
\]

**Shielding Effect of Cascode**

\[
A_v \approx g_m \left\{ \left( r_{o1} r_{o2} g_{m2} \right) \parallel \left( r_{o3} r_{o4} g_{m3} \right) \right\}
\]

---

**DIFFERENTIAL VERSUS SINGLE-ENDED**

**Single-Ended Source**  
**Differential Sources**

**Advantage: Reduced Sensitivity to Supply Noise**

**Clock Noise**  
**Supply Noise**
PSEUDO-DIFFERENTIAL AMPLIFIER

Disadvantage: Sensitive to Input Common-Mode Voltage

Differential Amplifier

Tail current: Rejects input common mode

Differential-Mode Gain

Common-Mode Gain
SMALL-SIGNAL ANALYSIS

Differential-Mode

\[ A_d = -g_m R_D \]

Common-Mode

\[ A_c = \frac{R_D}{2 \left( \frac{1}{2g_m} + R_{SS} \right)} \]

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COMMON-MODE RESPONSE

Load Resistor Mismatch

\[ \frac{V_X - V_Y}{V_{in,CM}} = \frac{g_m R_D}{1 + 2g_m R_{SS}} \]

Transistor Mismatch

\[ \frac{V_X - V_Y}{V_{in,CM}} = \frac{(g_{m1} - g_{m2}) R_D}{(g_{m1} + g_{m2}) R_{SS} + 1} \]

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**DIFF. AMP WITH ACTIVE LOAD**

\[ A_d = -g_m(N)(g^{-1}_{mP} \parallel r_{oN} \parallel r_{oP}) \approx -\frac{g_mN}{g_{mP}} \]

\[ A_d = -g_m(N)(r_{oN} \parallel r_{oP}) \]

\[ A_d \approx g_{m1}[g_m3r_{o3}r_{o1}) \parallel (g_m5r_{o5}r_{o7})] \]

**CURRENT MIRRORS**

**Reference Current**

\[ I_{out} \approx \frac{\mu C_{in} W}{2 L} \frac{R_2}{R_1 + R_2} (V_{DD} - V_{TH})^2 \]

Sensitive to \( V_{DD}, V_{TH}, W, L \)
CURRENT-BIASED DIFFERENTIAL AMPLIFIER

CASCODE CURRENT MIRROR

Low-Voltage Cascode
DIFFERENTIAL AMPLIFIER WITH ACTIVE CURRENT MIRROR

Large-Signal Operation

\[ I_{D1} = I_{D3} = I_{D4} = g_{m1,2} V_{in} / 2 \quad I_{D2} = -g_{m1,2} V_{in} / 2 \]

\[ I_{out} = I_{D2} - I_{D4} = -g_{m1,2} V_{in} \quad \Rightarrow G_m = g_{m1,2} \]

\[ R_{out} \approx r_{o2} \parallel r_{o4} \cdot (2r_{d1,2} >> [1/g_{m3}] || r_{o3}) \quad A_c \approx G_m R_{out} \]

Differential Amplifier with Active Load

Small-Signal Analysis

\[ A_v \approx G_m R_{out} \]
COMMON-MODE ANALYSIS

Common-Mode Gain

\[ A_{CM} \approx \frac{-1}{1 + 2g_{m1,2}R_{SS}} g_{m3,4} \]

Common-Mode Rejection Ratio

\[ CMRR = \frac{A_{DM}}{A_{CM}} = g_{m3,4} \left( r_{o1,2} || r_{o3,4} \right) (1 + 2g_{m1,2}R_{SS}) \]

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FREQUENCY RESPONSE OF AMPLIFIERS

Single-Pole Passive RC

\[ \frac{V_i(s)}{V_o(s)} = \frac{1}{sC} \left( \frac{R + 1/sC}{1 + s / \omega_p} \right) \]

\[ \omega_p = 1/2 \pi RC \quad : \text{pole frequency} \]

\[ s = j\omega \quad \Rightarrow \quad \frac{V_i(\omega)}{V_o(\omega)} = \frac{1}{1 + jRC\omega} \quad \Rightarrow \quad \left| \frac{V_o(\omega)}{V_i(\omega)} \right|^2 = \frac{1}{1 + (RC\omega)^2} \]

Miller's Theorem

\[ A_v = \frac{V_o}{V_x} \quad \Rightarrow \quad Z_1 = \frac{Z}{1 - A_v} \quad Z_2 = \frac{Z}{(1 - A_v)} \]

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AMPLIFIER FREQUENCY RESPONSE ANALYSIS

Capacitance Multiplication

\[ C_1 = C_p (1 - A_v) \]
\[ C_2 = C_p (1 - A^{-1}_v) = C_p \]

Association of Poles and Nodes

\[
\frac{V_{out}(s)}{V_{in}(s)} = \frac{A_1 A_2}{1 + R_c C_p \omega 1 + R_p C_p \omega 1 + R_c C_p \omega}
\]

COMMON-SOURCE FREQUENCY RESPONSE

Approximate Analysis (Miller)

\[ f_{p,in} = \frac{1}{2 \pi R_s [C_{GS} + (1 + g_m R_D) C_{GD}]} \]
\[ f_{p,out} = \frac{1}{2 \pi [(C_{GD} + C_{DS}) R_D]} \]

Exact Analysis

\[
\frac{V_{out}}{V_{in}} = \frac{(sC_{GD} - g_m)R_D}{s^2 R_s R_p (C_{GD} + C_{GD} C_{DB} + C_{GD} C_{DB}) + sR_c R_p (1 + g_m R_D) C_{GD} + R_c C_{GD} + R_D (C_{GD} + C_{DB}) + 1}
\]
### SOURCE FOLLOWER OR COMMON DRAIN

![Source Follower or Common Drain Circuit Diagram]

\[ V_{DO} = \frac{g_m + sC_{GS}}{s^2R_s(C_{GD}C_L + C_{GD}C_{GD} + C_{GD}C_L) + s(g_mR_sC_{GD} + C_{GD} + C_{GS}) + g_m} \]

\[ f_{pa} \approx \frac{s}{2\pi(g_mR_sC_{GD} + C_L + C_{GS})}, \text{ assuming } f_{pa} \gg f_{pa} \]

\[ Z_{in} \approx \frac{1}{sC_{GS}} + \left(1 + \frac{g_m}{sC_{GS}}\right) \frac{1}{g_{mb} + sC_L} \]

At low frequencies, \( g_{mb} \gg |sC_L| \)

\[ Z_{in} \approx \frac{1}{sC_{GS}} \left(1 + \frac{g_m}{g_{mb}}\right) + \frac{1}{g_{mb}} \]

\[ C_{in} = C_{GS}g_{mb}/(g_m + g_{mb}) + C_{GD} \text{ (same as Miller)} \]

At high frequencies, \( g_{mb} \ll |sC_L| \)

\[ Z_{in} \approx \frac{1}{sC_{GS}} + \frac{1}{sC_L} + \frac{g_m}{s^2C_{GS}C_L} \]
**SOURCE FOLLOWER OUTPUT IMPEDANCE**

\[
Z_{\text{OUT}} = \frac{V_x}{I_x} = \frac{sR_s C_{GS} + 1}{\frac{g_m}{s C_{GS}}} \\
\approx \frac{1}{g_m}, \text{ at low frequencies} \\
\approx R_s, \text{ at high frequencies}
\]

\[
R_2 = \frac{1}{g_m}, \quad R_1 = R_s - \frac{1}{g_m}, \quad L = \frac{C_{GS}}{g_m} (R_s - \frac{1}{g_m})
\]

Output ringing due to \(C_L\) and inductive component of output impedance.

**CASCODE STAGE**

\[
f_{pX} = \frac{1}{2\pi R_s \left[ C_{gs1} + C_{gs2} \left( 1 + \frac{g_{m1}}{g_{m2} + g_{m2}} \right) \right]}
\]

\[
f_{pX} = \frac{g_{m2} + g_{m1}}{2\pi \left( C_{gs1} + C_{gs2} + C_{gs2} + C_{gs2} \right)}
\]

\[
f_{pY} = \frac{1}{2\pi R_s \left( C_{db2} + C_L + C_{gd2} \right)}
\]
DIFFERENTIAL PAIR

\[ f_{p1} \approx \frac{1}{2\pi (r_{oN} \parallel r_{oP}) C_L} \]
\[ f_{p2} = \frac{g_{mP}}{2\pi C_E} \]
\[ f_L = 2f_{p2} = \frac{2g_{mP}}{2\pi C_E} \]

FEEDBACK PRINCIPLES

\[ Y(s) = H(s)[X(s) - G(s)Y(s)] \]
\[ \frac{Y(s)}{X(s)} = \frac{H(s)}{1 + G(s)H(s)} \]

* Gain Desensitization

\[ A_{CL} = \frac{Y}{X} = \frac{A}{1 + A\beta} = \frac{1}{\beta} \cdot \frac{A\beta}{1 + A\beta} \approx \frac{1}{\beta} \]

* Example

\[ A_{CL} = 1 + \frac{A\beta}{1 + A\beta} \]
\[ \frac{1}{\beta} = \frac{R_1}{R_2} \]
\[ A_{CL} \approx 1 + \frac{R_2}{R_1} \]
FEEDBACK EFFECT ON BANDWIDTH

\[ A_{cl} = \frac{1}{\beta} \frac{A_b \beta}{(1 + f/f_p)(1 + j\omega L + 1)} \]

FEEDBACK EFFECT ON OUTPUT IMPEDANCE

• Output Impedance

\[ I_X = \frac{V_X - V_M}{R_{out}} = \frac{V_X - (-\beta A_0 V_X)}{R_{out}} \]

\[ V_X = R_{out,CL} = \frac{R_{out}}{1 + \beta A_0} \]

• Input Impedance

\[ V_I = R_{in,CL} = R_{in}(1 + \beta A_0) \]
AMPLIFIER TYPES

Chapter 8

OP-AMP

Single-Ended Output

Differential Output

Ideal Op-Amp

\[ A_v \rightarrow \infty \]

\[ R_{in} \rightarrow \infty \]

\[ R_{out} = 0 \]

Chapter 9
SINGLE-STAGE OP-AMP

- OP-AMP as a voltage buffer

CASCODE OP-AMP: SINGLE-STAGE

Telescopic Cascode

+ Higher Gain
- Reduced Output Swing
- Output swing dependent on input swing

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Chapter 9

IMPROVED SINGLE-ENDED CASCODE OP-AMP

Low-Voltage Cascode Current Mirror

Chapter 9

TRIPLE CASCODE

- $A_v \approx (g_{m1} r_o)^3/2$
- Severely Limited Output Swing
- Complex biasing
FOLDED-CASCODE AMPLIFIER

PMOS Input

NMOS Input

+ High Gain
+ Output Swing Decoupled from Input Swing
- Reduced Speed

FOLDED-CASCODE OP-AMP

\[
|A_v| \approx g_{m3} \left[ \left( g_{m3} + g_{mb3} \right) r_{o3} \right] r_{o1}
\]

Cascode Gain
\[ |A_v| \approx g_{m1} \left\{ \left( g_{m3} + g_{mb3} \right) r_3 \left( r_{o1} \parallel r_{o5} \right) \right\} \left\{ \left( g_{m7} + g_{mb7} \right) r_7 r_{o9} \right\} \]

TELESCOPIC VERSUS FOLDED CASCODE

Non-dominant Pole

Non-dominant Pole
FOLDED-CASCODE OP-AMP IMPLEMENTATION

Current-Mirror

Devices in Signal Path

CURRENT-MIRROR

SINGLE-ENDED TWO-STAGE OP-AMPS

+ Large Voltage Swing
- Reduced Speed

Single-Ended Output Two-Stage Op Amp

Active Current Mirror
FULLY-DIFFERENTIAL TWO-STAGE OP-AMPS

+ Larger Voltage Swing
+ Better Noise Performance

Ex.1

Output Impedance Enhancement Using Feedback

\[ R_{out} = A g_{m2} r_{o2} r_{o1} \]

Disadvantage: Low swing or Large Supply Voltage

Regulated Cascode
DIFFERENTIAL GAIN BOOSTING

High-Supply

Low-Supply

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OP-AMP USING DIFFERENTIAL GAIN BOOSTING

Enhanced Telescopic Cascode

Enhanced Folded Cascode

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**COMPARISON**

Performance Comparison of OP-AMP Topologies

<table>
<thead>
<tr>
<th>Gain</th>
<th>Output Swing</th>
<th>Speed</th>
<th>Power Dissipation</th>
<th>Noise</th>
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<tbody>
<tr>
<td>Telescopic</td>
<td>Medium</td>
<td>Highest</td>
<td>Low</td>
<td>Low</td>
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<tr>
<td>Folded-Cascode</td>
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<td>Medium</td>
<td>Medium</td>
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<td>Medium</td>
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<td>Gain-Boosted</td>
<td>High</td>
<td>Medium</td>
<td>Medium</td>
<td>High</td>
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**COMMON-MODE FEEDBACK**

- Output common-mode voltage in a low-gain diff-pair is well-defined.
- Output common-mode voltage in a low-gain diff-pair is ill-defined.

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COMMON-MODE FEEDBACK PRINCIPLE

Auxiliary amplifier sets the output common-mode.

\[
\frac{V_{x1} + V_{x2}}{2} = V_{\text{ref}} = V_{CM}
\]

COMMON-MODE SENSING METHODS

Resistive

Buffered-Resistive
FOLDED-CASCODE WITH COMMON-MODE CONTROL

(a)

(b)

SIMPLIFIED CMFB

- $M_7$ and $M_8$ in Triode.

- Advantages:
  - Simple, low power

- Disadvantages:
  - Low Accuracy
  - Reduced Output Swing due to $M_7$ and $M_8$
  - Increased Output Parasitic Capacitance

- CMFB with improved output swing:
**IMPROVED CMFB**

Through Symmetry:

\[ V_{\text{ref}} = V_{\text{CM}} \]

Complete Implementation

**TRANSIENT LARGE-SIGNAL: SLEWING**

Slew rate:

\[ SR = \frac{dV_{\text{out}}(t)}{dt} = \frac{I_{SS}}{C_L} \]
SLEWING IN TELESCOPIC OP-AMP

Fully-Differential:
\[ SR = \frac{dV_{out}(t)}{dt} = \frac{2I_{SS}}{C_L} \]

FOLDED-CASCODE SLEWING

Fully-Differential:
\[ SR = \frac{dV_{out}(t)}{dt} = \frac{2I_{SS}}{C_L} \]