Homework 6

Due before class Wednesday, November 25, 2009. Assume room temperature \( T = 300 \) K in all problems

1. (a) Using the figures on pages 133 and 134 of the Lecture Notes, Part II, as a guide, sketch the band diagram of an MOS capacitor with an \( n \)-type Si substrate in
   i) accumulation, ii) at flat band condition, and iii) at the onset of strong inversion (that is, \( \psi_s = 2 \psi_B \)). Assume an Al gate with electron affinity \( e\phi_M = 3.0 \) eV, use for Si the work-function \( e\chi = 3.2 \) eV, and assume the \( n \)-type substrate to be doped with \( N_D = 3 \times 10^{17} \) donors/cm\(^3\).

(b) What is the value of the flatband voltage \( V_{FB} \) and of the threshold voltage \( V_{T0} \) (see Eq. (247) of the Notes, Part III)?

(c) What is the value of the depletion capacitance \( C_D \) at the onset of strong inversion?

2. Assuming an oxide thickness \( t_{ox} \) of 5 nm and a gate area of 100 \( \mu m^2 \), sketch the capacitance-voltage \( (C - V) \) characteristics of the MOS capacitor of problem 1, as in the figure at page 140 of the Lecture Notes. Recall that this capacitor is on an \( n \)-type substrate!

3. Consider a Si \( n \)MOSFET with the following parameters:
   substrate doping (\( p \)-type): \( N_A = 5 \times 10^{16} \) cm\(^{-3} \)
   channel length \( L = 0.5 \) \( \mu m \)
   gate width \( W = 5 \) \( \mu m \)
   electron mobility \( \mu_n = 600 \) cm\(^2\)/Vs
   oxide thickness \( t_{ox} = 15 \) nm
   flatband voltage \( V_{FB} = 0 \).
   Using the simplified model of the Lecture Notes, pages 159-162, especially Eq. (255), plot as accurately as you can the \( I_D - V_D \) characteristics of the device assuming that the source contact is grounded (that is, \( V_S = 0 \)). More specifically, plot \( I_D \)-vs-\( V_D \) for \( V_G - V_{T0} = 0.0, 0.5, 1.0, 1.5, \) and \( 2.0 \) V for \( V_D \) ranging from 0 to 5 V. Indicate as best as you can the separation between the linear and saturated region by computing \( V_{D, sat} \) for the various values of \( V_G - V_{T0} \). Also indicate the value of the threshold voltage \( V_{T0} \).
4. As in problem 3 above, plot the same $I_D - V_D$ characteristics, but now account for the degradation of the electron mobility with increasing $V_G$ via Eq. (298) of the Lecture Notes. To do this, just replace $\mu_n$ in Eq. (255) with $\mu_{\text{eff}}$ given by Eq. (298). Use a value of $K$ such that $K C_{ox}/(2\epsilon_s) = 0.5 \, \text{V}^{-1}$.

5. Consider a Si $n$MOSFET with the following parameters:
   
   - substrate doping ($p$-type): $N_A = 5 \times 10^{16} \, \text{cm}^{-3}$
   - channel length $L = 1.0 \, \mu\text{m}$
   - gate width $W = 10 \, \mu\text{m}$
   - electron mobility $\mu_n = 600 \, \text{cm}^2/\text{Vs}$
   - oxide thickness $t_{ox} = 4 \, \text{nm}$
   - threshold voltage $V_{T0} = 1 \, \text{V}$

   Using, as in the previous problem, the simplified model of the Lecture Notes, pages 159-162, especially Eq. (255), calculate the width of a similar $p$MOSFET giving the same saturated current for the same gate overdrive (that is, at the same value of $|V_G - V_{T0}|$). Assume for the hole mobility a value of $\mu_p = 200 \, \text{cm}^2/\text{Vs}$. If you wish, you may assume also for the threshold voltage of the $p$MOSFET the value of $-1 \, \text{V}$. Recall that in dealing with the $p$FET all polarities ($V_D$ and $V_G$) are switched.

   Do you really need to know the entire set of parameters characterizing the devices in order to reach your answer?