The thickness of the obtained accumulation layer is ~ 10 nm.

Capacitance is $C = \frac{\epsilon_{ox}}{t_{ox}}$ → permittivity of SiO_2

t_{ox} → thickness of the oxide

$$\epsilon_{ox} = \epsilon_{r_{SiO_2}} \times \epsilon_0$$

* Derivation of the thickness of the accumulation layer

Poisson equation $\Rightarrow$ $-\frac{d^2V(x)}{dx^2} = \frac{\rho}{\epsilon_{Si}} = +\frac{q}{\epsilon}(p - n + N_d - N_a)$

$$p(x) = p_{p_0} \exp\left(\frac{-qV(x)}{k_BT}\right) = N_a \exp\left(\frac{-qV(x)}{k_BT}\right)$$

(p_{p_0} → equilibrium.)

$$n(x) = n_{p_0} \exp\left(\frac{qV(x)}{k_BT}\right) = \frac{n_i^2}{N_a} \exp\left(\frac{qV(x)}{k_BT}\right)$$

Far from the surface $V(x \Rightarrow \infty) = 0$.

in the hole accumulation layer formed we assume

$$n \ll p \; ; \quad N_d \ll N_a.$$

$$-\frac{d^2V(x)}{dx^2} = +\frac{q}{\epsilon} N_a \left[\exp\left(\frac{qV(x)}{k_BT}\right) - 1\right]$$

Also we assume that here, the hole concentration is greater than the hole concentration due to doping.

$$p \gg N_a.$$

$$+\frac{d^2V(x)}{dx^2} \simeq -\frac{qN_A}{\epsilon}\exp\left(\frac{-qV(x)}{k_BT}\right)$$

we can integrate this equation if we multiply by $2\frac{dV(x)}{dx}$

$$\Rightarrow 2\frac{dV(x)}{dx}\frac{d^2V(x)}{dx^2} = \frac{2qN_A}{\epsilon}\exp\left(\frac{-qV(x)}{k_BT}\right)\frac{dV(x)}{dx}$$

$$\Rightarrow \frac{d}{dx}\underbrace{\left(\frac{dV}{dx}\right)^2}_{\mathcal{E}^2} = 2\frac{N_A}{\epsilon}k_BT\frac{d}{dx}\left[\exp\left(\frac{-qV(x)}{k_BT}\right)\right]$$

we integrate $\int_x^{x_{acc}}$. x_{acc} thickness of the layer

with $\mathcal{E}(x=x_{acc}) = V(x=x_{acc}) = 0$ neutrality.

$$\boxed{\mathcal{E}^2(x) = \frac{2}{L_D^2}\left(\frac{k_BT}{q}\right)^2\left[\exp\left(-q\beta V(x)\right) - 1\right]}$$

with $L_D = \sqrt{\frac{\epsilon k_BT}{q^2N_A}}$ == Debye length.

Definition of Debye length = distance in semiconductor over which local electric field affects distribution of free charge carriers.

$L_D \searrow$ if concentration $\nearrow$

See textbook p 172-173 for the derivation of $V(x)$ from $E(x)$. [BC's: $V(x_{acc}) = 0$, $V(0) = V_S$

$\Rightarrow$ after calculations

$$V(x) = -\frac{k_B T}{q} \ln\left[\frac{1}{\cos^2\left[\alpha - \frac{x}{\sqrt{2}L_D}\right]}\right]$$

$$\alpha = \cos^{-1}\left(\exp\left(\frac{qV_S}{2k_BT}\right)\right)$$

$$V(x_{acc}) = 0 \Rightarrow \boxed{x_{acc} = \sqrt{2}\, L_D \cos^{-1}\left(\exp\left(\frac{qV_S}{2k_BT}\right)\right)}$$

V_S is in practice very small even for large V_G.

$\Rightarrow x_{acc}$ is small. Since the hole concentration is an exponential function of the potential, the charge density increases rapidly close to the surface.

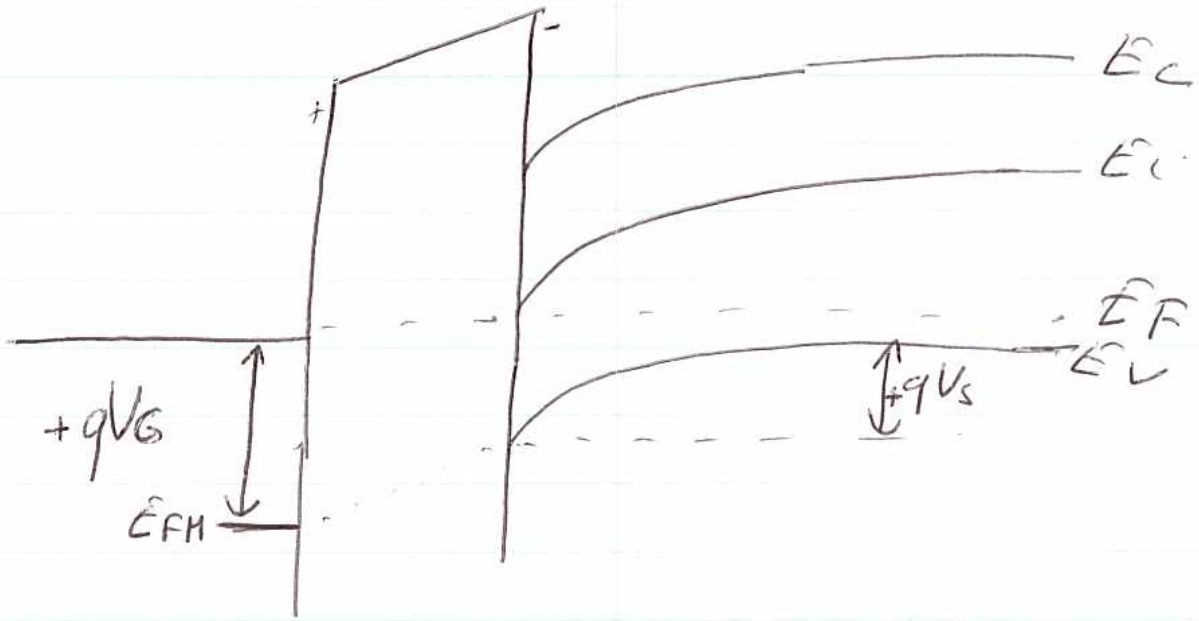
$\Rightarrow$ surface charge

So $\Rightarrow$ $C = \frac{\epsilon_{ox}}{t_{ox}}$ is a good approximation.

~~Surface~~

③ Depletion

if a small positive bias is applied to the gate $V_G > 0$, holes near the Silicon surface are repelled by the gate.
A negative charge appears due to the acceptor doping atoms.



- A positive charge appear at the Gate/Oxide interface
  ⇒ Surface charge
- At the Oxide/Silicon interface it appears a depletion region which extends into the Silicon from $x = 0$, $x = x_{d1}$

* The potential in the depletion region is solution of the Poisson equation.

$$\frac{d^2V(x)}{dx^2} = -\frac{\rho}{\epsilon} = -\frac{q}{\epsilon}\left(p - N_A\right) = \frac{-q}{\epsilon} N_a \left[\exp\left(\frac{-qV(x)}{k_BT}\right) - 1\right]$$

Near the interface $p \ll N_a$; (exponential term is small since the potential is positive)

$$\Rightarrow \frac{d^2V(x)}{dx^2} \simeq \frac{qN_a}{\epsilon} \Rightarrow \text{depletion approximation}$$

B.C $\Rightarrow V(x_d) = 0$, $\left.\frac{dV(x)}{dx}\right|_{x_d} = 0$

$$\Rightarrow \boxed{V(x) = \frac{qN_a}{2\epsilon}(x - x_d)^2}$$

Surface potential $\boxed{V_s = V(x=0) = \frac{qN_a x_d^2}{2\epsilon}}$

$$\Rightarrow \boxed{x_d = \sqrt{\frac{2\epsilon V_s}{qN_a}}}$$

* "the depletion charge" between $x=0$, $x=x_d$ is equal to

$$Q_d = -qN_a x_d = -\sqrt{2q\epsilon N_a V_s}$$

"depletion capacitance" $\boxed{C_D = \epsilon / x_d}$.

* [the gate voltage, V_G, = potential drop across the oxide + potential variation in the semiconductor.

$$\boxed{V_G = V_s + V_{ox} = V_s - \frac{Q_d}{C_{ox}}} \qquad \boxed{C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}}$$

- Capacitance of MOS structure is:

$$C = \frac{dQ_G}{dV_G} = -\frac{dQ_d}{dV_G} = \frac{-dQ_d}{d\left(\frac{-Q_d}{C_{ox}} + V_S\right)} = \frac{-dQ_d/dV_S}{d\left(\frac{-Q_d}{C_{ox}} + V_S\right)/dV_S}$$

$$C = \frac{C_D C_{ox}}{C_D + C_{ox}} = \frac{1}{\frac{1}{C_{ox}} + \frac{1}{C_D}} \Rightarrow \text{with } C_D = \frac{-dQ_D}{dV_S} = \frac{\epsilon}{x_d}$$

- C can also be expressed in function of the gate voltage:

$$V_G = -\frac{Q_d}{C_{ox}} + V_S = \frac{qN_a x_d}{C_{ox}} + \frac{qN_a}{2\epsilon} x_d^2$$

$$\Rightarrow x_d = -\frac{\epsilon}{C_{ox}} + \sqrt{\left(\frac{\epsilon}{C_{ox}}\right)^2 + \frac{2\epsilon}{qN_a} V_G}$$

since

$$C_D = \frac{\epsilon_{Si}}{x_d}$$

$$\Rightarrow \boxed{C = \frac{C_{ox}}{\sqrt{1 + \frac{2C_{ox}^2 V_G}{qN_a\epsilon}}}}$$

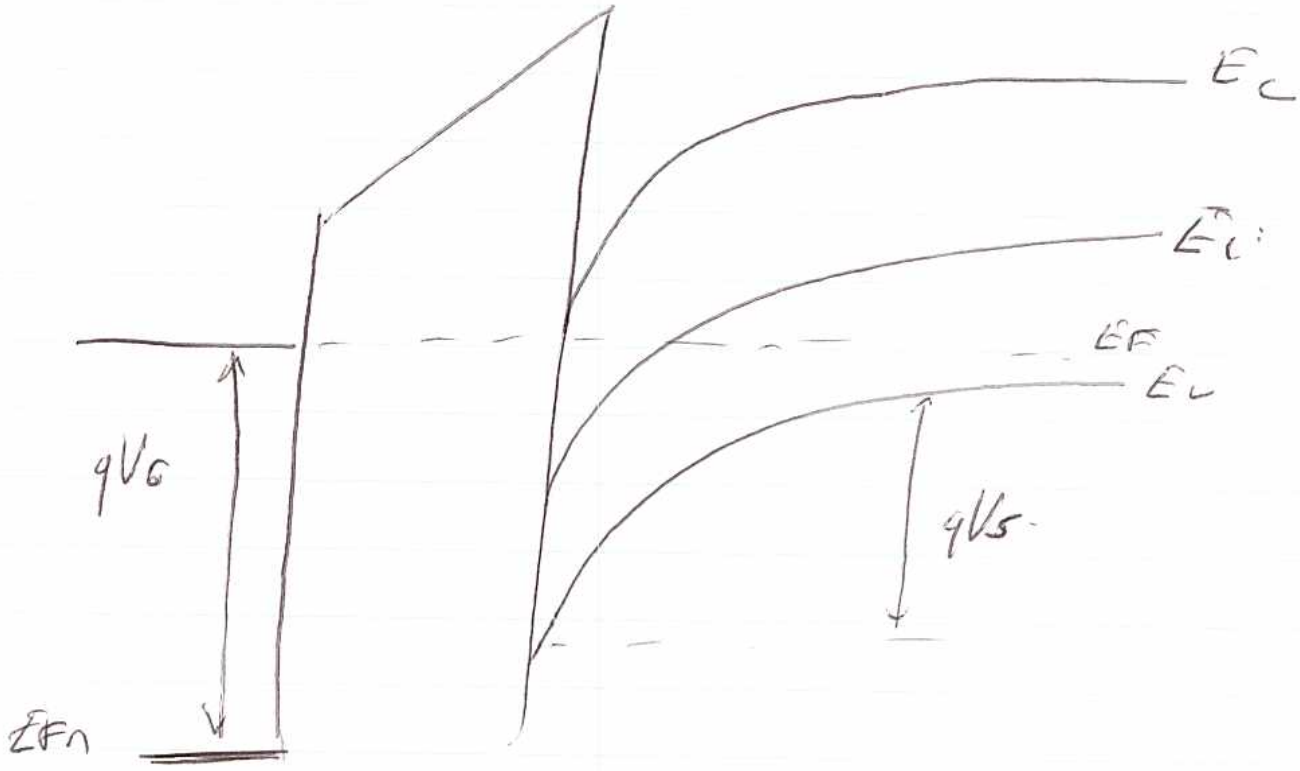
(4) Inversion

If a larger positive voltage is applied $V_G > 0$, the surface potential V_S will continue to increase.

According to the following relation:

$$\begin{cases} p(x=0) = N_a \exp\left(-\dfrac{qV_S}{k_BT}\right) & \text{majority carriers.} \\ n(x=0) = \dfrac{n_i^2}{N_a} \exp\left(\dfrac{qV_S}{k_BT}\right) & \text{minority carriers} \end{cases}$$

$p \searrow$ and $n \nearrow$



At Surface concentration of e^- and holes are equal if

$n(0) = p(0) = n_i$ if $(E_i == E_F)$ at $x = 0$.

Since $\begin{cases} n = n_i \exp(\beta(E_F - E_i)) \\ p = n_i \exp(-\beta(E_F - E_i)) \end{cases}$

$$V_S = \frac{k_B T}{q} \ln\left(\frac{N_a}{n_i}\right)$$

$\Rightarrow$ we have got at $\underline{V_S = V_F}$

$$\left[N_a \exp\left(-q\frac{V_F}{k_B T}\right) = \frac{n_i^2}{N_a} \exp\left(q\frac{V_F}{k_B T}\right) \right] (*)$$

AC: If ~~V_F~~ V_G is increased further

~~$n(0) = p_{p0}$~~ $n(0)$ becomes equal to $p_{p0} = N_a$ which is the original concentration of hole in Silicon.

$\Rightarrow$

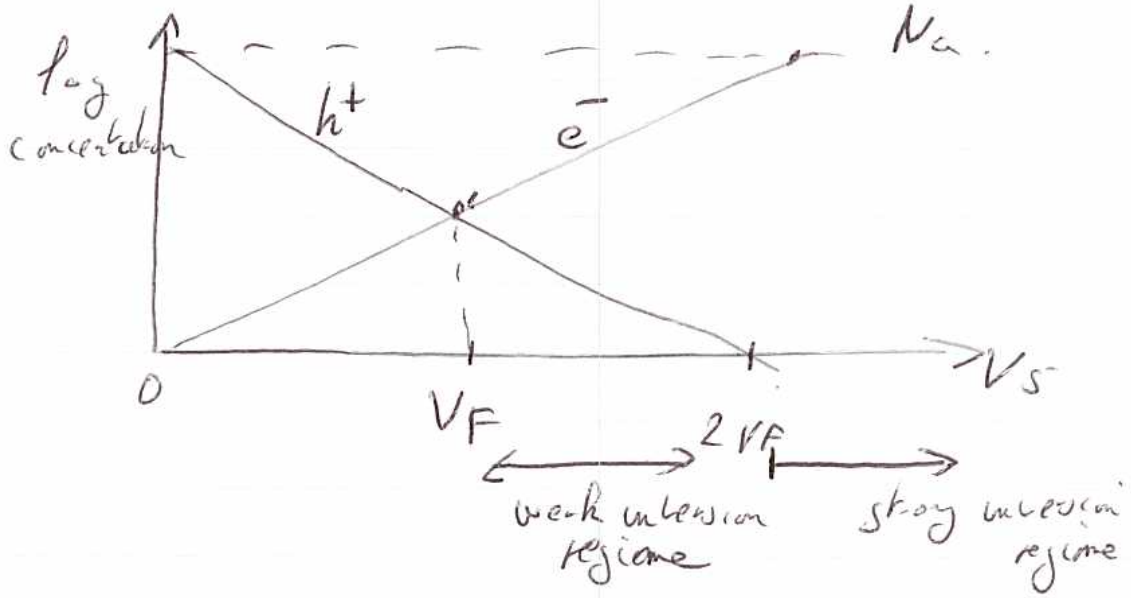
$$N_a = \frac{n_i^2}{N_a} \exp\left(q\frac{V_p}{k_B T}\right)$$

$(*)$

$$N_a \exp\left(-\frac{q V_F}{k_B T}\right) = \frac{n_i^2}{N_a} \exp\left(q\frac{(V_p - V_F)}{k_B T}\right)$$

Using $(*) \Rightarrow V_p - V_F = V_F \Rightarrow \boxed{V_p = 2V_F}$.

Finally we get



The inversion layer is rich in electrons, and therefore, it is a good conductor.

The MOS capacitor consists then of two conducting electrodes, the metal gate and the inversion layer.
As in the case of accumulation, the capacitance of the MOS is once again equal to C_{ox}.

* When an inversion layer is formed e^- are really majority carriers at the surface.
The thickness of the inversion layer remains very small if V_G increases. The electron charge in the layer can be considered as surface charge, as in the case of accumulation, the e^- charge in the inversion layer depends exponentially on the surface potential Quasi $\exp\left(\frac{qV_S}{kTT}\right)$.

- We suppose that $V_S = 2V_F$ when an inversion layer is present [if $V_G \uparrow$ V_S increases only slightly above $2V_F$]

The depth of the depletion region is given by

$$x_{dmax} = \sqrt{\frac{4\epsilon V_F}{qN_a}}$$

(5) Threshold voltage

it is the voltage V_G that must be applied to form an inversion layer.

$$V_G = V_S + \frac{Q_G}{C_{ox}}$$ Q_G is the positive charge at the gate electrode

~~$V_G = V_S - \frac{Q_D}{C_{ox}}$~~

~~$V_{th} = -Q_{ss}$~~.

In practice, the flat-band voltage must be added for "non-ideal" threshold voltage:

$$V_G = V_{FB} + V_S + \frac{Q_G}{C_{ox}} \quad \text{and} \quad Q_G = -(Q_D + Q_{inv})$$

We get

$$V_G = V_{FB} + V_S - \left(\frac{Q_d + Q_{inv}}{C_{ox}}\right)$$

with $\left[Q_d = -qN_a x_{dT} = -\sqrt{2q\epsilon N_A V_S}\right]$

* in the depletion regime $Q_{inv} \simeq 0$ $\quad 0 \leq V_S \leq 2V_F$

$$V_G = V_{FB} + V_S + \frac{\sqrt{2\epsilon q N_A V_S}}{C_{ox}}.$$

* in the inversion regime $Q_{inv} \neq 0$ $\quad V_S > 2V_F$.

$$\boxed{V_G = V_{FB} + V_S + \frac{\sqrt{2\epsilon q N_A V_S}}{C_{ox}} - \frac{Q_{inv}}{C_{ox}} \equiv V_T - \frac{Q_{inv}}{C_{ox}}.}$$

where $\boxed{V_T = V_{FB} + V_S + \frac{\sqrt{2\epsilon q N_A V_S}}{C_{ox}}}$ Threshold voltage.

Remark the flat band potential can be affected by the presence of charge in the oxide or oxide/semiconductor interface.

if Q_i is the charge at the surface and ρ_{ox} is the charge density distributed within the oxide.

then the flat band voltage becomes.

$$V_{FB} = V_{MS} - \frac{Q_i}{C_{ox}} - \frac{1}{\epsilon_{ox}} \int_0^{t_{ox}} x \rho_{ox}(x)\, dy$$

V_{MS} — already defined as

$$V_{MS} = V_M - \left(\chi + \frac{E_g}{2} + V_B\right)$$

C_{ox} — charge at oxide/semi interface

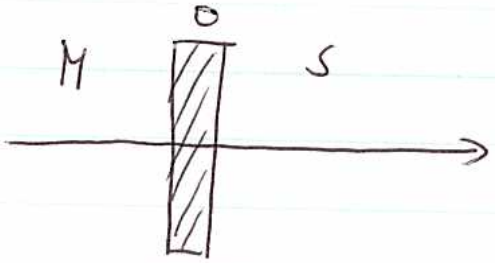
$\rho_{ox}(x)$ — charge density in the oxide

* The actual calculation of the flatband voltage is further complicated by the fact that charge can move within the oxide - Also the charge at the oxide/semic. due to surface state depends on the position of the Fermi energy.

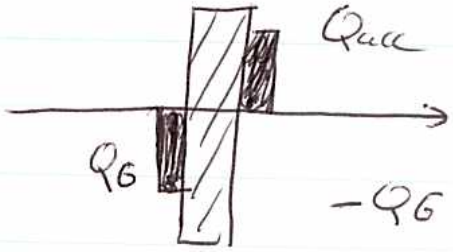
6 Summary

Charges in the MOS structure

Flat band



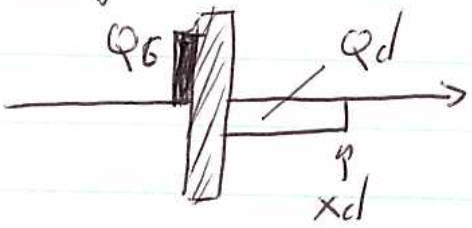
Accumulation



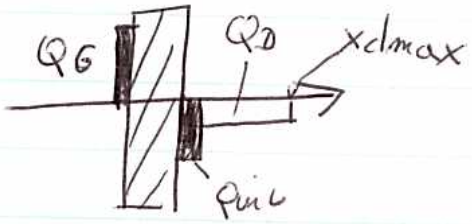
$-Q_G = Q_{acc}$

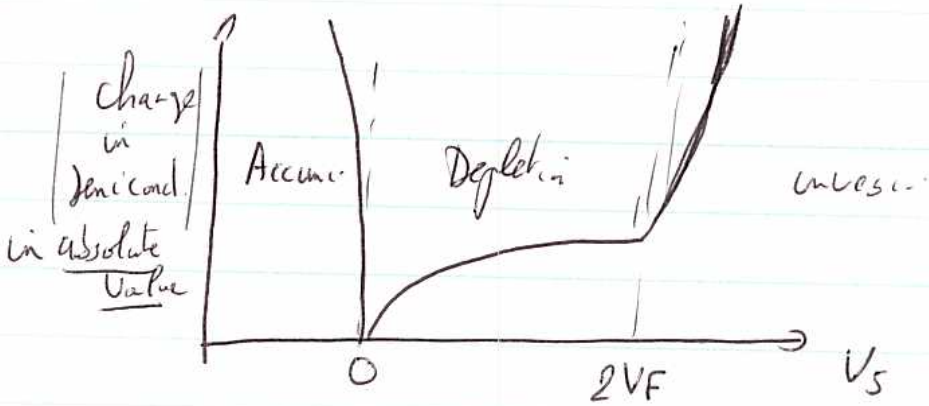
Depletion

$-Q_G = Q_d$

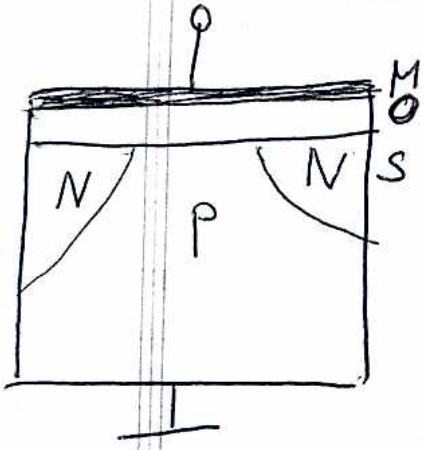


$-Q_G = Q_d + Q_{inv}$

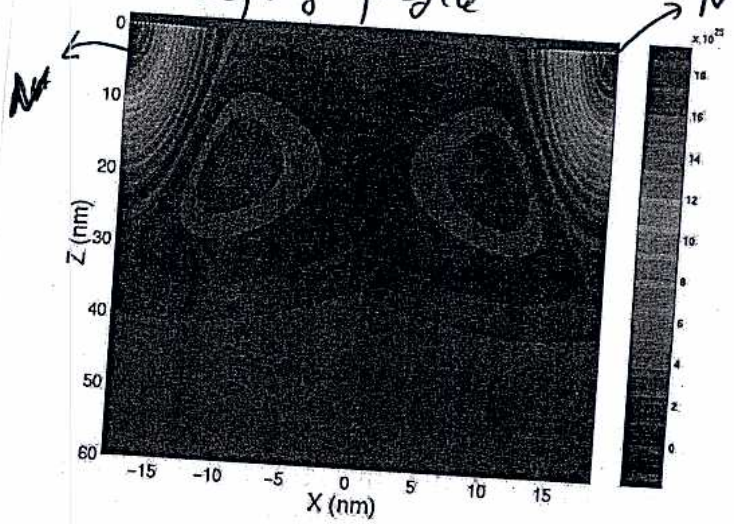




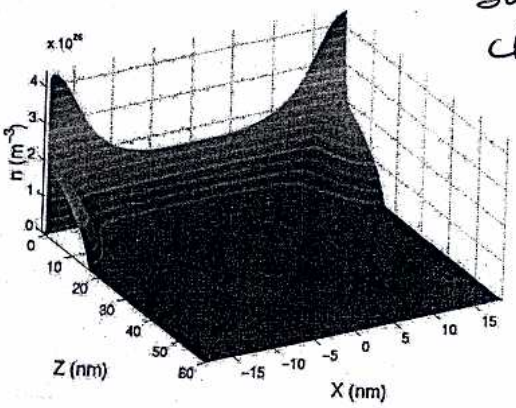
$V_G = 1V$



Doping profile

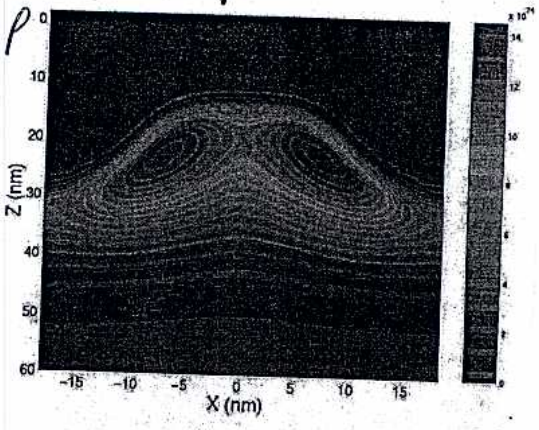


n



Semi-classical

P



U (eV) – Semi-classical.