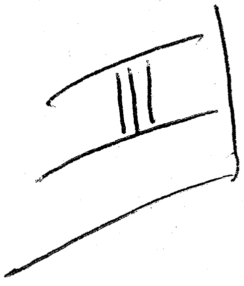


III The MOS Capacitor

MOS = Metal-Oxide-Semiconductor

(or MIS = Metal-Insulator-Semiconductor)

- Most used device in VLSI technology [Si/SiO_2]
- Oxide thickness typically from 5-50 nm
- Oxide is an amorphous material

(1) Structure and Principle of operation

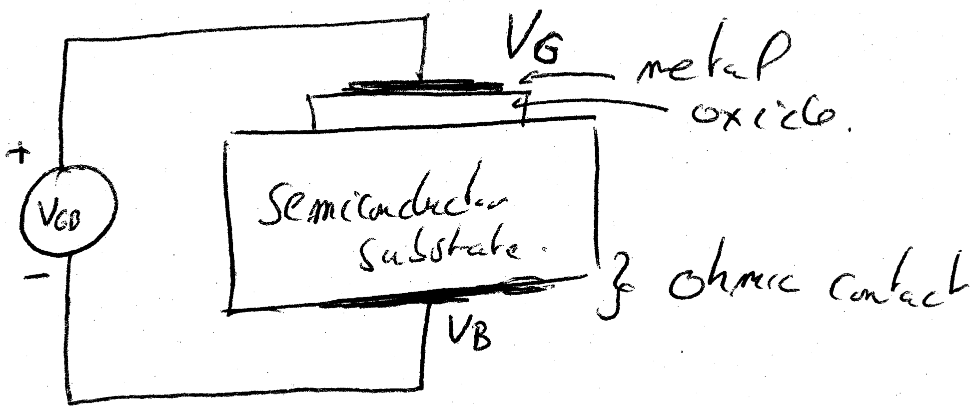


Fig 16.1

De Junction

- For a P-type SC we talk about nMOS capacitor (it is related to the concept of inversion layer)
- For a N-type SC → pMOS capacitor.

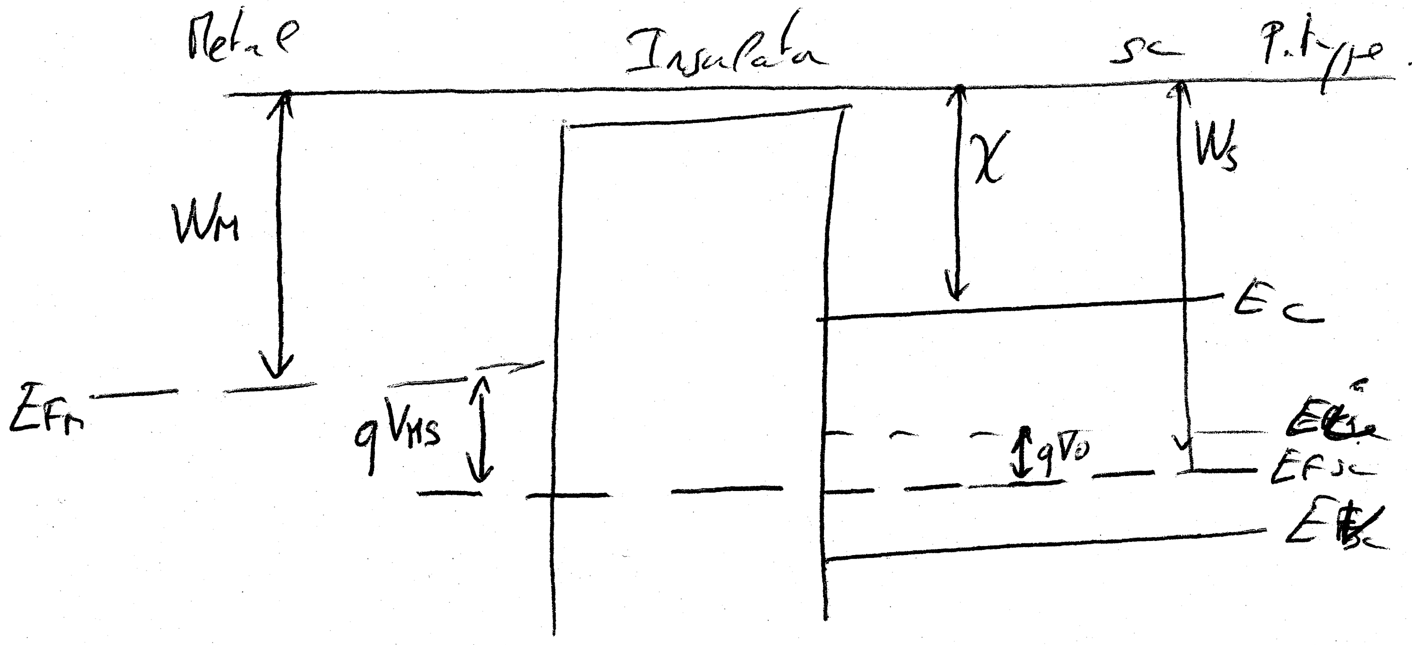
In the following we consider a nMOS capacitor

4 mode of operation

flat-band, accumulation, depletion, inversion.

(a) "Unbiased" junction

the energy band diagram of the sc is flat



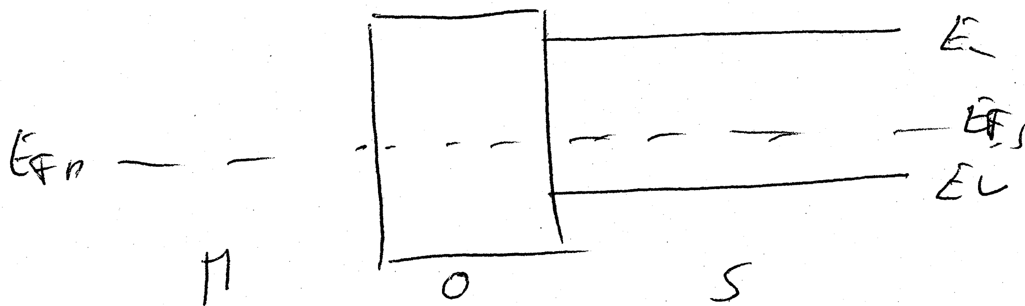
In the ideal case, charge would flow across the insulator so that E_{FM} and E_{FS} would line-up and the difference V_{MS} between metal and sc workfunction would vanish.

$$qV_{MS} = W_M - W_S = W_M - \overbrace{\left(\chi + \frac{E_g}{2} + qV_0\right)}^{\text{p-type sc}} = 0$$

In practice the ideal situation is never achieved (very long lines).

The application of a small bias V_{FB}, is required to line-up the Fermi-level. Its value is given by the non-vanishing V_{MS}.

$\Rightarrow$ we obtain a **flat-band regime**



(3) Biased junction

we consider 3 different regime

$V_G < 0$	$0 < V_G < V_T$	$V_T < V_G$
Accumulation	Depletion	Inversion

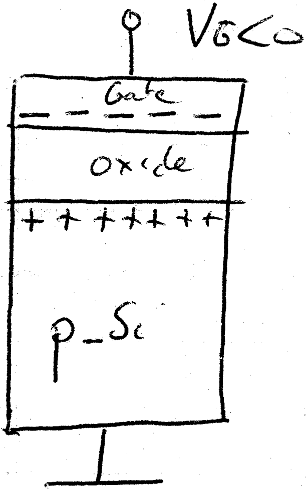
V_T = threshold voltage

V_G = Gate voltage.

The "0" is ~~from~~ relative from the flat-band regime.

Accumulation

$V_G < 0$



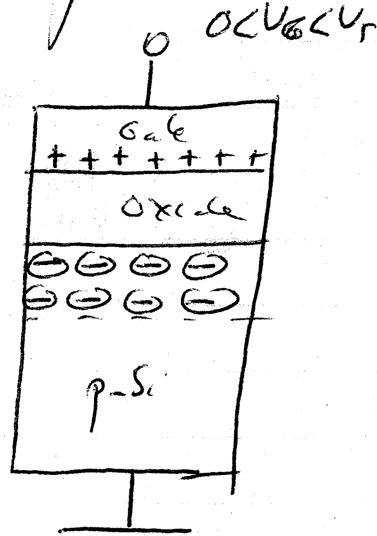
negative charges on the gate attracts holes from the substrate to the interface.

The structure behaves like parallel-plate capacitor.

The hole form an accumulation layer

Depletion

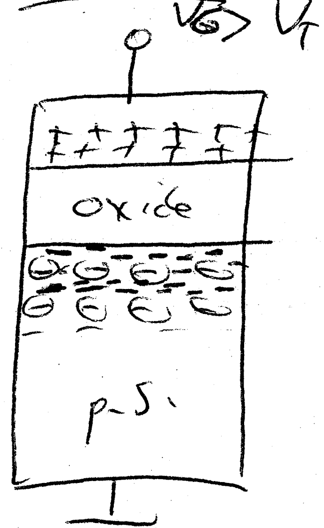
$0 < V_G < V_T$



positive charges on the gate repels the holes from the interface ⇒ creation of a depletion layer containing the ionized acceptors

Inversion

$V_G > V_T$

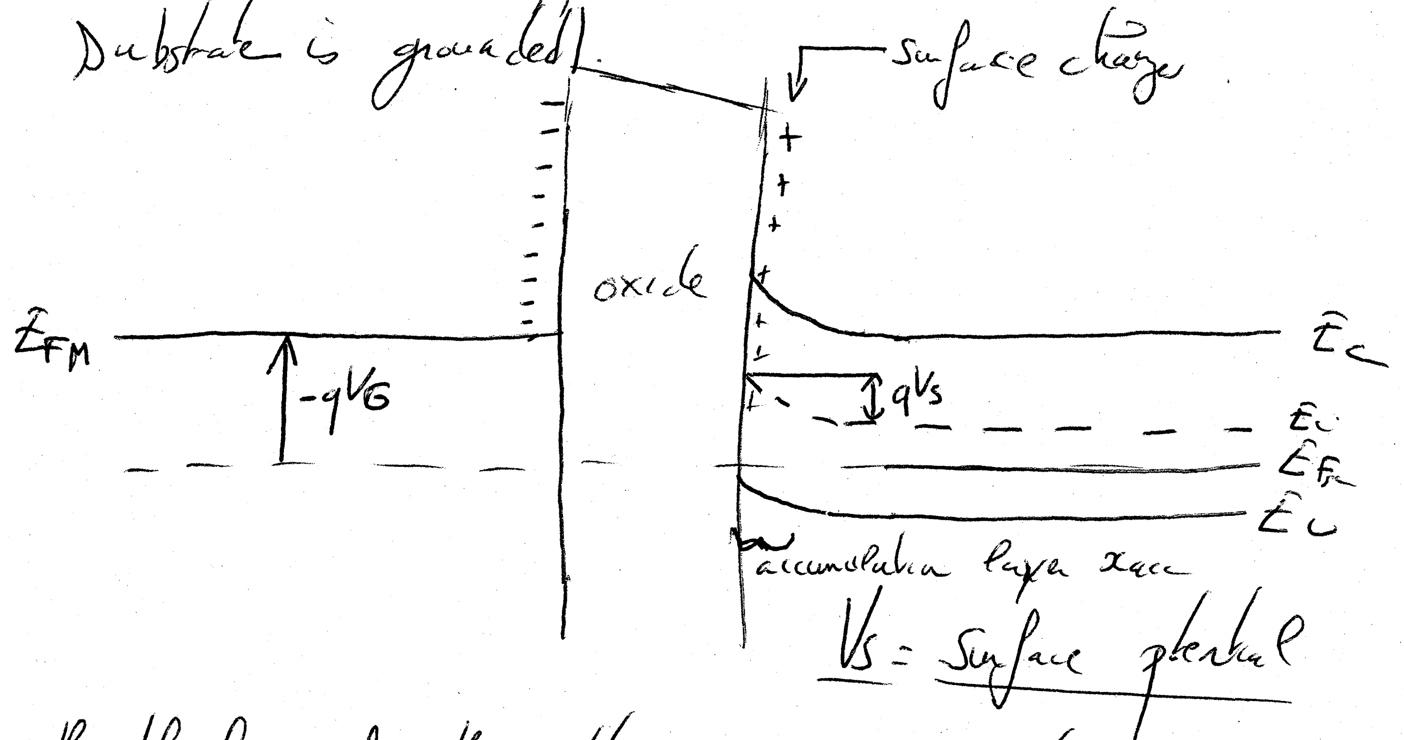


if the potential increases, minority carriers (electrons) will be accumulated at the interface oxide/Si and form the so-called inversion layer

This charge increases exponentially with the surface potential

② Accumulation

a negative bias is applied to the metal gate (the Silicon Substrate is grounded).



The thickness of the obtained accumulation layer is ~ 10nm. Capacitance is

$$C = \frac{\epsilon_{ox}}{t_{ox}}$$

(ϵ_{ox} → permittivity of oxide; t_{ox} → thickness of oxide)

$$\epsilon_{ox} = K_{SiO_2}\,\epsilon_0$$

(ϵ_0 ← vacuum)

In order to derive the thickness ~~of the~~ of the accumulation layer x_{acc}, the electric field and electrostatic potential variation in the semiconductor we need to solve the following equation:

Poisson equation

charge density

$$\frac{d\mathcal{E}}{dx} = \frac{\rho}{\epsilon_{Si}} = \frac{q}{\epsilon_{Si}}(p - n + N_d - N_A) \; ; \quad \mathcal{E} = -\frac{dV}{dx}$$

AGo

$$\begin{cases} p(x) = p_{p0} \exp\left(-\frac{qV}{k_BT}\right) = N_A \exp\left(-q\frac{V(x)}{k_BT}\right) \\ n(x) = n_{p0} \exp\left(\frac{qV}{k_BT}\right) = \frac{n_i^2}{N_A} \exp\left(q\frac{V(x)}{k_BT}\right) \end{cases}$$

$\Rightarrow$ self-consistent problem between p, n, V

Approximation: we suppose that in the hole accumulation layer:

$n \ll p$ and $N_d \ll N_a$. and also we assume $p \gg N_A$.

$$\Rightarrow \quad +\frac{d^2V}{dx^2} \simeq \frac{qN_A}{\epsilon} \exp\left(-q\frac{V(x)}{k_BT}\right)$$

It is a non-linear equation but it is still possible to integrate. After calculation we get:

$$\mathcal{E}^2(x) = \frac{2}{L_D^2}\left|\frac{k_B T}{q}\right|^2 \left[\exp\left(\frac{-qV(x)}{k_B T}\right) - 1\right]$$

with $L_D = \sqrt{\frac{\epsilon k_B T}{q^2 N_A}}$ Debye length

⇒ distance in semiconductor over which local electric field affects the distribution of free carriers. $L_D \searrow$ if concentration $N_A \nearrow$.

we can also get after calculations.

$$V(x) = -\frac{k_B T}{q} \ln\left[\frac{1}{\cos^2\left[\alpha - \frac{x}{\sqrt{2} L_D}\right]}\right]$$

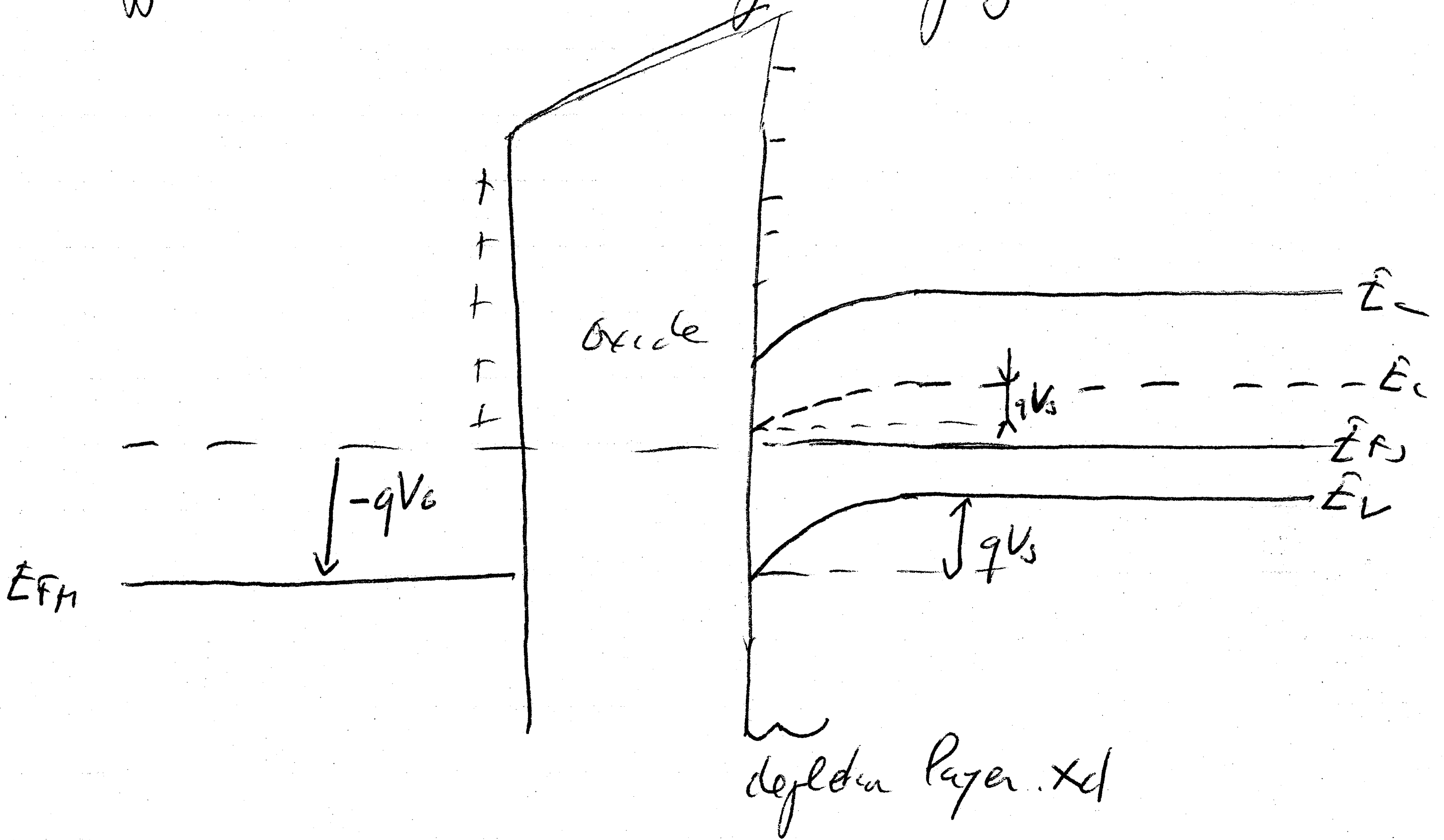
$$\alpha = \cos^{-1}\left(\exp\left(\frac{qV_s}{2 k_B T}\right)\right)$$

$V(x_{acc} = 0) \Rightarrow$
$$x_{acc} = \sqrt{2}\, L_D \cos^{-1}\left(\exp\left(\frac{qV_s}{2 k_B T}\right)\right)$$

V_s (surface potential) is in practice very small, even for large $V_G \Rightarrow x_{acc}$ is small; since $p(x)$ increase exponentially in function of potential, $p(x)$ increases rapidly close to surface.

3) Depletion

a small positive voltage is applied to the gate $V_G > 0$.
holes are repelled by the gate and a negative charge appears due to the acceptor doping atoms.



the potential in the depletion region is solution of the Poisson equation.

$$\frac{d^2V(x)}{dx^2} \simeq q\frac{N_A}{\varepsilon_{Si}}$$

(using the depletion approximation $p \ll N_A$)

the Boundary conditions are $V(x_d) = 0$ $\left.\frac{dV(x)}{dx}\right|_{x_d} = 0$

$$\Rightarrow \boxed{V(x) = \frac{qN_A}{2\epsilon_{si}}(x - x_d)^2}$$

surface potential is $\boxed{V_s = V(x=0) = \frac{qN_A}{2\epsilon_{si}} x_d^2}$

$$\Rightarrow \boxed{x_d = \sqrt{\frac{2\epsilon V_s}{qN_A}}}$$

* the depletion charge between $0 \leq x \leq x_d$ is equal to $\boxed{Q_d = -qN_A x_d = -\sqrt{2q\epsilon_{si} N_A V_s}}$

the depletion capacitance is then

$$\Rightarrow \boxed{C_D = \frac{\epsilon_{si}}{x_d} = \frac{d|Q_D|}{dV_s}}$$

* the gate voltage V_G is also equal to

$$\boxed{V_G = V_s + V_{ox} = V_s - \frac{Q_d}{C_{ox}}}$$ $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$

(V_{ox}: potential drop in the oxide.)

$$\boxed{Q_G = -Q_d}$$

the capacitance of the structure is:

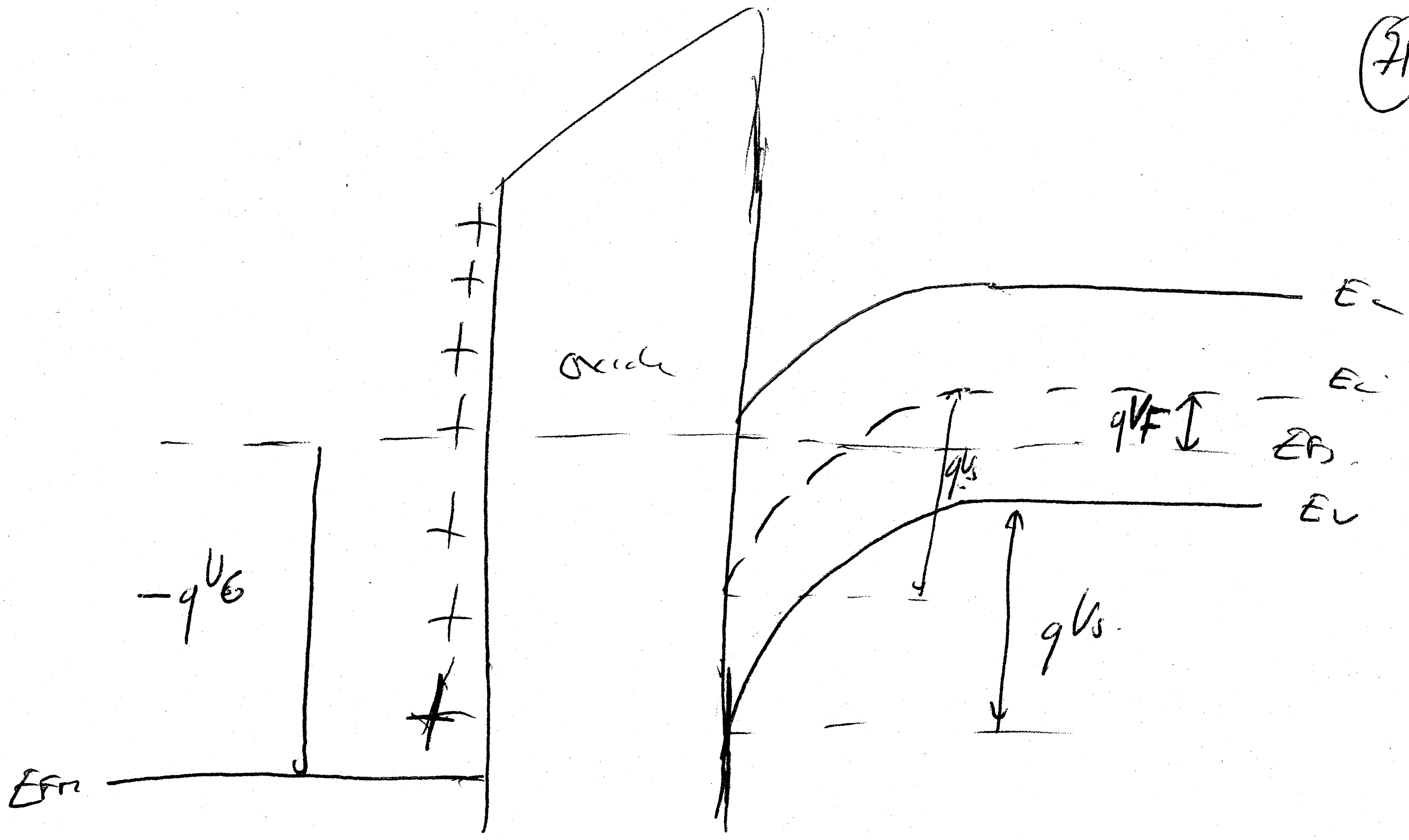
$$C = \frac{dQ_G}{dV_G} = -\frac{dQ_D}{dV_G} = \frac{-dQ_d}{d\left(-\frac{Q_d}{C_{ox}} + V_s\right)} = \frac{-dQ_d/dV_s}{d\left(-\frac{Q_d}{C_{ox}} + V_s\right)/dV_s}$$

$$\Rightarrow \boxed{C = \frac{C_D C_{ox}}{C_D + C_{ox}} = \frac{1}{\frac{1}{C_{ox}} + \frac{1}{C_D}}}$$

④ <u>Inversion</u>: if a larger positive voltage is applied the surface potential V_s will continue to increase according to the relations.

$$\begin{cases} p(x=0) = N_A \exp\left(\frac{-qV_s}{k_BT}\right) & \text{minority concen.} \\ n(x=0) = \frac{n_i^2}{N_A} \exp\left(\frac{qV_s}{k_BT}\right) & \text{majority concen.} \end{cases}$$

$\underline{\underline{p \searrow}}$ and $\underline{\underline{n \nearrow}}$ at the surface.



Let us study 2 limiting cases:

(i) * if surface concentration of e^- and h^+ are equal.

$$n(0) = p(0) = n_i \Rightarrow \text{if } (E_i == E_F) \text{ at } x = 0.$$

$$\Rightarrow \boxed{qV_s = qV_F = k_BT \ln\left(\frac{N_A}{n_i}\right)}$$

$n(0) = p(0)$ gives also the following relation.

$$N_A \exp\left(-\frac{qV_F}{k_BT}\right) = \frac{n_i^2}{N_A} \exp\left(\frac{qV_F}{k_BT}\right) \quad (*)$$

(ii) If V_G increases further.

$n(0)$ becomes equal to $p_{p0} = N_A$ which is the original concentration of holes (majority carriers) in the Silicon.

$n(0) = N_A$.

$$\Rightarrow \quad N_A = \frac{n_i^2}{N_A} \exp\left(\frac{qV_s}{k_BT}\right) \quad * \exp\left(\frac{-qV_F}{k_BT}\right)$$

$$N_A \exp\left(\frac{-qV_F}{k_BT}\right) = \frac{n_i^2}{N_A} \exp\left(q\frac{V_s - V_F}{k_BT}\right)$$

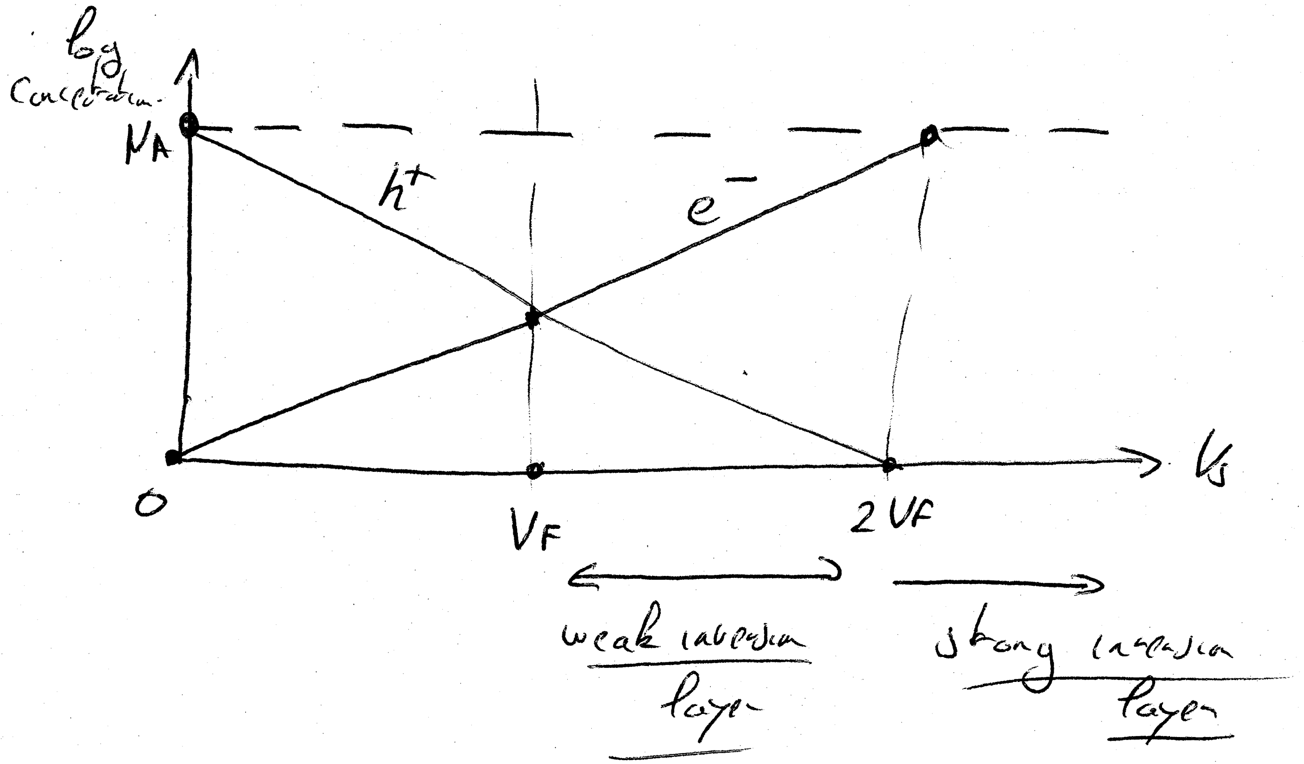
using (*)

$$\frac{n_i^2}{N_A} \exp\left(q\frac{V_F}{k_BT}\right)$$

$$\Rightarrow \quad V_s - V_F = V_F \Rightarrow \boxed{V_s = 2V_F}$$

$(\Rightarrow n(0) = N_A)$

<u>Summary</u> finally we get



- The inversion layer is rich in electrons, and therefore, it is a good conductor.
- When an inversion layer is formed $\bar{e}$ are locally majority carriers at the surface. The thickness of the inversion layer remains very small if V_G increases. The $\bar{e}$ charge can be considered as surface charge and depends exponentially of the surface potential:

* The MOS capacitor consists then of two conducting electrodes, the metal gate and the inversion layer. As in the case of accumulation, the capacitance of the MOS is equal to C_{ox}.

In the inversion region,

the depth of the depletion region is given by.

$$x_{dmax} = \sqrt{\frac{4 \epsilon V_F}{q N_A}}$$

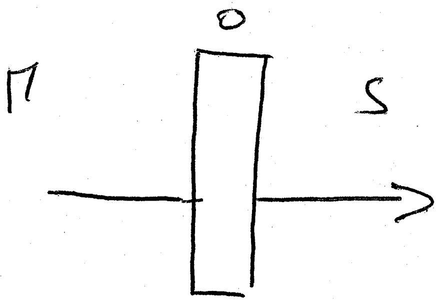
since if $V_G \uparrow$, V_s increases only slightly above $2V_F$.

~~(5) Threshold voltage~~

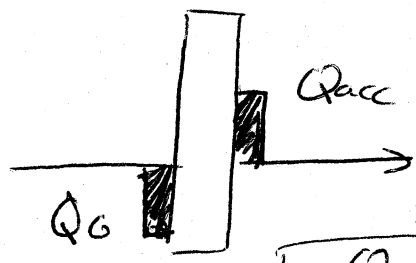
~~it is the voltage V_G that must be applied to form an inversion layer.~~

5 Charges in the MOS structure

Flat_band



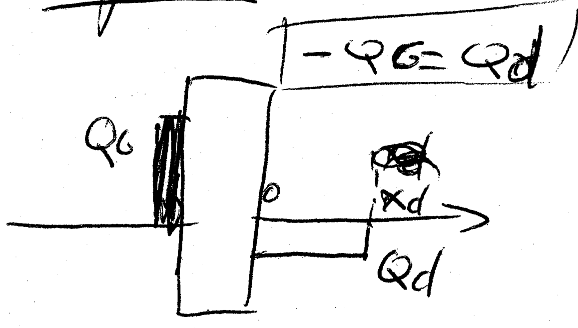
Accumulation



$-Q_G = Q_{acc}$

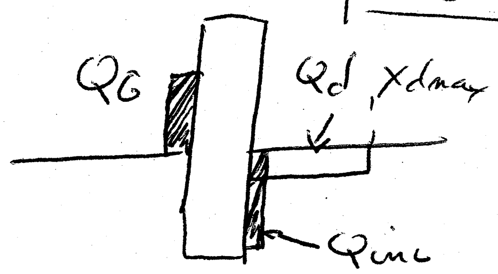
Depletion

$-Q_G = Q_d$

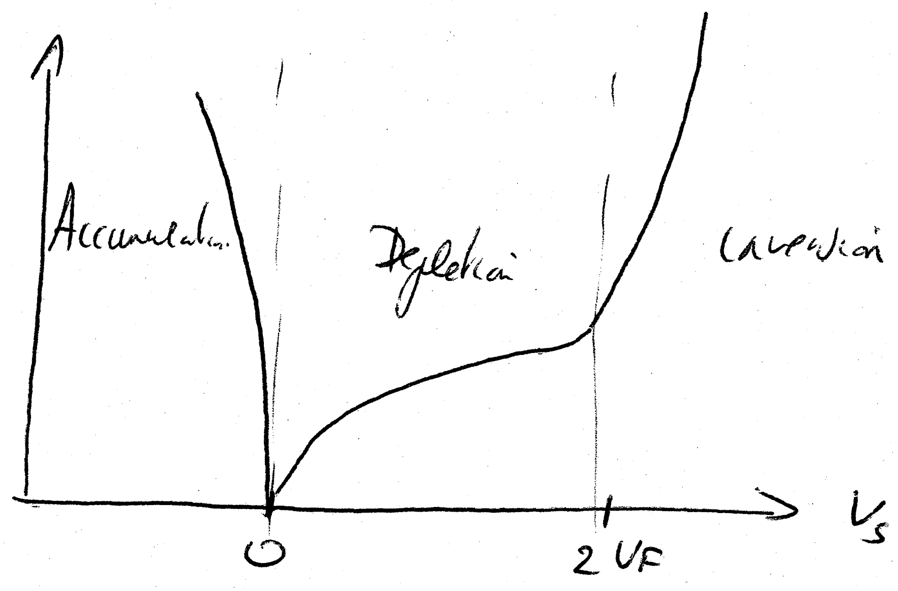


Inversion

$-Q_G = Q_d + Q_{inv}$



|Charge in semiconductor| in absolute value.



6 Threshold voltage

It is the voltage V_G that must be applied at the gate to form an inversion layer.

We know that $V_G = V_S + V_{ox}$ $\qquad V_{ox} = \frac{Q_G}{C_{ox}}$

Q_G is the positive charge of the gate electrode.

In practice, the flat-band voltage must be added for "non ideal" threshold voltage.

$$V_G = V_{FB} + V_S + \frac{Q_G}{C_{ox}}$$

Let us consider $Q_G = -(Q_d + Q_{inv})$

with $Q_d = -qN_A x_d = -\sqrt{2q\epsilon N_A V_S}$

if $0 \leq V_s \leq 2V_F$

Depletion regime $Q_{inv} \simeq 0$

$$V_G = V_{FB} + V_s + \frac{\sqrt{2\epsilon_{si} q N_A V_s}}{C_{ox}}$$

if $V_s > 2V_F$

Inversion regime $Q_{inv} \neq 0$

$$V_G = V_{FB} + V_s + \frac{\sqrt{2\epsilon q N_A V_s}}{C_{ox}} - \frac{Q_{inv}}{C_{ox}}$$

at $V_s = 2V_F$

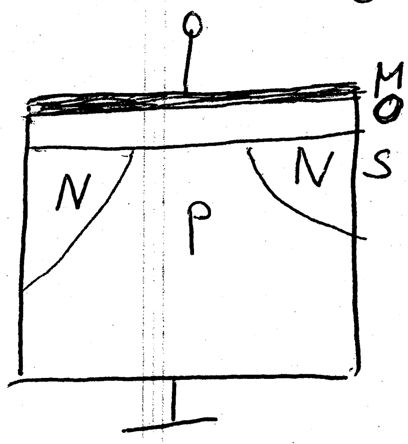
$\Downarrow$

$V_G = V_T$ threshold voltage.

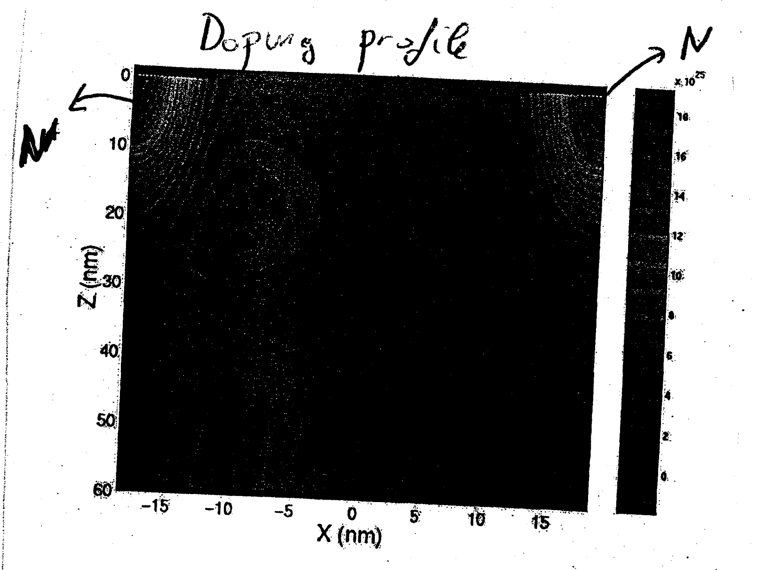
$$\Rightarrow \boxed{V_T = V_{FB} + 2V_F + \frac{\sqrt{4\epsilon q N_A V_F}}{C_{ox}}}$$

equivalent to 17.1a in the book

$V_G = 1V$

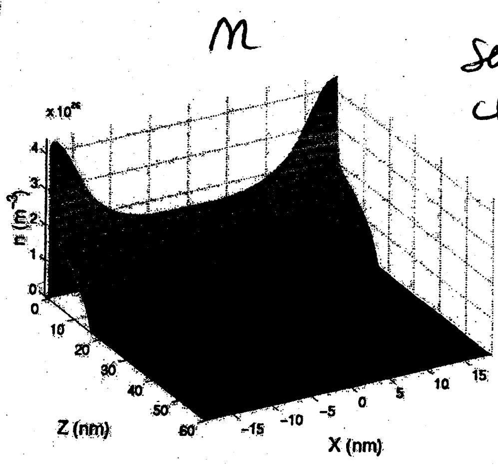


Doping profile

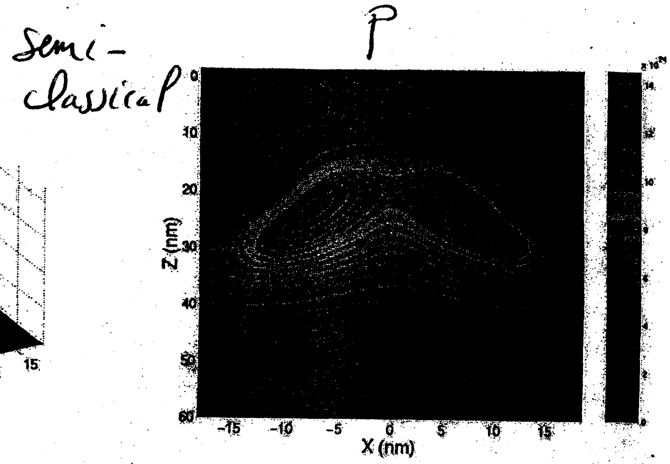


Semi-classical

n



p



U (eV) - Semi-classical