V.I.A.

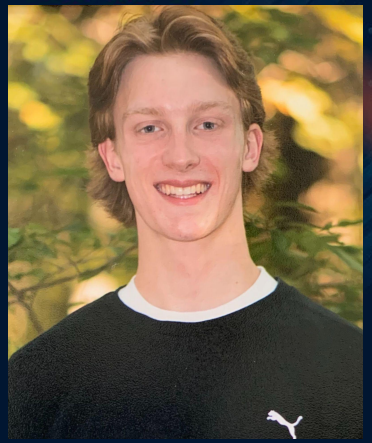
Visually Integrated Assistant

Meet the team

Antonio Romanoski Neto
Electrical Engineering

Lucas Georg Guertin
Electrical Engineering

Kevin Alfred Bardhi
Electrical Engineering



Jared Louis Simmons
Electrical Engineering

Problem Statement

Modern advancements in voice and eye control of computers allow for more accessibility options for individuals with disabilities.

Voice control options are the most common way for increasing accessibility options for users

Eye control options are limited to systems that depend on an expensive investment into specific equipment and control capabilities are limited to one’s own computer.

Project Goal

To design and create a cyber physical system that utilizes human eye movement as an input, and allows the user to control different connected devices wirelessly within a given closed environment.

Proposed CDR Deliverables from MDR

- Configure GUI to write 32 bit strings to serial port
- Configure Peripheral Board to parse Bluetooth messages up to 32 bits using an extra 16 bits for delimiters “{“ and “}” for a total of 54 bits of information
- Add 2 way communication for feedback capabilities

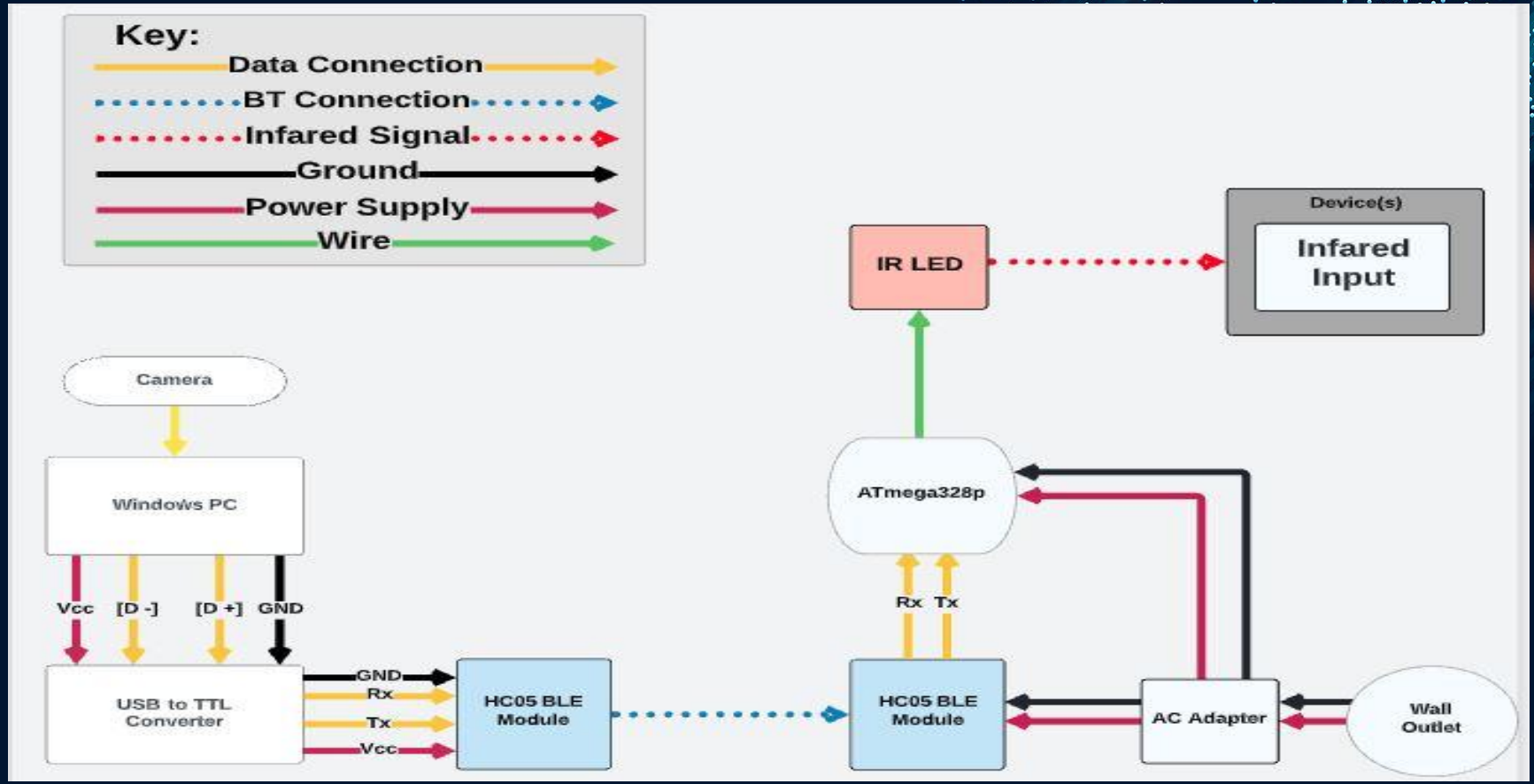
Actual CDR Deliverables/Current Progress

- We optimized hardware usage in our PCB design
- Decreased transmission time from 7s ~ 4s on average
- We were able to remove all Arduino hardware
- We have our first revision PCB designed and ordered with other revisions already being made
- We added a Roku tv to our list of controllable devices and can fully operate the tv using eye movement

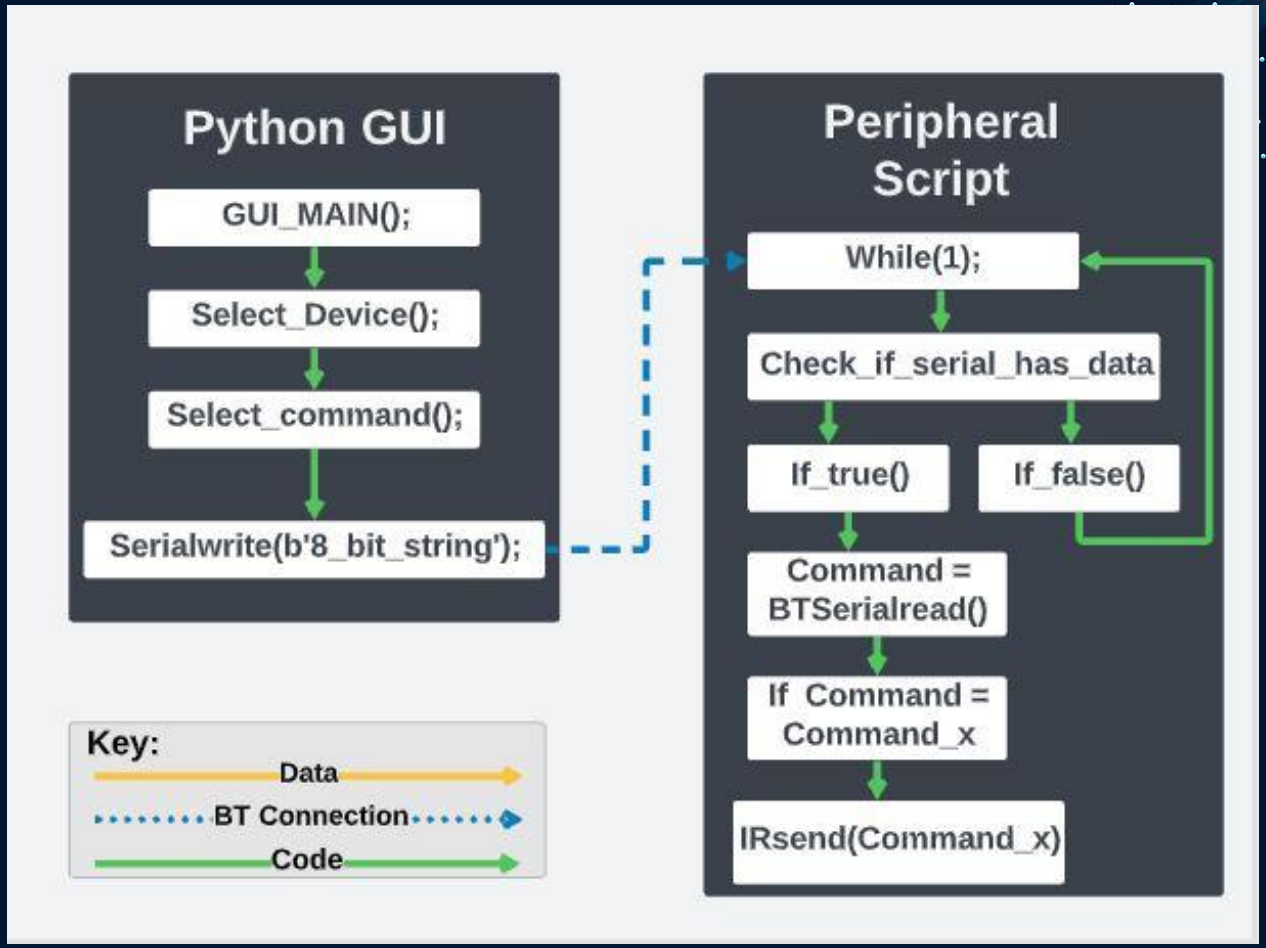
Noticeable Changes in design since MDR

- We are no longer making use of our previous Main Board's capabilities, we will now only make use of the FT232RL PCB and the Peripheral PCB
  - The hc-05 takes UART logic as input, our designed TTL converter uses UART as an output, making main board obsolete
  - We can handle all data processing on Peripheral

Current Hardware Block Diagram



Current Software Block Diagram

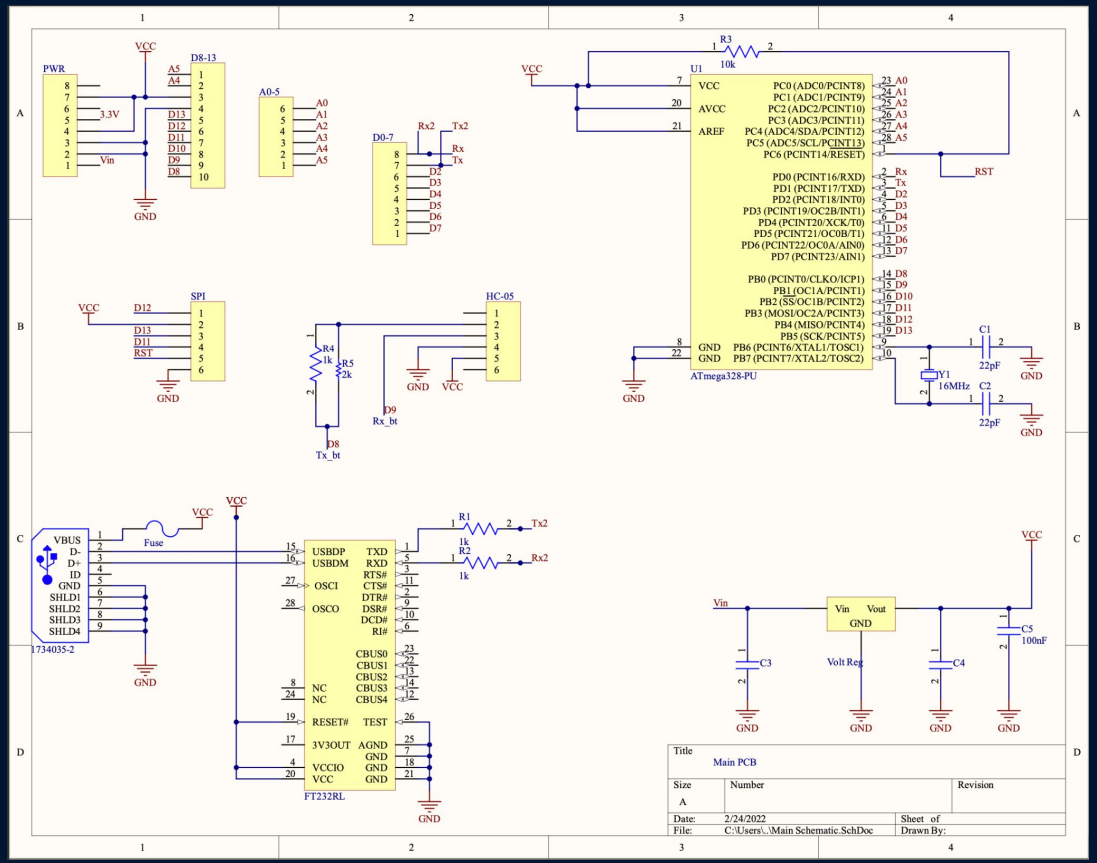


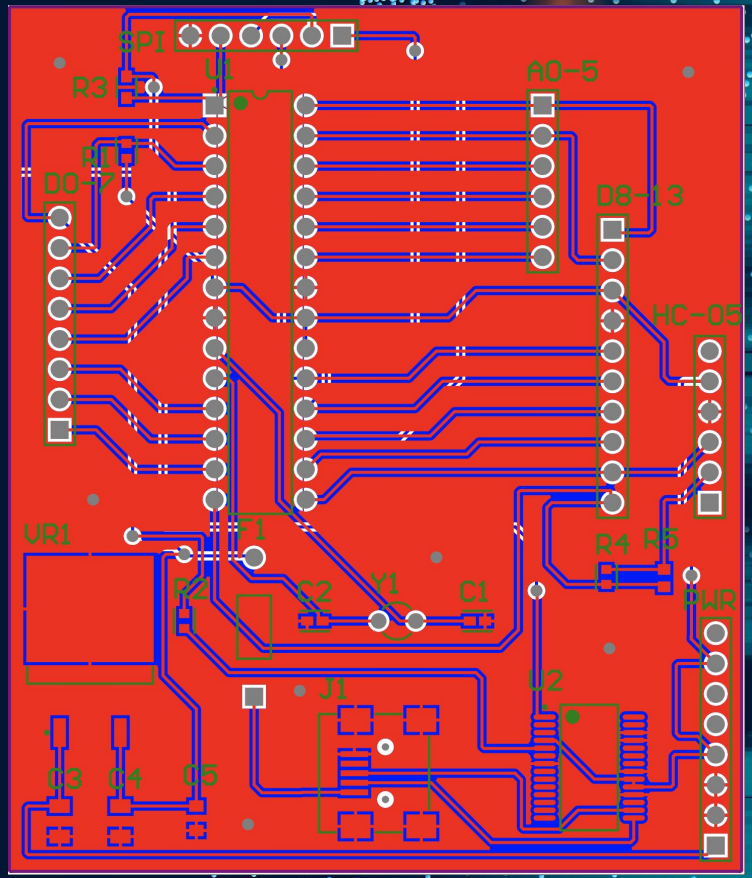
Challenges/Lessons Learned

- Challenges faced
  - Importing/interacting libraries into AVR C
  - Designing PCBs for the first time
    - Size of PCB
    - Size of components
    - Traces
    - Revisions
  - Global chip shortage
  - Over-engineering
- Lessons learned
  - Order components needed months in advance, not just weeks
  - Time management
  - Resource allocation

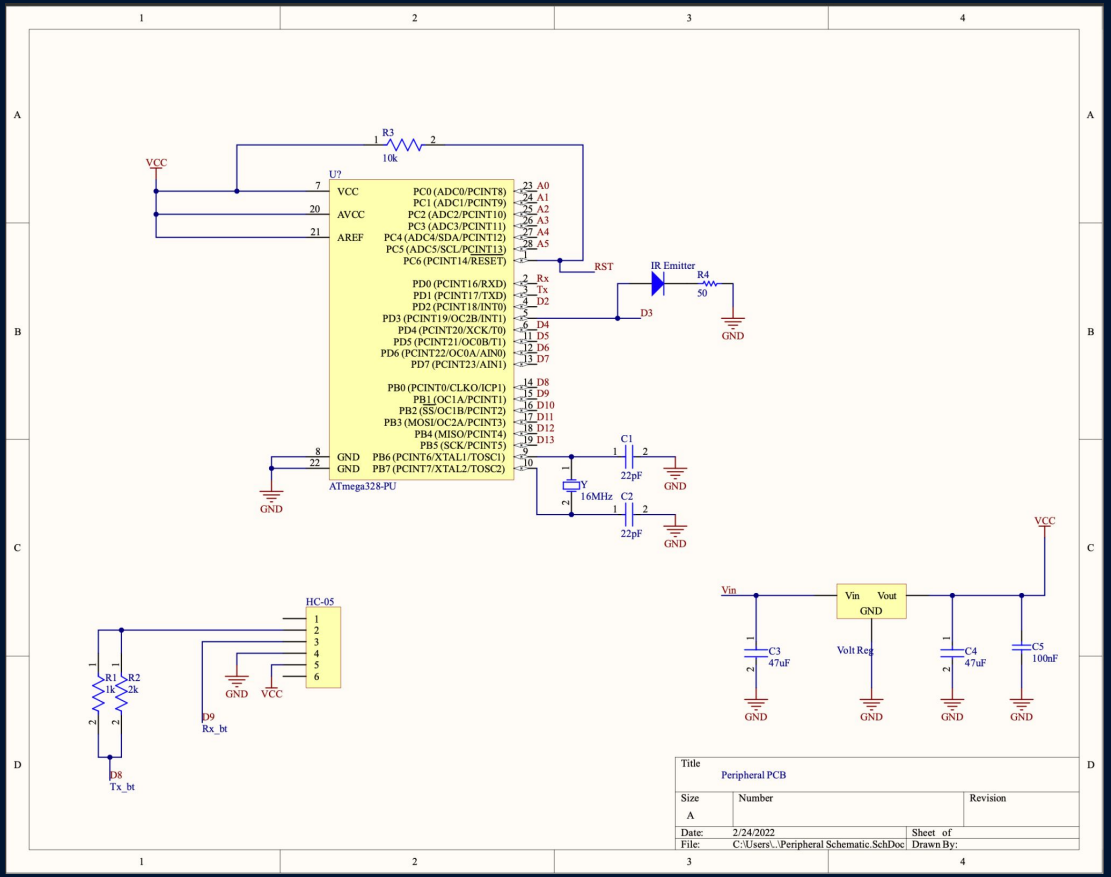
Live Demonstration

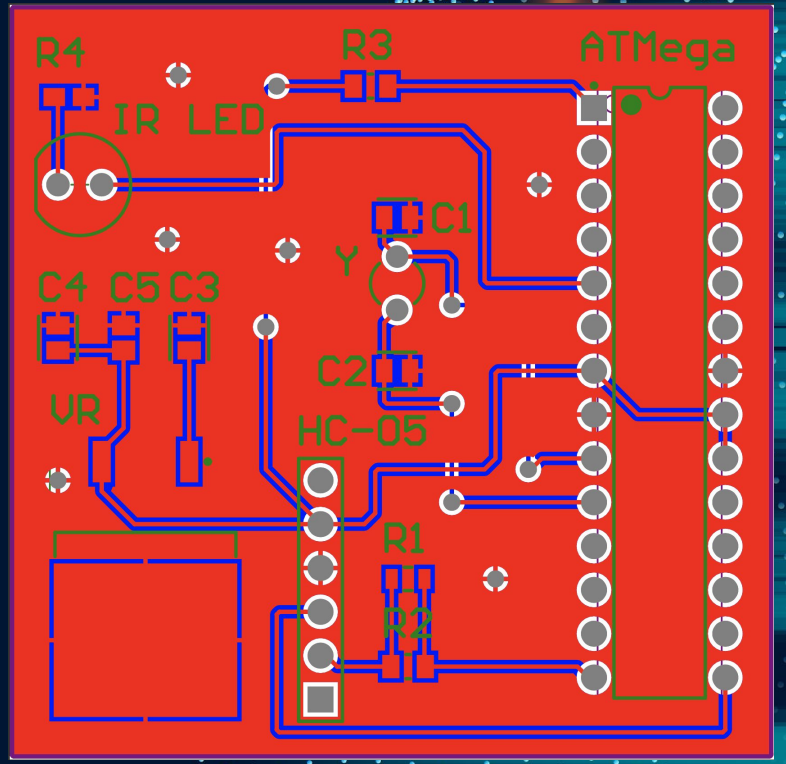
Main PCB


PWR
VCC
3.3V
Vin
GND
A5
A4
D8-13
D13
D12
D11
D10
D9
D8
A0-5
A0
A1
A2
A3
A4
A5
D0-7
Rx2
Tx2
Rx
Tx
D2
D3
D4
D5
D6
D7
R3
10k
U1
VCC
AVCC
AREF
PC0 (ADC0/PCINT8)
PC1 (ADC1/PCINT9)
PC2 (ADC2/PCINT10)
PC3 (ADC3/PCINT11)
PC4 (ADC4/SDA/PCINT12)
PC5 (ADC5/SCL/PCINT13)
PC6 (PCINT14/RESET)
RST
PD0 (PCINT16/RXD)
PD1 (PCINT17/TXD)
PD2 (PCINT18/INT0)
PD3 (PCINT19/OC2B/INT1)
PD4 (PCINT20/XCK/T0)
PD5 (PCINT21/OC0B/T1)
PD6 (PCINT22/OC0A/AIN0)
PD7 (PCINT23/AIN1)
PB0 (PCINT0/CLKO/ICP1)
PB1 (OC1A/PCINT1)
PB2 (SS/OC1B/PCINT2)
PB3 (MOSI/OC2A/PCINT3)
PB4 (MISO/PCINT4)
PB5 (SCK/PCINT5)
PB6 (PCINT6/XTAL1/TOSC1)
PB7 (PCINT7/XTAL2/TOSC2)
ATmega328-PU
C1
22pF
Y1
16MHz
C2
22pF
SPI
D12
D13
D11
RST
HC-05
R4
1k
R5
2k
D9
Rx_bt
D8
Tx_bt
VBUS
D-
D+
ID
GND
SHLD1
SHLD2
SHLD3
SHLD4
1734035-2
Fuse
USBDP
USBDM
OSCI
OSCO
TXD
RXD
RTS#
CTS#
DTR#
DSR#
DCD#
RI#
CBUS0
CBUS1
CBUS2
CBUS3
CBUS4
RESET#
TEST
3V3OUT
AGND
VCCIO
NC
FT232RL
R1
1k
R2
1k
Tx2
Rx2
Vin
Vout
Volt Reg
C3
C4
C5
100nF
Title
Main PCB
Size
A
Number
Revision
Date:
2/24/2022
File:
C:\Users\..\Main Schematic.SchDoc
Sheet of
Drawn By:

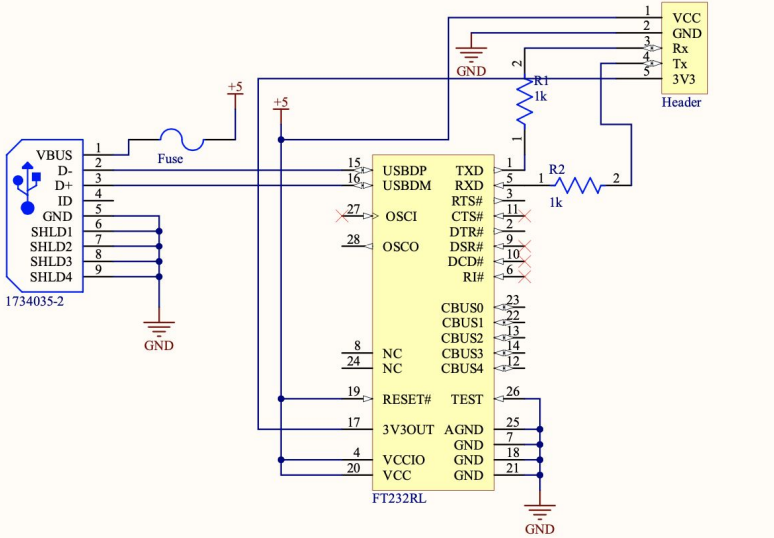

SPI
R3
U1
A0-5
D0-7
D8-13
HC-05
VR1
F1
R4
R5
R2
C2
Y1
C1
PWR
J1
U2
C3
C4
C5

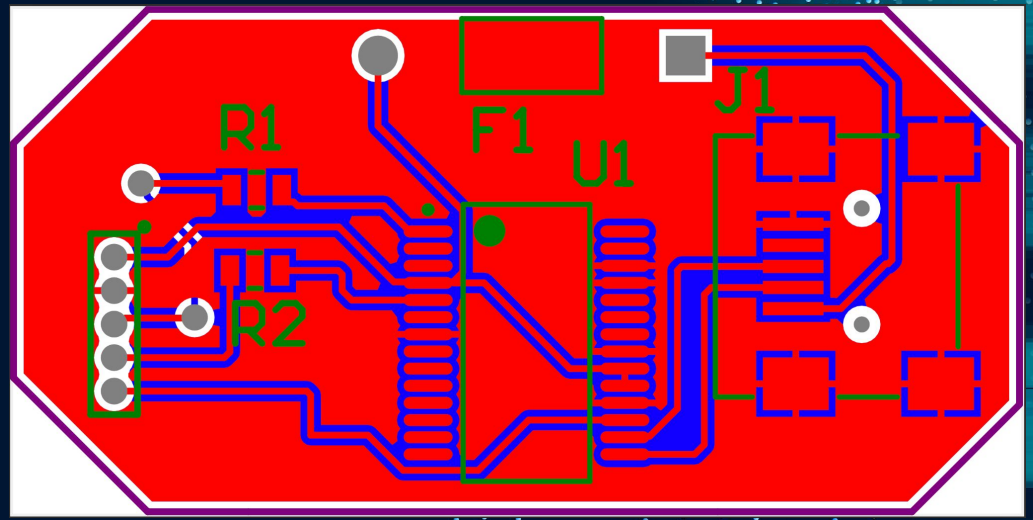
Peripheral PCB





FT232RL PCB


VCC
GND
Rx
Tx
3V3
Header
R1
1k
R2
1k
Fuse
+5
GND
VBUS
D-
D+
ID
GND
SHLD1
SHLD2
SHLD3
SHLD4
1734035-2
USBDP
USBDM
OSCI
OSCO
NC
NC
RESET#
3V3OUT
VCCIO
VCC
TXD
RXD
RTS#
CTS#
DTR#
DSR#
DCD#
RI#
CBUS0
CBUS1
CBUS2
CBUS3
CBUS4
TEST
AGND
GND
FT232RL


R1
F1
U1
J1
R2

PCB Components

Peripheral PCB

- R1: 1k ohms, 0805
- R2: 1k ohms, 0805
- R3: 10k ohms, 0805
- R4: 50 ohms, 0805
- C1: 22pF, 0805
- C2: 22pF, 0805
- C3: 47uF, 0805
- C4: 47uF, 0805
- C5: 100nF, 0805
- Y: 16MHz Crystal Oscillator
- IR Emitter
- VR: Voltage Regulator

FT232RL PCB:

- R1: 1k ohms, 0805
- R2: 2k ohms, 0805
- F1: Fuse
- J1: 1734035-2 USB port, USB2.0 MINI
- U1: FT232RL

Previous PCB Plan for CDR/FPR

- Main Board
  - Components
    - HC-05 Bluetooth module
    - Infrared Receiver
    - Atmega328p
    - External Crystal oscillator
- Peripheral Board
  - Components
    - HC-05 Bluetooth module
    - Infrared Transmitter
    - Power Relay
    - Atmega328p
    - External Crystal oscillator

PCB Improvements for FPR

- Main board is no longer needed
- **Peripheral Board**
  - Make PCB bigger, to have more space to solder components accurately
  - Fix traces to not have any interference
  - Fix incorrect placing of components
- **FT232RL**
  - Make PCB bigger, to have more space to solder components accurately
  - Make header more spaced out
    - Can not be accessed right now without interference

FPR Goals

- Improvements to PCBs as mentioned previously
- Improve GUI
  - Functionality
  - Accessibility
  - Aesthetic Improvement
- Improve Eye Tracking
  - Better Calibration
  - Start with minimal input from user
- Hardware Reliability
  - Consistently
  - Stress Test
  - Backup Plan

Timeline

- **Within Two Weeks**: Complete Software Development in AVR C
- **End of March:** PCB Revisions Completed and Website created once domain has been specified
- **1st Week of April:** GUI and Eye Tracking stress tested and PyGaze and or Gazepointer fully implemented
- **2nd Week of April:** Finalized Hardware for showcase tested and ready for FDR
- **3rd Week of April:** Optimization and Aesthetic improvement

Expenditures

Total Expenditure for CDR	Cost	Amount	Total Price
MDR Expenditures	112	1	112
Expenditures for research and development	90	1	90
PCB	91	1	91
Atmega-PU	21.26	2	42.52
500 mA Fuse	7.19	1	7.19
Adafruit RFM95W LoRa Transceiver	19.95	2	39.9
Shipping	9.03	1	9.03
PCB Revisions	100	1	100
Total			491.64