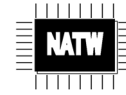


# Advance Program

## 12th IEEE North Atlantic Test Workshop, NATW 2003



May 15-16, 2003  
Gurney's Inn at the Sea  
Montauk, New York, USA  
<http://www.ecs.umass.edu/natw>



### Thursday, May 15

**7:00 - 8:10** Breakfast

**8:10 - 8:20** Opening Greeting

Ian G. Harris, Michael Bushnell, Peilin Song

**8:20 - 9:20** Invited Presentation

"Fault Modeling and ATPG for Nanometer Technologies", Sanjay Sengupta, Principal Engineer, Mobile Processors Group, Intel Corp.

**9:20 - 10:35** Session 1: Defect Oriented Testing/Cross Talk Noise Testing

Session Chair: R. Dean Adams - PDATech, Inc.

1. "Realistic N-Detect Analysis", R.D. Blanton, K.N. Dwarakanath\*, A. B. Shah - Carnegie Mellon Univ.
2. "Detection of Crosstalk Faults in Deep Sub-Micron Chips Using Stuck-At Fault Tests and Tools", H. Hashempour\* and F. Lombardi - Northeastern Univ.
3. "An Encoding Scheme for Instruction, Data and Address in a Multi-GHz Processor for Concurrent Cross-talk Fault Detection", N. Venkateswaran\*, V. Balaji, V. Mahalingam and T. L. Rajaprabhu - Waran Research Foundation, India

**10:35 - 11:00** Coffee Break

**11:00 - 12:15** Session 2: Testability Analysis

Session Chair: James Monzel - IBM Corp.

1. "Fault Collapsing via Functional Dominance", V. D. Agrawal\*, - Rutgers Univ., A. V. S. S. Prasad, and M. V. Atre, - Agere Systems, India
2. "A Survey on Testability Measurements at Various Abstraction Levels", N. Karimi, - Univ. of Tehran, Iran, P. A. Riahi\* and Z. Navabi - Northeastern Univ.
3. "Theorems on Redundancy Identification", V. J. Mehta\*, V. D. Agrawal, M. L. Bushnell - Rutgers Univ.

**12:15 - 13:45** Lunch

**13:45 - 15:25** Session 3: Analog/Mixed Signal Testing

Session Chair: Shianling Wu - SynTest Technologies, Inc.

1. "Reducing Overall Cost for RF Transceivers through Enhanced Wafer-level Testing", S. Ozev\* - Duke Univ., Christian Olgaard - LitePoint Corp.
2. "How to Reduce Aliasing in Analog Testing", Z. Guo\* - NJIT
3. "Long Term Jitter Measurement for PLL", T. Xia\* and J.C. Lo - Univ. of Rhode Island
4. "A Novel Integrated Approach for Low Power Testing and Fault Tolerance in Analog to Digital Converters", N. Venkateswaran\*, S. P.B, M. Mani, S. M. Prabhu, K. Bharath, Annamalai. S. - Waran Research Foundation, India

**15:25 - 15:50** Coffee Break

**15:50 - 18:30** Social Event/Free Time: Tour to the Historical Lighthouse

**18:30 - 20:30** Dinner Award Presentations, Announcements, Open Floor NATW Committee Meeting

\* - presenter

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### Friday, May 16

**7:10 - 8:00** Breakfast

**8:00 - 9:00** Keynote Presentation

"IEEE P1500: An upcoming standard to test embedded cores in SOCs", Sudipta Bhawmik, Ph.D, SoC Design, Verification and DFT, Agere Systems

**9:00 - 10:15** Session 4: Resource Partition/Design for Test

Session Chair: Jose T. de Sousa - IST/INESC-ID, Portugal

1. "Global Test Resource Partitioning for Mixed-Signal SOCs", S. Ozev\* and K. Chakrabarty - Duke Univ.
2. "A New Distributed Test Control Architecture with Multihop Wireless Test Connectivity for GigaHertz System-Chips", D. Zhao\*, S. Upadhyaya, - SUNY Buffalo and M. Margala - Univ. of Rochester
3. "Testability Features of the Alpha 21364 Microprocessor", S. Erlanger\*, D. Bhavar, - Intel, R. Davies, - HP

**10:15 - 10:45** Coffee Break

**10:45 - 12:25** Session 5: Design Validation/Fault Tolerant

Session Chair: Jien-Chung Lo - Univ. of Rhode Island

1. "A Deterministic Globally-Asynchronous Locally-Synchronous Methodology for Validation, Debug and Test", M. Heath and I. Harris\* - Umass Amherst
2. "Timing Validation of LSSD Design Using PICA", P. Song\*, A. J. Weger, M. K. McManus, - IBM T.J. Watson Research Center, Yorktown Heights, NY, USA
3. "Re-Computing using Ruptured Dependences: A Low-cost Low-latency Register Transfer Level Approach to Fault-Secure Datapaths", K. Wu\*, R. Karri - Polytechnic Univ.
4. "Towards a Strongly Fault Tolerant VLSI Processor Array", S. P. Bahukudumbi\*, Srivatsan P. - Sri Venkateswara College of Engineering, India.

**12:25 - 13:45** Lunch

**13:45 - 15:25** Session 6: Fault Simulation/Delay Testing

Session Chair: Martin Margala - U. Rochester

1. "Fault Simulation using Partial Reconfiguration of Field Programmable Gate Arrays", A. Parreira, J.P. Teixeira, M.B. Santos, and J.T. de Sousa\* - IST/INESC-ID, Portugal
2. "A VPI-based IP Core Serial Fault Simulation and Test Generation Methodology", P. A. Riahi\*, Z. Navabi, F. Lombardi - Northeastern Univ.
3. "Can Signal Integrity Faults Be Detected by Delay Testes?", V. H.-W. Meyer\*, A. K. Palit, W. Anheier, - Univ. of Bremen, Germany, A. Sticht and J. Schloeffel, - Phillips Semiconductors, Hamburg, Germany
4. "Bridge, Single Stuck & Multiple Stuck Fault Coverage Analysis in EDAC Encoded FSM", N. Venkateswaran\*, V. Balaji, V. Mahalingam, T. L. Rajaprabhu - Waran Research Foundation, India

\* - presenter