Silicon single-electron quantum-dot transistor switch operating at room temperature

Lei Zhuang,[a] Lingjie Guo, and Stephen Y. Chou[b]
Department of Electrical Engineering, NanoStructure Laboratory, University of Minnesota, Minnesota 55455 and Princeton University, New Jersey 08544

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We fabricated a silicon single-electron quantum-dot transistor, which showed drain current oscillations at room temperature. These oscillations are attributed to electron tunneling through a single silicon quantum dot inside a narrow wire channel. Analysis of its current–voltage characteristic indicates that the energy level separation is about 110 meV and the silicon dot diameter is about 12 nm. © *1998 American Institute of Physics.* [S0003-6951(98)01210-8]

Semiconductor single electron devices based on the Coulomb blockade and quantum size effect have attracted much attention due to their small size, low power consumption, and unique functionality. However, to make the devices work at room temperature, the size of the quantum dot has to be smaller than 15 nm. This presents a challenge even to the state-of-the-art nanofabrication technology. Various novel approaches have been used to increase operation temperature, including oxidation,[1–3] anisotropic wet etch,[4–6] scanning tunneling microscope nano-oxidation process,[7] and side gate on thin silicon-on-insulator (SOI) wafer.[8]

Previously, the silicon single electron transistor operating at 170 K and single hole transistor operating at 110 K were reported.[9,10] Furthermore, the room temperature silicon single-electron memory has been demonstrated where a polysilicon dot is placed between the channel and the gate to serve as a storage node.[11] In this letter, we present the room-temperature operation of a single-electron quantum-dot transistor switch where the dot is placed inside the channel to switch the current.[12]

The device is a SOI metal–oxide–semiconductor field-effect transistor (MOSFET), but its channel consists of a silicon dot connected to two narrow wires through two constrictions (Fig. 1). In fabrication, e-beam lithography and reactive ion etch (RIE) were used to pattern a narrow (30 nm wide) but long channel in the top silicon layer (32 nm thick) of a SOI wafer. After growing a 10 nm thick SiO_2 in the (100) Si direction and 14 nm in the (110) direction at 950 °C, the nominal channel width was reduced from 30 nm to about 16. However, the noise in e-beam lithography created variations in the silicon channel width, and the variations became much enhanced during the oxidation due to the stress in the oxide (Fig. 2). The enhanced channel width variation created a series of dots inside the channel separated by constrictions. The dot size can be smaller than the nominal channel width if the separation between the two constrictions is less than the channel width. Furthermore, as we will describe later, at high temperatures only the smallest dot controls the behavior of the device. After the thermal oxidation, another 25 nm thick gate oxide was deposited by plasma enhanced chemical vapor deposition, followed by a 350 nm thick polysilicon using low pressure chemical vapor deposition. Then the gate was patterned by photolithography and RIE. The rest of the device process is similar to a standard MOSFET fabrication.

The device was characterized using an HP-4145B semiconductor parameter analyzer. The drain current (I_d) as a function of the gate voltage (V_g) ($I-V$) was measured at different temperatures with the drain voltage fixed at 100 mV (Fig. 3). The $I-V$ characteristic clearly shows four staircases at room temperature. As the temperature decreases, the staircases evolve into the peaks, suggesting the existence of quantum dots in the channel. These peaks are caused by the electron tunneling through the quantized energy levels inside the dot.

To determine whether these peaks come from the energy levels in a single dot or multiple dots, we first estimated the energy level separations in the dot from the observed $I-V$ characteristics. The transconductance versus gate voltage curve at room temperature (Fig. 4) shows that the gate voltage separations (ΔV_g) between those peaks are nearly the same, 1.4 V, strongly suggesting that these four major peaks come from the same dot. The energy level separation (ΔE) in the dot can be estimated by using $\Delta E = \alpha e \Delta V_g$, where the gate modulation coefficient α relates the gate voltage to the electron energy inside the dot. This coefficient can be determined from the temperature dependence of the peak's full width at half-maximum: FWHM$=3.5kT/(\alpha e)$,[13] where k is Boltzmann's coefficient, T is the temperature, and e is

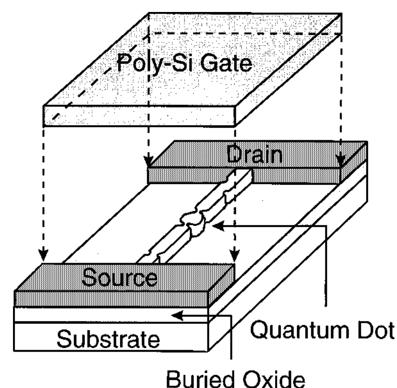

FIG. 1. Schematic of device structure.

[a]Electronic mail: lzhuang@ee.princeton.edu
[b]Electronic mail: chou@ee.princeton.edu

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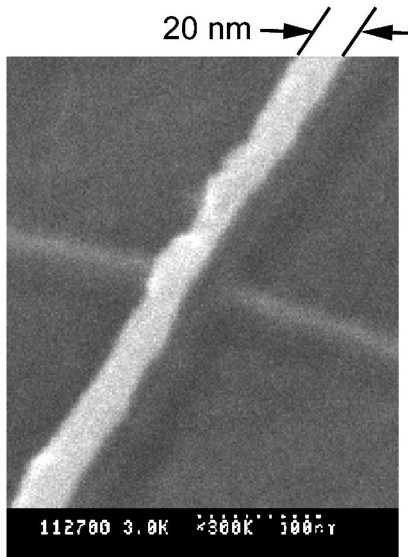

FIG. 2. Scanning electron micrograph of the channel after oxidation.

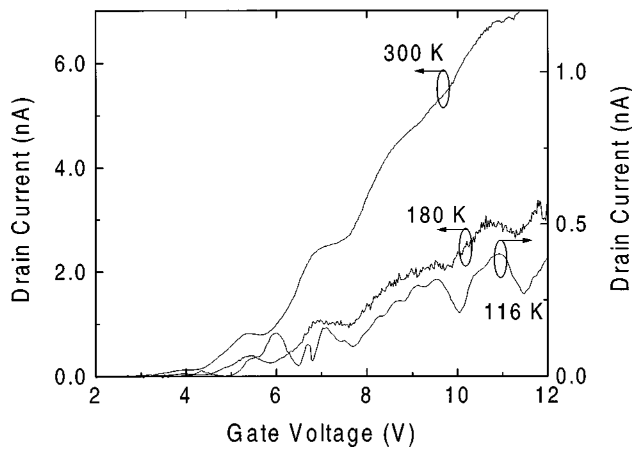

FIG. 3. Temperature dependence of drain current at fixed drain voltage, $V_{DS}=100$ mV.

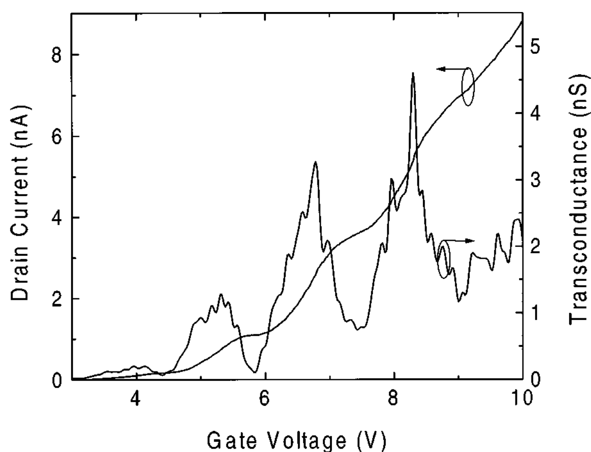

FIG. 4. $I-V$ characteristic and transconductance at room temperature.

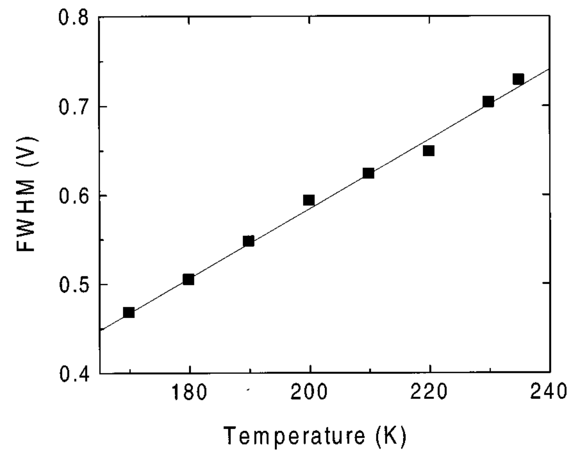

FIG. 5. Temperature dependence of FWHM of the second peak in Fig. 3 and linear curve fit.

electron charge. From the temperature dependence of FWHM of the second peak and the linear fit result (Fig. 5), α is found to be 0.077. Therefore, ΔE is 110 meV.

The energy level spacing also can be estimated from the differential conductance versus the drain voltage and the gate voltage plot (Fig. 6). Two rhombus are clearly shown in the plot. The nodes between the rhombus correspond to the three major peaks. The one that is related to the first peak is not seen because the differential conductance is too small at the threshold. The two rhombus shown are of the same size, further justifying that the oscillations come from a single dominant dot.[14] The energy spacing can be estimated from the plot to be 130 meV, agreeing with the previous estimation based on the peak separations.

Using the energy level separation, the size of the dot is estimated to be 12 nm in diameter. At this small size, both the Coulomb charging energy and the quantum confinement energy have to be considered. Assuming a spherical dot and an oxide thickness of 35 nm, the total capacitance of the dot is calculated to be 1.7 aF. Accordingly, the charging energy is 96 meV and the quantum energy is 17 meV. Therefore, the total energy of charging an electron into the dot is 113 meV, agreeing with the measured values.

Although there may be a number of dots formed in series inside the channel, we believe that the smallest dot deter-

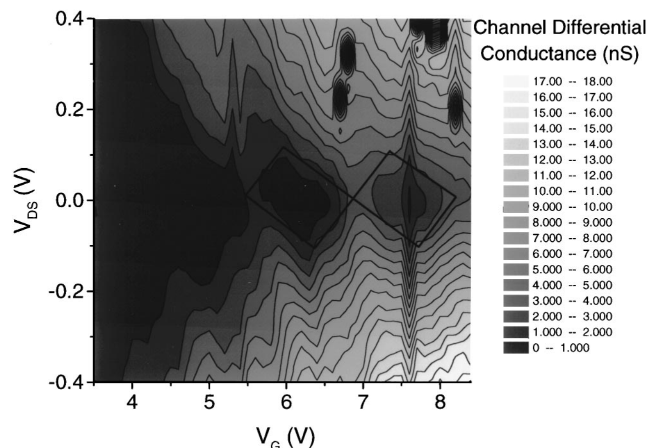

FIG. 6. Contour plot of channel differential conductance vs gate voltage and drain bias.

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mines the peaks in the $I-V$ at room temperature. The smallest dot has the highest charging energy, hence the highest threshold. It is the last one to be turned on, so that it dominates the behavior of the entire transport. The discreteness of the energy levels in the larger dots is negligible at room temperature but they can come into play at low temperatures, as indicated by the small peaks in Fig. 3.

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