Oscillations up to 712 GHz in InAs/AlSb resonant-tunneling diodes

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Oscillations have been obtained at frequencies from 100 to 712 GHz in InAs/AlSb double-barrier resonant-tunneling diodes at room temperature. The measured power density at 360 GHz was 90 W cm^{-2}, which is 50 times that generated by GaAs/AlAs diodes at essentially the same frequency. The oscillation at 712 GHz represents the highest frequency reported to date from a solid-state electronic oscillator at room temperature.

The double-barrier resonant-tunneling diode (RTD) has demonstrated useful high-speed characteristics as an oscillator and a switch. Until recently most of the high-speed experiments have been conducted with RTDs made from the GaAs/AlAs material system (GaAs quantum well and cladding layers, AlAs barriers). Oscillators made from such diodes have operated at room temperature up to 420 GHz.[1] Switches have been demonstrated with peak-to-valley switching times of 2 ps,[2] and 6–10 ps.[3] It has been argued that the oscillator frequency and the switching speed of GaAs/AlAs RTDs are limited primarily by the RC time delay in the negative-differential conductance (NDC) region of the current-voltage (I-V) curve.[1,4] In this letter, we present experimental oscillations from InAs/AlSb RTDs at frequencies up to 712 GHz. These results are consistent with a theoretical maximum frequency of oscillation f_{max} of 1.24 THz. According to our estimates, this f_{max} is limited more by the resonant-tunneling traversal and depletion-layer transit times than by the fundamental RC time delay of the device.

The InAs/AlSb materials system has several advantages over GaAs/AlAs for making high-speed RTDs.[5] First, the InAs/AlSb band offset (staggered type II at the Γ point) allows an electron to tunnel through an AlSb barrier with a smaller attenuation coefficient than it would have at the same energy in the AlAs barrier of a GaAs/AlAs structure (type-I band offset). This leads to a higher available current density ΔJ for a given barrier thickness, where $\Delta J = J_P - J_V$, and J_P and J_V are the peak and valley current densities, respectively. A higher ΔJ usually leads to a reduced RC time delay in RTDs. A second advantage is that electrons will drift across a given depletion layer much more rapidly in InAs than in GaAs provided that this layer is narrow enough ($\lesssim 0.1$ μm) or the voltage drop is small enough to maintain a low probability of impact ionization.[6] A shorter depletion-layer transit time in RTDs generally raises the f_{max}, as expected intuitively.[1] A third advantage is that InAs RTDs have a lower total series resistance R_S, which always increases the f_{max}. The lower R_S follows from the higher mobility of electrons in InAs (for any fixed n-type doping concentration) and the lower specific resistance of ohmic contacts.

One InAs/AlSb wafer (referred to as wafer B in Ref. 5) was used to make RTDs for the present work. It was grown by molecular beam epitaxy on semi-insulating (100)GaAs substrates at 500 °C. The double-barrier structure consists of two 1.5-nm-thick undoped AlSb barriers separated by a 6.4-nm-thick undoped InAs quantum well. Diode mesas are fabricated by first defining gold pads on top of the wafer by a photoresist liftoff technique. Approximately 500 nm of the epilayer material is then removed by wet chemical etching using the gold pad as a mask. The exposed surface of the etched wafer is a 1.0-μm-thick InAs epilayer doped to $N_D = 5\times10^{18}$ cm^{-3}. Further details regarding the fabrication are given in Ref. 5.

In preparation for high-frequency experiments, the fabricated wafer was diced into 100×100 μm chips and the sidewalls of the chips were plated with palladium and gold. This procedure creates a very low resistance current path between the diode mesas and the ground plane, which is the bottom surface of the chip. Between a mesa and the top edge of the chip, the current flows in the $N_D = 5\times10^{18}$ cm^{-3} InAs layer. From the top edge to the bottom edge, the current flows in the sidewall metalization. The dc current-voltage (I-V) characteristic of a 1.8-μm-diam diode is given in Fig. 1 with negative voltage applied to the top contact. The I-V curve shows a peak-to-valley current ratio of about 3.4 at room temperature, and a peak current density of 2.8×10^5 A cm^{-2}, corresponding to $\Delta J \cong 2.0\times10^5$ A cm^{-2}. The discontinuous nature of the experimental I-V curve in the NDC region is caused by self-rectification of the oscillations.[7]

To study these diodes as oscillators, the chips were mounted in one of four full-height rectangular waveguide resonators operating in frequency bands around 100, 200, 400, and 650 GHz, respectively. The design of the first three resonators and the techniques used to measure power and frequency in these bands are the same as used in previous experiments.[1] The highest power density obtained by

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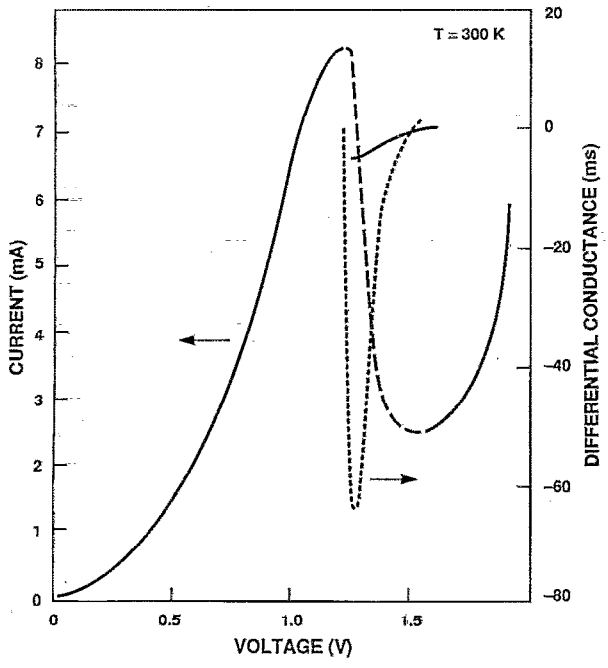

FIG. 1. Room-temperature I-V curve (solid line) of a 1.8-μm-diam InAs/AlSb RTD measured while the diode was oscillating near 360 GHz. The step structure spanning the NDC region is caused by rectification of the oscillations. The long-dashed curve connecting the peak and valley points is a physical model of the (stable) I-V curve that would be measured in the absence of oscillations. The short-dashed line is the G-V curve (right-hand scale) derived from the model I-V curve.

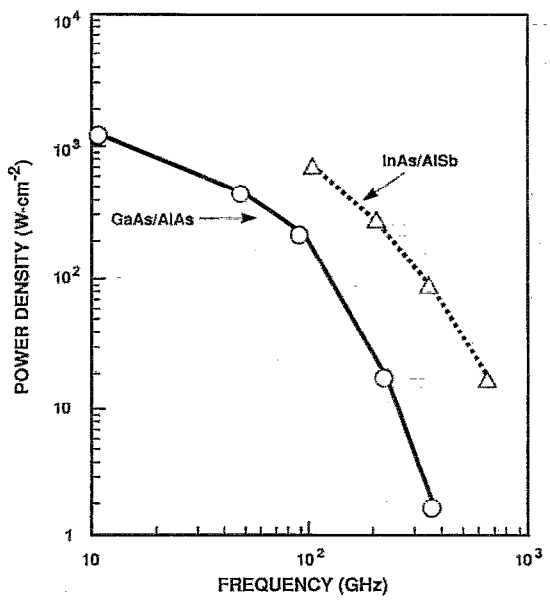

FIG. 2. Experimental oscillator results for the InAs/AlSb RTD (solid line) and the best GaAs/AlAs (dashed line) tested to date. All of the oscillations were obtained at room temperature.

1.8-μm-diam diodes in each of the resonators is shown in Fig. 2. At 360 GHz an absolute power of 3 μW was obtained, corresponding to a power density of 90 W cm^{-2}. This is 50 times the power density obtained previously from GaAs/AlAs RTDs at 370 GHz, and is indicative of a very high f_{max}, as discussed later.

The highest frequency oscillations were obtained in a 0.030×0.015 cm rectangular waveguide resonator designed to operate between roughly 600 and 750 GHz. The highest power obtained in this resonator was 0.3 μW from a 1.8-μm-diam InAs/AlSb RTD oscillating at 712 GHz. This corresponds to a power density of 15 W cm^{-2}. Our uncertainty in these values is about 50%, reflecting the difficulty in calibrating the power measurements in this frequency region. The power was measured by coupling the radiation out of the waveguide with a pyramidal feedhorn and focusing it onto a composite bolometer. The oscillation frequency was measured by placing a scanning Fabry–Perot spectrometer in the path between the waveguide oscillator and the bolometer. By scanning one mirror of the spectrometer over a distance of about 5 cm, we were able to determine the wavelength to an accuracy of 0.1 %. Using the spectrometer, we looked for changes in the oscillation frequency with variations in the position of the waveguide backshort. We found that the backshort tuned the output frequency by about 2 GHz. This tuning would probably not be observed if the oscillation was a second or higher harmonic since propagation at the fundamental frequency would not occur in the waveguide, and thus the oscillation frequency would not depend on the backshort position. However, second (or higher) harmonic tuning effects cannot be ruled out, and better techniques are needed for this determination.

We estimate the f_{max} of the present diodes by applying a small-signal electrical model recently developed for the RTD.[1] The basis for the model is a lumped-element equivalent circuit consisting of the parallel combination of a conductance G and a capacitance C, in series with R_S. The quantity G is the differential conductance across the active region of the device, C accounts for the accumulation and depletion space-charge layers on the cathode and anode sides, respectively, of the double-barrier structure, and R_S is the sum of the ohmic-contact resistance and the spreading resistance from the RTD mesa to the ground plane of the chip. At high frequencies or short time scales, this circuit must be generalized to account for several time-delay mechanisms. The resonant-tunneling traversal time is included by replacing G with a resonant-tunneling admittance, $G(1 + i\omega\tau_1)^{-1}$, where τ_1 is the quasibound-state lifetime. This is equivalent to adding an inductance, $L_{QW} = \tau_1/G$, into the basic circuit. The effect of the depletion-layer transit time is included through an ac analysis in which the electron is assumed to cross the depletion layer with a uniform drift velocity v_D, but the double-barrier structure remains as a lumped-element (injection admittance) proportional to $G(1 + i\omega\tau_1)^{-1}$. The classical skin effect confines the ac current to a surface layer having a thickness roughly equal to the skin depth, and thus it causes R_S to increase slowly with frequency. All parameters in the model other than G depend weakly on bias voltage and thus are assumed to be constant throughout the NDC region.

We estimate G from a theoretical model of the (stable) I-V curve in the NDC region. The theoretical NDC region shown in Fig. 1, is the sum of a resonant-tunneling and an

excess-current component. The resonant-tunneling component is based on the stationary-state tunneling integral with a Breit–Wigner form for the transmission probability.[8] The excess-current component is a second-order polynomial in V. It is not possible to estimate G from the experimental I-V curve since this curve is highly distorted by the oscillation. We determine τ_1 from separate numerical calculations of the full width at half maximum, Γ_1, of the transmission probability T^*T, using a two-band model for the tunneling dispersion relation in the barriers. The result is $\tau_1 = \hbar/\Gamma_1 = 90$ fs. The capacitance is approximated by $C = \epsilon a(L_D + L_W + L_A)^{-1} = 2.8$ fF, where a is the RTD area (2.5×10^{-8} cm^2), L_W is the width of the double-barrier structure (9.4 nm), L_D is the width of the depletion layer ($\simeq$75 nm), and L_A is the width of the accumulation layer ($\sim$20 nm). The values of L_D and L_A are taken from the solution to Poisson's equation with the peak voltage applied across the device. The drift velocity across the depletion layer, $v_D = 8\times10^7$ cm s^{-1}, is obtained from the results of Monte Carlo simulations of electron transport in InAs under conditions similar to those in the depletion layer at the peak voltage.[6] The ohmic contact resistance is assumed to be 2 Ω in accordance with a specific contact resistance of $\rho_C = 5\times10^{-8}$ Ω cm^2. This ρ_C was estimated from transmission-line-model (TLM) measurements made on separate InAs ohmic contacts.[9] The frequency-dependent spreading resistance is approximated as 1.0 Ω at dc and 1.5 Ω at 600 GHz, based on a resistivity of 0.0003 Ω cm in the InAs epilayer doped to $N_D = 5\times10^{18}$ cm^{-3}.

The small-signal model yields a quantity, called the resistive cutoff frequency f_R, at which the real part of the terminal impedance equals zero. This is a frequency above which oscillation cannot occur. We plot f_R in Fig. 3 as a function of G with the other parameters held constant. This curve displays a peak value of 1.24 THz at $G = -20$ mS. This is a realizable G since it is less in magnitude than the minimum G (-64 mS) in the theoretical NDC region in Fig. 1. Thus, 1.24 THz is the $f_{\max}$ of this RTD.

The presence of the peak in the f_R vs G curve is a consequence of the series resistance in the model. To understand this, note that the basic G-C-R_S circuit yields $f_R = (2\pi C)^{-1}(-G/R_S - G^2)^{1/2}$. This expression displays a peak value of $(4\pi CR_S)^{-1}$ at $G = (2R_S)^{-1}$. The addition of the lifetime and transit time delays leads to a reduction in the $f_{\max}$ (and a reduction in the G at which the $f_{\max}$ occurs), but it does not change the peaked nature of the f_R vs G curve. The basic circuit can also be described by an RC time constant, $\tau_{RC} = C(-G/R_S - G^2)^{-1/2}$. Over the range of the G-V curve in Fig. 1 (and assuming $R_S = 3$ Ω and $C = 2.8$ fF) this expression yields a minimum value of $\tau_{RC} = 21$ fs at $G = -64$ mS. This is much less than τ_1 (90 fs) or the depletion-layer transit time ($L_D/v_D = 94$ fs). Therefore, we believe that the speed of this RTD is not limited by the fundamental RC time delay, and that changes in the materials parameters (such as thinner AlSb barriers to decrease τ_1 or optimization of the InAs depletion layer to reduce the effect of transit time) could further increase the $f_{\max}$. The difference between the present τ_{RC} and that of the best GaAs/AlAs RTDs ($\tau_{RC} \geqslant 100$ fs) is attributed in part to the four times larger ΔJ of the InAs/AlSb RTD, and in part to the lower series resistance (at least three times lower specific contact and spreading resistances). The larger ΔJ is responsible for the fact that the minimum G in Fig. 1 is about ten times larger in magnitude than the minimum G of a GaAs/AlAs RTD having the same area.

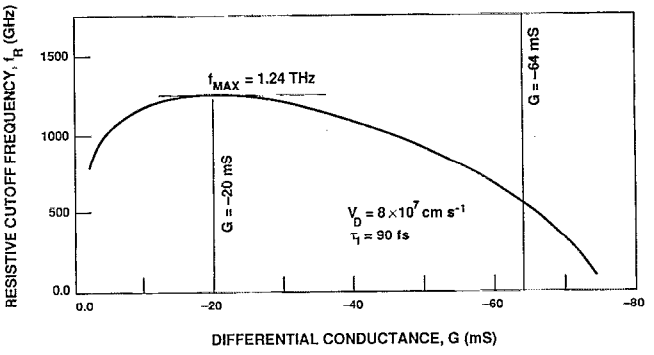

FIG. 3. Theoretical resistive cutoff frequency vs differential conductance for a 1.8-μm diam InAs/AlSb RTD obtained from the small-signal impedance model of the device.

In summary, an InAs/AlSb RTD has oscillated up to 712 GHz at room temperature, and has generated a 50 times higher power density at 360 GHz than GaAs/AlAs RTDs operating near the same frequency. We emphasize that these results were obtained with RTDs containing a 7% lattice mismatch between the active epitaxial layers and the semi-insulating GaAs substrate.[5] This suggests that InAs/AlSb RTDs could find application in a number of monolithic integrated circuits, such as planar oscillator arrays and signal-processing circuits, for which semi-insulating GaAs is the most desirable III-V substrate material.

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