Synthesis and Simulation with Altera's Quartus II software
A short Tutorial

Altera's Quartus II software is available for free from the following website:

http://altera.com/products/software/products/quartus2web/sof-quarwebmain.html

1. Compiling and Synthesizing the Design

In order to compile and synthesize your design you need to open the design file (in verilog or VHDL) and create a project for your design. For the Altera tools it is important that the name of the top module of your design has the same name as the file name.

- From the main **File** menu choose **Open** to open your design file
- From the main **File** menu start **New Project Wizard** that will guide you in the creation of the project for your design. (If you already have an existing project, choose **Open Project** instead).
- The following information will be required to build the project file.
  - File name with the top module
  - Location of other modules/files, referenced by the top file
  - Device, such as Max, Stratix, Cyclon II, etc.
  - Optional: other, third party tools for simulation, verification, and synthesis to be used with this project.
- Once the project is created, you must compile your design.
  - Use the command **Start Compilation** from the main **Processing** menu or click on the Start Compilation icon (violet triangle) from the main memu.
  - Full compilation includes: initial design analysis and synthesis, fitting and assembling the design on the target device, and performing timing analysis. All of those steps are needed for creating a design that can be downloaded onto the PLD device and for timing analysis. For functional analysis only the initial compilation step (Analysis and Synthesis) is needed.

2. Viewing Design after Compilation

This is a very useful feature that will allow you to visually check if the design coded in the HDL file(s) is the one you intended to create. Several views are available. All of those views are accessible from the main **Tools** menu.

- **RTL Viewer**, provides a hierarchical view of your design, from RTL down to gate-level, depending how your design was coded in HDL.
- **FSM Viewer**, gives a state transition diagram and table for designs written in a finite state machine format (with explicitly defined states)
- **Technology Mapped Viewer**, shows the design mapped onto lookup tables (LUTs)
- **Chip Viewer** provides physical view of the design.

3. Functional Simulation

To perform functional simulation, you need to generate the required functional simulation netlist and set the simulation parameter to *functional*. You do not need to run the compilation or synthesis to perform functional simulation.

- From the **Processing** menu, choose **Generate Functional Simulation Netlist**. No compilation is required.
- Specify simulation settings by opening the **Quartus II** menu (in the main menu banner) and choosing **Simulator Tool.** A window will open that will allow you to set the simulation mode. Set the simulation mode to *functional*.
- (An alternative way to set the simulation parameters is to go to **Assignments** (in the main menu) then **Settings**, and choose **Simulator Settings**, which will open the same window. Or go to Tools, choose Simulation **Tool**, etc. These paths will allow you to set parameters for all the tools.).

You can also set Simulation Breakpoints

- Go to **Processing** menu, then to **Simulation Debug** menu and click on **Breakpoints**. A new window will open that will help you set up the breakpoints in your simulation.

4. Timing Simulation

To perform timing simulation, you must first fully compile and synthesize the design using one of the target devices (FPGA, PLD) from the Quartus II device library. The library is presented to you when you first create the Project. (You can change the device by opening the **Assignments** menu and then choosing the **Device** menu, if needed.) Only when the design is fully mapped on the target device will the software know the actual delays of logic blocks and interconnect wires.

- In the main **File** menu open **New** file
  - click on **Other Files**
  - chose **Vector Waveform File** (VWF) item

  A simulation window opens with two major fields: the left window is reserved for all the signals (input, output, registers, etc.) and the right window will show the actual waveforms.

- Before you start creating the waveform, you should define the *grid* in time units and the simulation time, called *end time*. To do that go to the **Edit** menu and choose **Grid** to set up the grid size, and **End Time** to define the simulation time. Pay attention to the units you use. The PLD devices available in the Quartus library run at 200 - 400MHz, so you can expect delays in the order of several nanoseconds.

- Make sure to set the correct simulation mode, in this case timing mode. From the **Quartus II** menu choose **Simulator Tool.** In the window that will open, set the simulation mode to *timing.*

- Creating the simulation waveforms
    - Position the mouse in the left part of the window (reserved for signal names) and right-click there. Choose option **Insert Node or Bus,** then click on **Node Finder.** It will open a new window that will allow you to bring in the signals into the simulator. Use **Filter** to select the required signal types (e.g. *Pins: all*) and click on **List** to see the signals available for simulation. Select the signals you need in the **Nodes Found** window and move them to the **Selected Nodes** window using the > and >> buttons. When you close the window, the selected nodes will appear in the simulation window.
    - Select the signal you need (left click) and use the drawing tools and signal value assignment facilities (on the left part of the menu) to create a desired waveform.
    - Pay special attention to your clock signal. You can give it a periodic value by selecting (right click) its signal name, selecting the **Value** from the pull-down menu and then choosing the **Clock** option. A new window will open, which will allow you to specify the clock frequency and duty cycle.
- Make sure to save the waveform before performing simulation, typically under the same name as your design (with automatically given extension *.vwf*). If several versions of the simulation file are created, you have to tell simulator which *vwf* file to use. To do that, go to **Quartus II** (in the main menu), choose **Simulator Tool**, and provide the simulation file name in the Simulation input field.

- Running the simulation:
    - Click on the simulation icon (blue waveform) from the main menu to start the simulation. (Alternatively, choose the **Start Simulation** option from the **Processing** menu). If you need to change the simulation parameters (grid size, end time, simulation file, etc.) go to the respective assignment menus as described above.
    - View the simulation results in the **Simulation Report**, automatically created in the main simulation window. If you want to make changes to the input waveform, do it on the original input simulation waveform (your *file.vwf*), not on the simulation result waveform.
    - Advances feature: Quartus II allows you to compare the simulation results to a reference file, should you have one. To do that, go to the **View** menu and choose Compare to **Waveforms in File**.

5. Online Tutorials and Help

Additional information on the different tools and options of Quartus II is available using the **Help** menu and the embedded **Tutorial**.