



ECE 332 – Embedded Systems Lab

Lab 1: Using NIOS II processor for code execution on FPGA

Objectives

- Introduction to Altera tools
- Walk through from project creation to chip configuration (Lab1-Part I)
- Instructions to get started with Part II

Tools

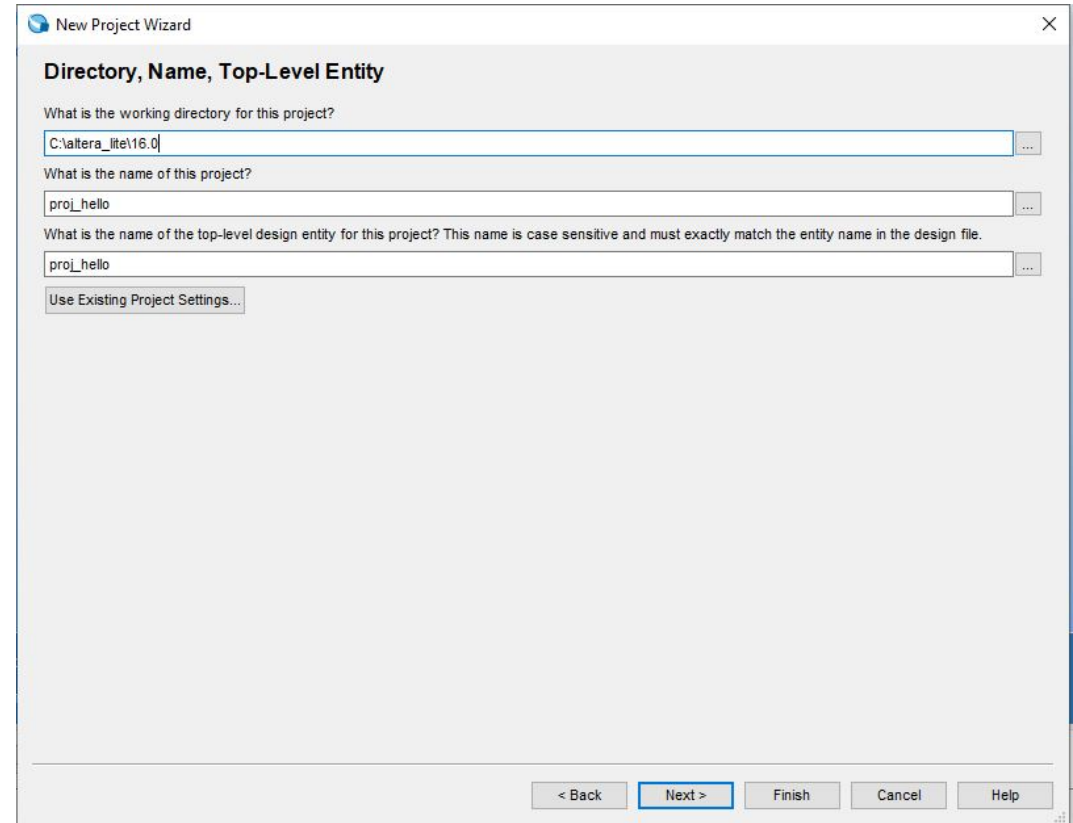
- Quartus Prime
 - FPGA development: Design, simulation, synthesis and download
- QSYS
 - Build target QSYS system
 - Based on a Processor-core (NIOS II processor), you can add other peripherals (e.g. Parallel IO, Ethernet Controller, Serial Ports, etc.)
- NIOS II Software Build Tools for Eclipse
 - Software platform for developing programs

Lab1 Objectives

- Part 1 :
 - Display “Hello, world” in your debug console from NIOS II
- Part 2 :
 - Implement a counter program and display the output on the LED, and the seven segment display.

New Project Creation

- Open Quartus Prime, and select file -> New Project Wizard...
- Specify a working directory and name your project
- NOTE: Make sure your working directory contains no white-space. (This will cause problems later when trying to compile your project from the QSYS)



The screenshot shows the 'New Project Wizard' dialog box with the title 'New Project Wizard'. The main section is titled 'Directory, Name, Top-Level Entity'. It contains three text input fields with browse buttons (three dots) to their right. The first field is labeled 'What is the working directory for this project?' and contains the text 'C:\altera_lite\16.0'. The second field is labeled 'What is the name of this project?' and contains the text 'proj_hello'. The third field is labeled 'What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.' and also contains the text 'proj_hello'. Below these fields is a button labeled 'Use Existing Project Settings...'. At the bottom of the dialog are five buttons: '< Back', 'Next >', 'Finish', 'Cancel', and 'Help'. The 'Next >' button is highlighted with a blue border.

FPGA Selection

- Select Cyclone V in the drop-down box labeled “family”. We will be using device 5CSEMA5F31C6.
- Click finish. All necessary project parameters have been configured.

New Project Wizard

Family, Device & Board Settings

Device Board

Select the family and device you want to target for compilation.
You can install additional device support with the Install Devices command on the Tools menu.

To determine the version of the Quartus Prime software in which your target device is supported, refer to the [Device Support List](#) webpage.

Device family

Family: Cyclone V (E/GX/GT/SX/SE/ST)

Devices: All

Target device

☐ Auto device selected by the Filter

☒ Specific device selected in 'Available devices' list

☐ Other: n/a

Show in 'Available devices' list

Package: Any

Pin count: Any

Core Speed grade: Any

Name filter:

☒ Show advanced devices

Available devices:

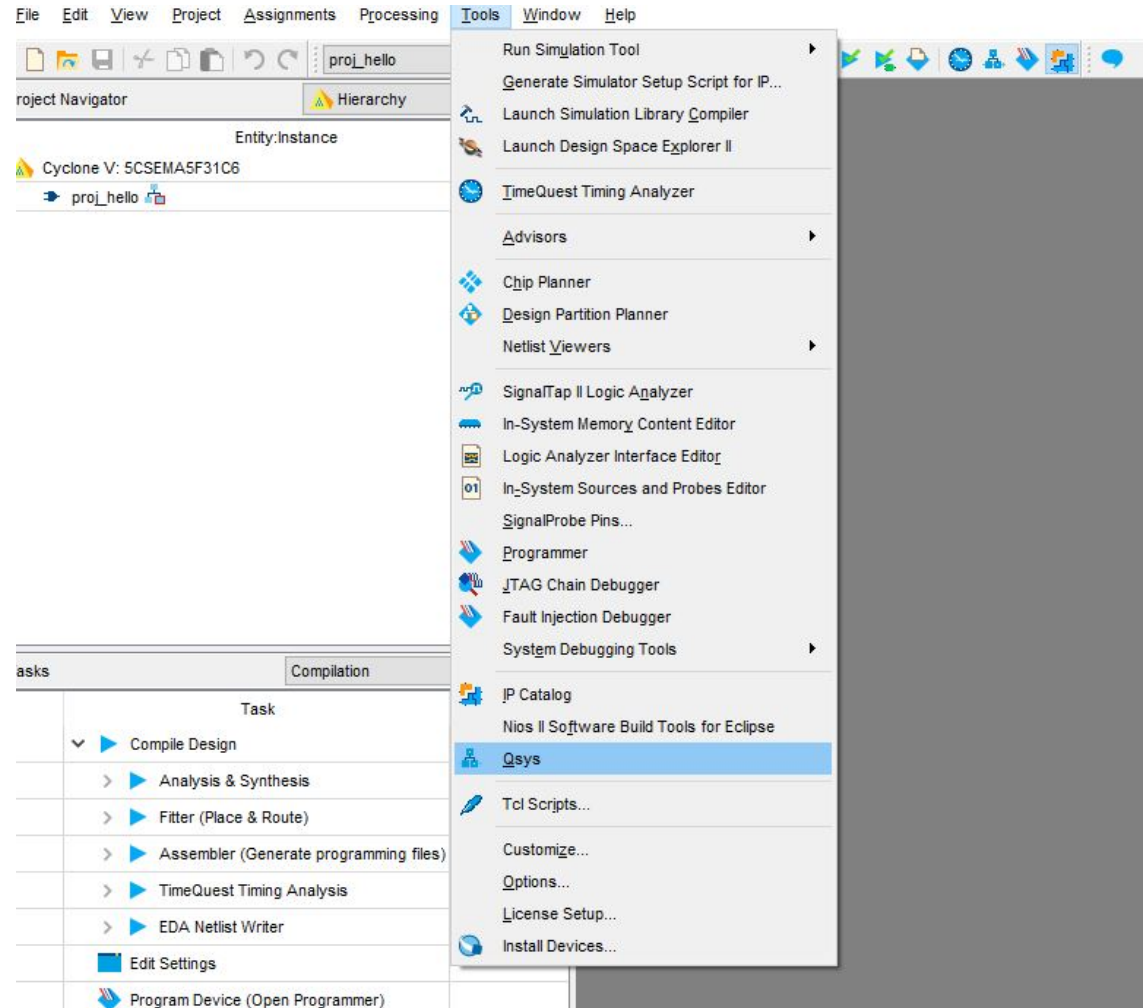
Name	Core Voltage	ALMs	Total I/Os	GPIOs	GXB Channel PMA	GXB Channel PCS	F ^
5CSEMA5F31A7	1.1V	32070	457	457	0	0	0
5CSEMA5F31C6	1.1V	32070	457	457	0	0	0
5CSEMA5F31C7	1.1V	32070	457	457	0	0	0
5CSEMA5F31C8	1.1V	32070	457	457	0	0	0
5CSEMA5F31I7	1.1V	32070	457	457	0	0	0

< Back Next > Finish Cancel Help

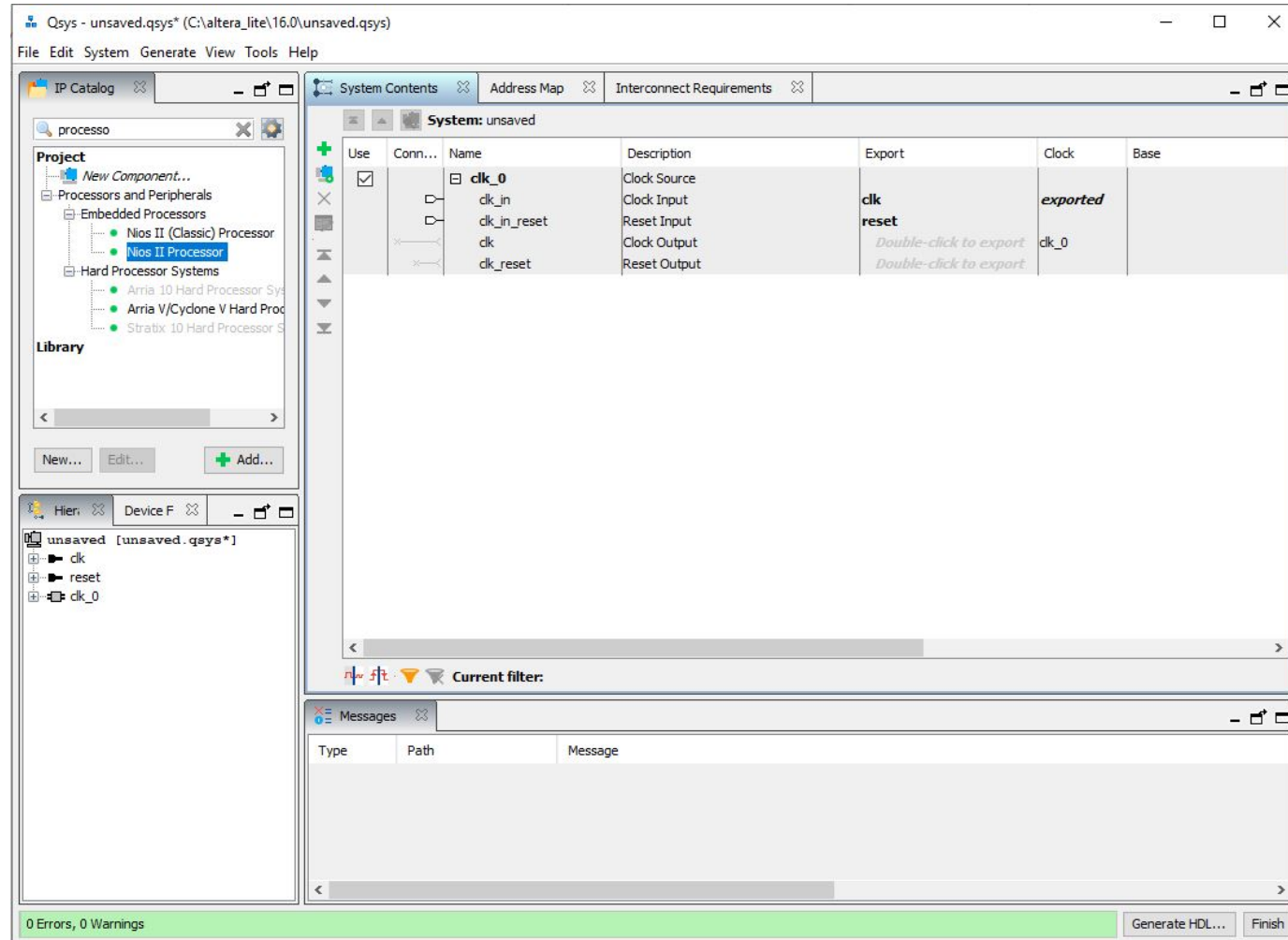
Using the QSYS System

- SOPC Builder (System on a Programmable Chip Builder) is software made by [Altera](#) that automates connecting IP cores to create a complete system that runs on any of its various [FPGA](#) chips.
- Qsys is the next-generation SOPC Builder tool powered by a new FPGA-optimized network-on-a-chip (NoC) technology.
- Open Tools -> Qsys to start the system, save the system with the same name as the Top Level entity.

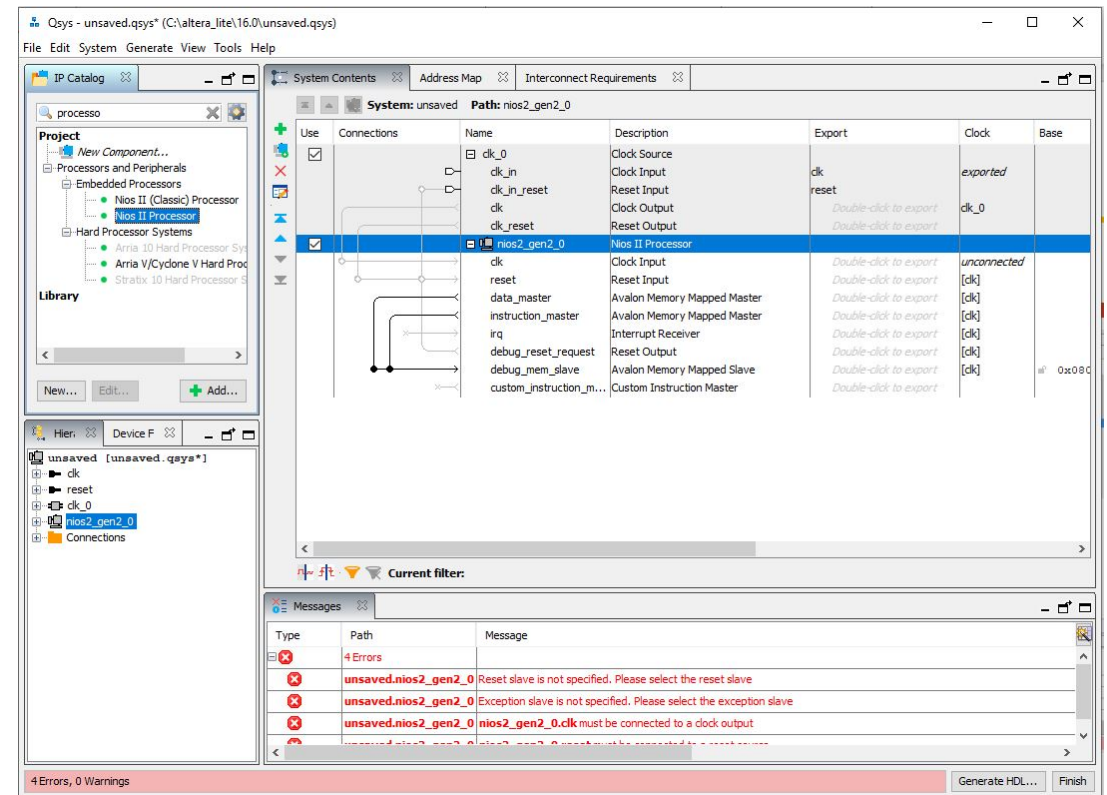
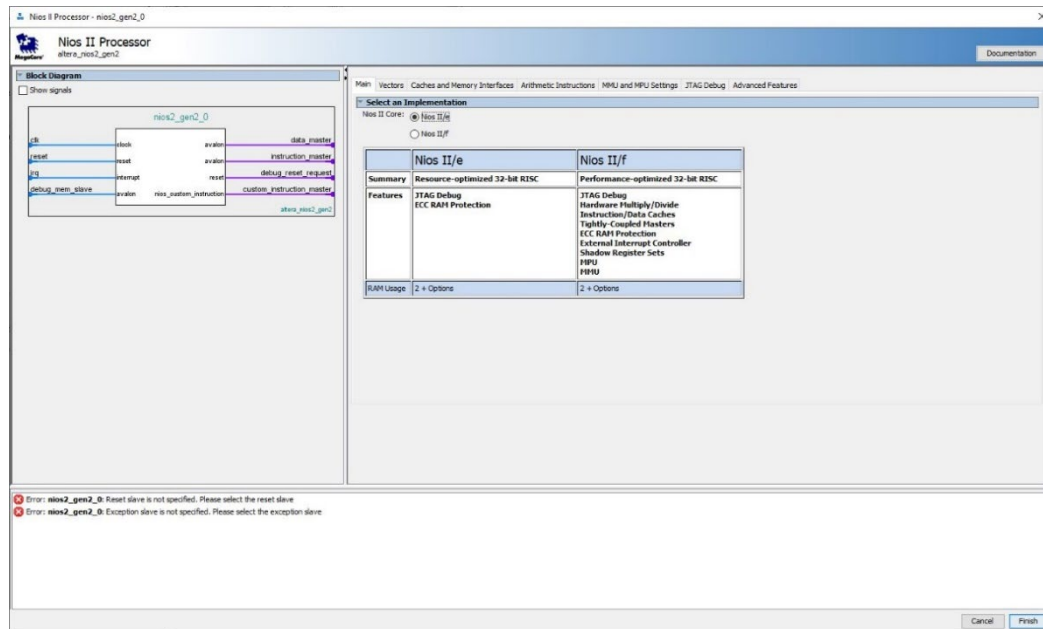
Launching QSYS



QSYS Screenshot

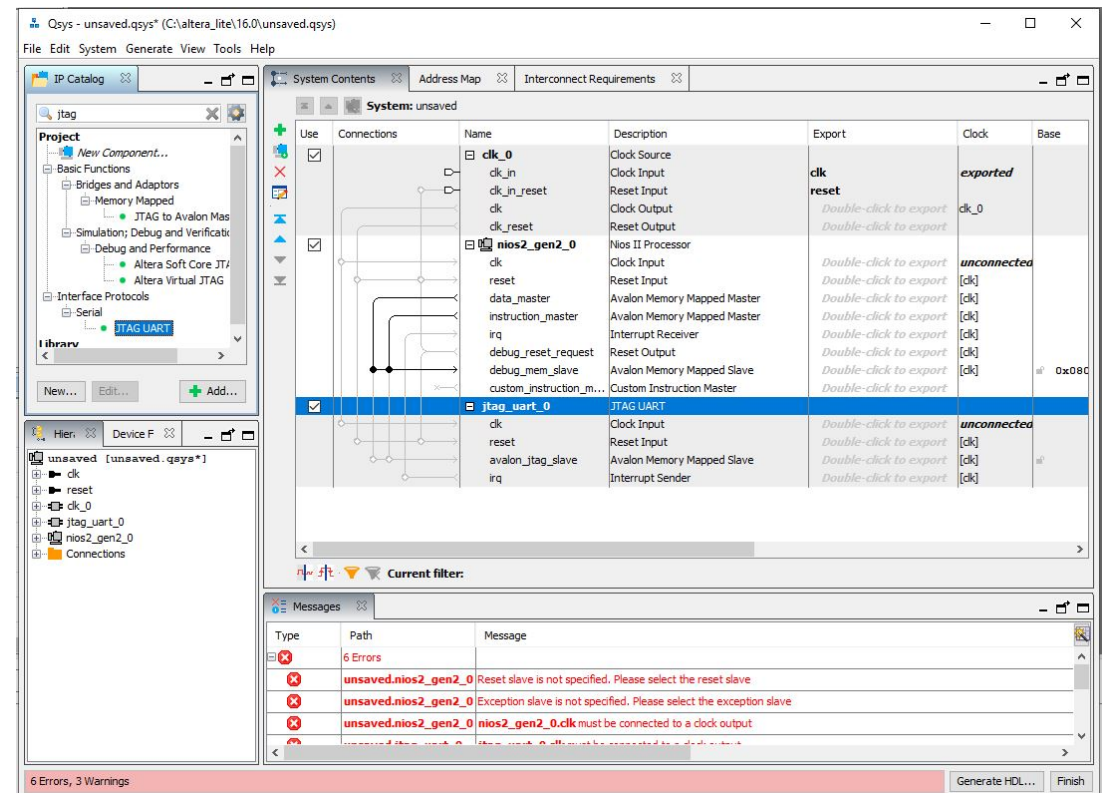
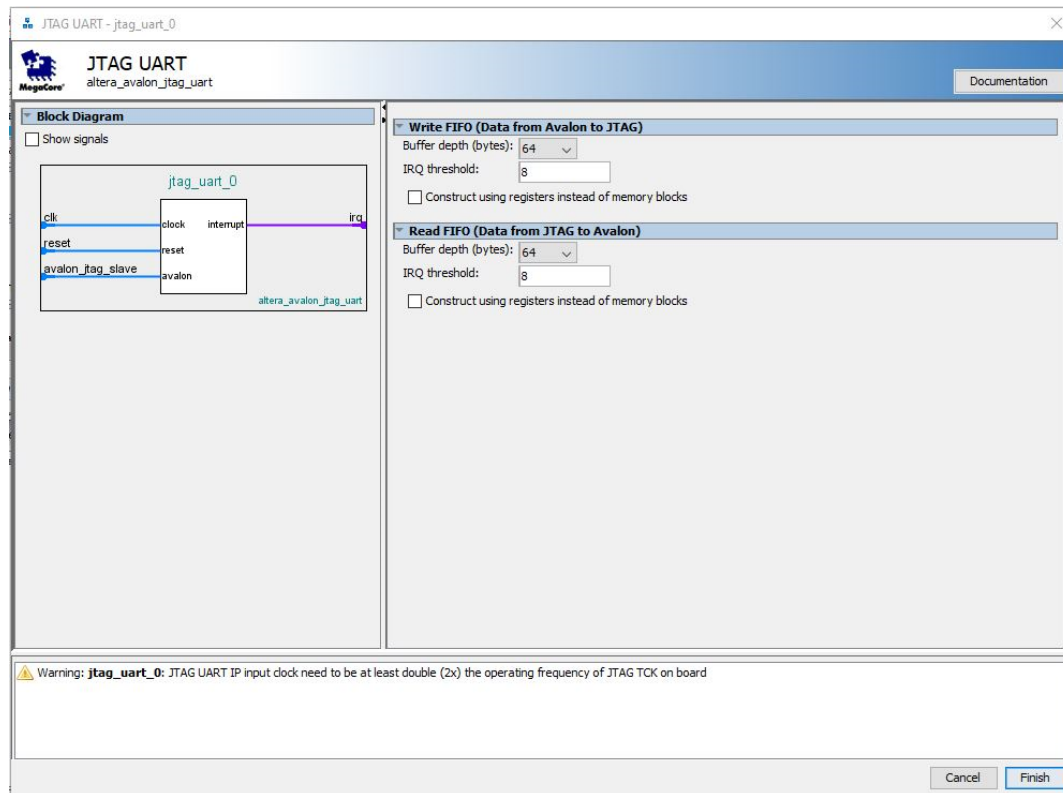


Adding NIOS II Processor



Adding JTAG UART

- Next, we will be adding a JTAG UART module, found under Serial.



Adding On -Chip Memory

Memory type

Type:

RAM (Writable) ▾

☐ Dual-port access

☐ Single clock operation

Read During Write Mode:

DONT_CARE ▾

Block type:

AUTO ▾

Size

☐ Enable different width for Dual-port access

Slave S1 Data width:

32 ▾

Total memory size:

4096

bytes

☐ Minimize memory block usage (may impact fmax)

Read latency

Slave s1 Latency:

1 ▾

Slave s2 Latency:

1 ▾

ROM/RAM Memory Protection

Reset Request:

Enabled ▾

ECC Parameter

Extend the data width to support ECC bits:

Disabled ▾

Memory initialization

☒ Initialize memory content

☐ Enable non-default initialization file

Type the filename (e.g: my_ram.hex) or select the hex file using the file browser button.

User created initialization file:

onchip_mem.hex

☐ Enable In-System Memory Content Editor feature

Instance ID:

NONE

Memory will be initialized from unsaved_onchip_memory2_0.hex

The screenshot shows the Qsys IDE interface. The top menu bar includes File, Edit, System, Generate, View, Tools, and Help. The main window is titled "Qsys - unsaved.qsys* (C:\altera_lite\16.0\unsaved.qsys)". The "System Contents" tab is active, showing a hierarchical tree of components on the left and a table of their properties on the right.

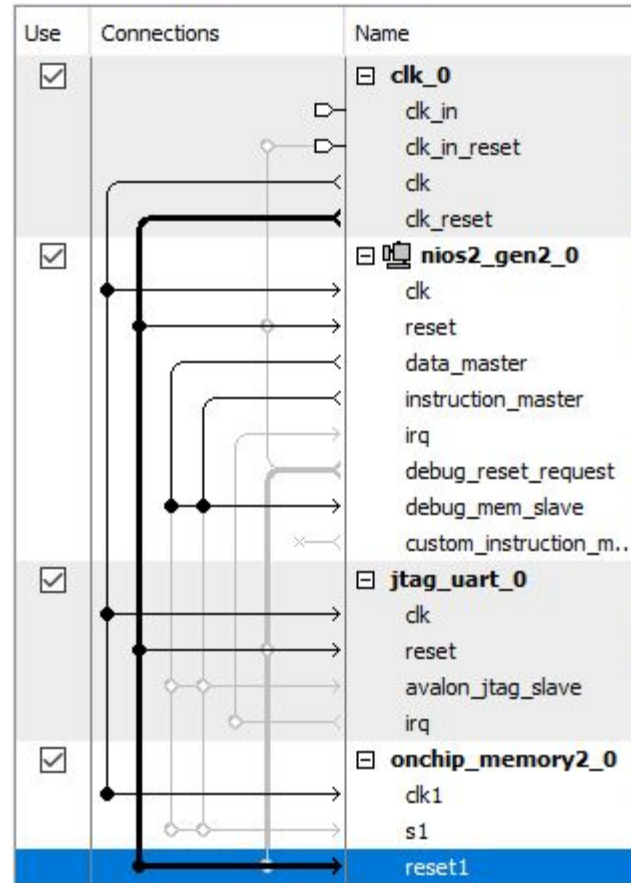
The hierarchical tree on the left shows the following structure:

- Project
 - New Component...
 - Basic Functions
 - On Chip Memory
 - Altera On-Chip Flash
 - On-Chip Memory (RAM or ROM)
- Library

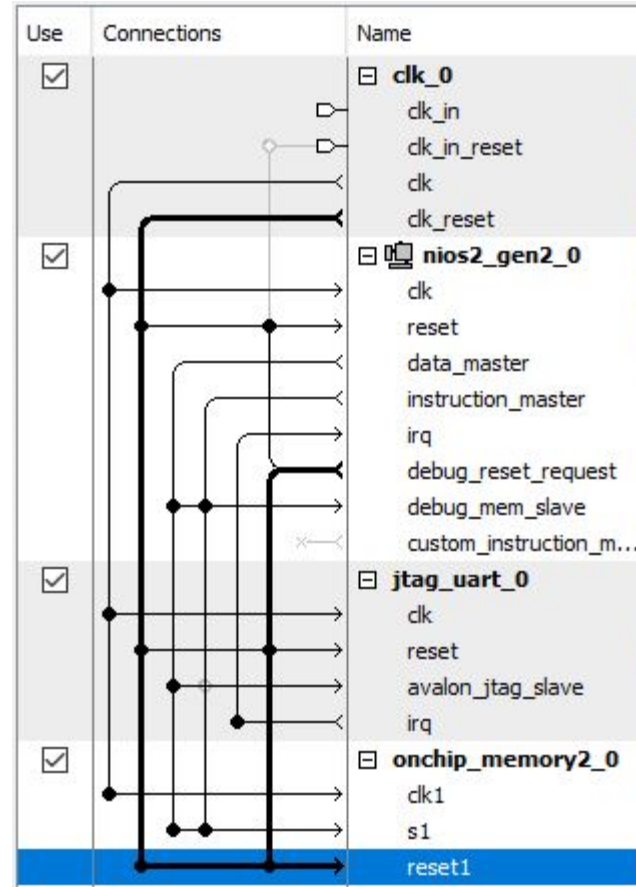
The table on the right lists the components and their properties:

Use	Connections	Name	Description	Export	Clock	Base
<input type="checkbox"/>		clk_in	Clock Input	clk	exported	
<input type="checkbox"/>		clk_in_reset	Reset Input	reset		
<input type="checkbox"/>		clk	Clock Output		clk_0	
<input type="checkbox"/>		clk_reset	Reset Output			
<input type="checkbox"/>		nios2_gen2_0	Nios II Processor			
<input type="checkbox"/>		clk	Clock Input			
<input type="checkbox"/>		reset	Reset Input			
<input type="checkbox"/>		data_master	Avalon Memory Mapped Master			
<input type="checkbox"/>		instruction_master	Avalon Memory Mapped Master			
<input type="checkbox"/>		irq	Interrupt Receiver			
<input type="checkbox"/>		debug_reset_request	Reset Output			
<input type="checkbox"/>		debug_mem_slave	Avalon Memory Mapped Slave			
<input type="checkbox"/>		custom_instruction_master	Custom Instruction Master			
<input type="checkbox"/>		jtag_uart_0	JTAG UART			
<input type="checkbox"/>		clk	Clock Input			
<input type="checkbox"/>		reset	Reset Input			
<input type="checkbox"/>		avalon_jtag_slave	Avalon Memory Mapped Slave			
<input type="checkbox"/>		irq	Interrupt Sender			
<input checked="" type="checkbox"/>		onchip_memory2_0	On-Chip Memory (RAM or ROM)			
<input type="checkbox"/>		clk1	Clock Input			

Clock and Reset Connections



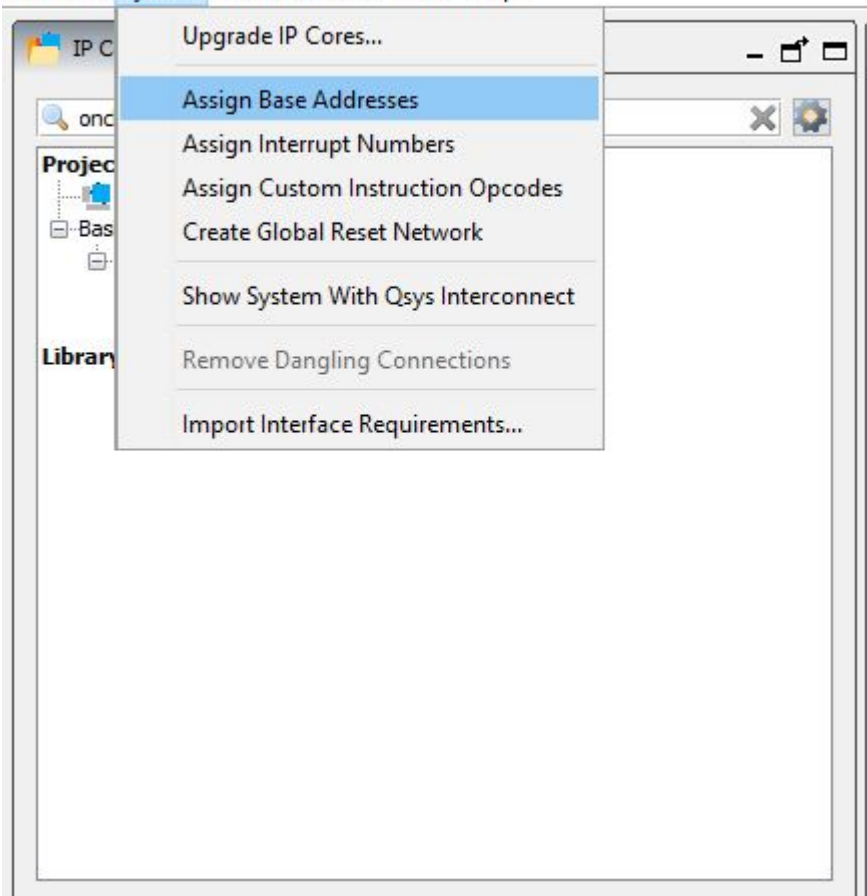
Other Connections



Assigning Reset and Exception Vectors

Qsys - unsaved.qsys* (C:\altera_lite\16.0\unsaved.qsys)

File Edit System Generate View Tools Help



The screenshot shows the 'Address Map' window in the Qsys software. The window displays a table of system components and their address ranges. The components are listed in the left pane, and the table in the center shows their details.

Use	Connections	Name	Description	Export	Clock	Base	End	IRQ	Tags	Opcode Name
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	clk_0	Clock Source	clk	exported					
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	clk_in	Clock Input	Double-click to export	clk_0					
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	clk_in_reset	Reset Input	Double-click to export						
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	clk_reset	Clock Output	Double-click to export						
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	reset	Reset Output	Double-click to export						
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	nios2_gen2_0	Nios II Processor							
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	clk	Clock Input	Double-click to export	clk_0					
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	reset	Reset Input	Double-click to export	[clk]					
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	data_master	Avalon Memory Mapped Master	Double-click to export	[clk]					
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	instruction_master	Avalon Memory Mapped Master	Double-click to export	[clk]					
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	irq	Interrupt Receiver	Double-click to export	[clk]			IRQ 0	IRQ 31	
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	debug_reset_request	Reset Output	Double-click to export	[clk]					
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	debug_mem_slave	Avalon Memory Mapped Slave	Double-click to export	[clk]	# 0x2800	0x2fff			
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	custom_instruction_m...	Custom Instruction Master	Double-click to export	[clk]					
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	jtag_uart_0	JTAG UART							
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	clk	Clock Input	Double-click to export	clk_0					
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	reset	Reset Input	Double-click to export	[clk]					
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	avalon_jtag_slave	Avalon Memory Mapped Slave	Double-click to export	[clk]	# 0x3000	0x3007			
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	irq	Interrupt Sender	Double-click to export	[clk]					
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	onchip_memory2_0	On-Chip Memory (RAM or ROM)							
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	clk1	Clock Input	Double-click to export	clk_0	# 0x1000	0x1fff			
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	s1	Avalon Memory Mapped Slave	Double-click to export	[clk1]					
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	reset1	Reset Input	Double-click to export	[clk1]					

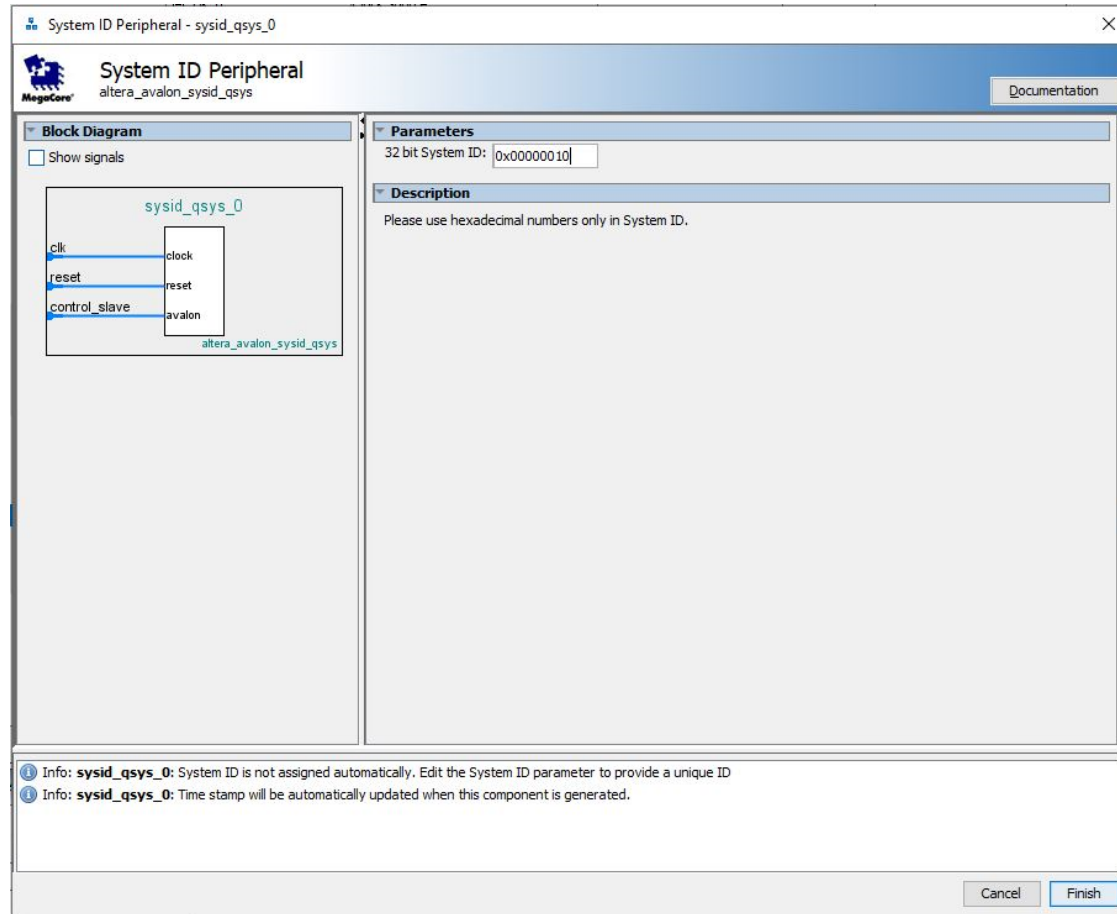
Current filter:

Messages

Type	Path	Message
1 Info Message		
1	unsaved.jtag_uart_0	JTAG UART IP input clock need to be at least double (2x) the operating frequency of JTAG TCK on board

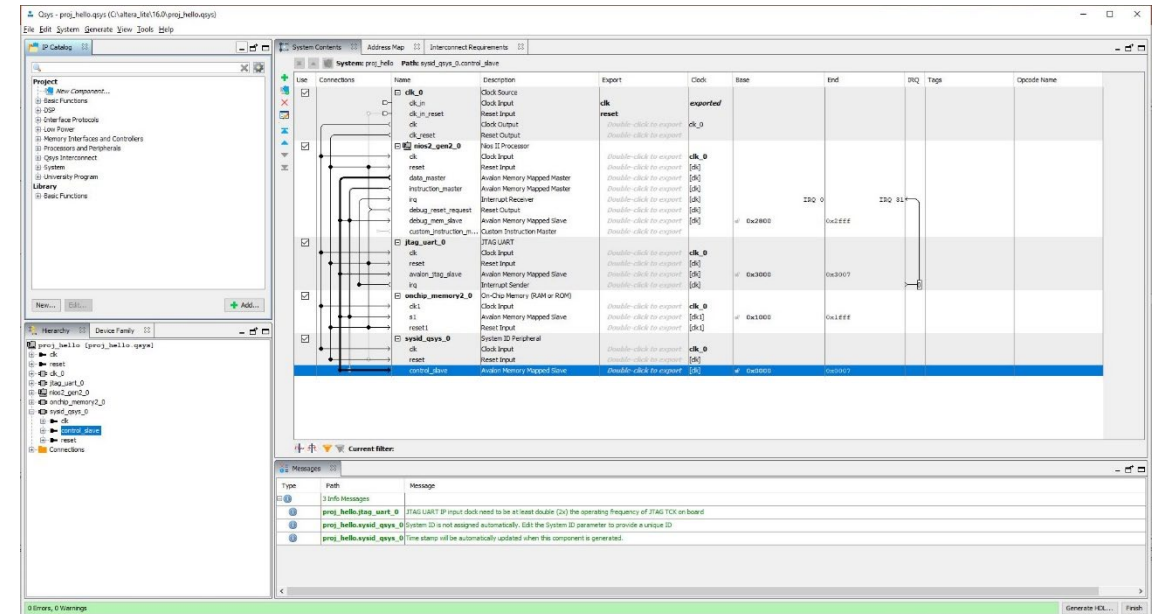
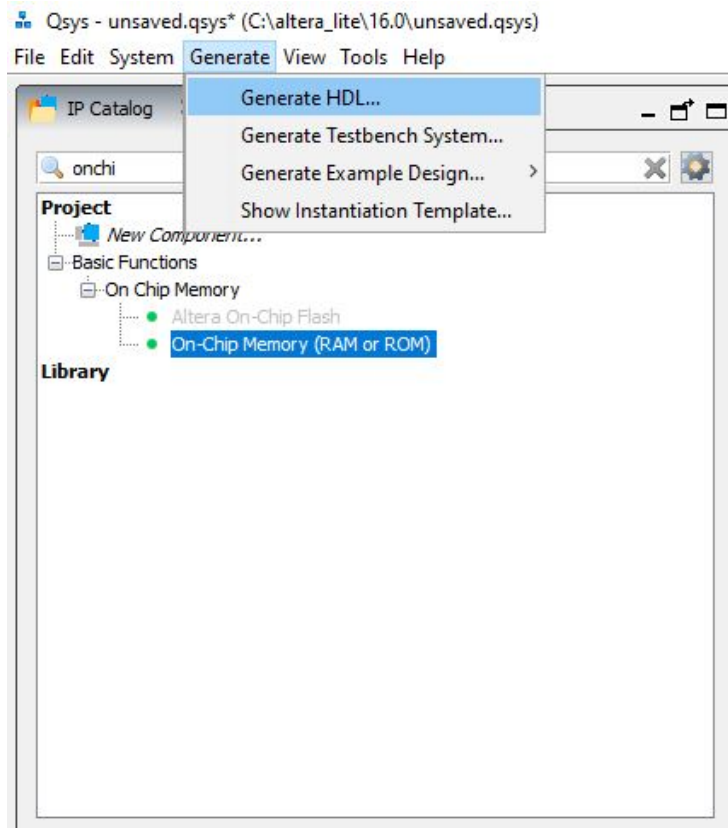
Generate HDL... Finish

Adding system ID



Use	Connections	Name	Description
<input checked="" type="checkbox"/>		clk_0 clk_in clk_in_reset clk clk_reset	Clock Source Clock Input Reset Input Clock Output Reset Output
<input checked="" type="checkbox"/>		nios2_gen2_0 clk reset data_master instruction_master irq debug_reset_request debug_mem_slave custom_instruction_m...	Nios II Processor Clock Input Reset Input Avalon Memory Mapped Master Avalon Memory Mapped Master Interrupt Receiver Reset Output Avalon Memory Mapped Slave Custom Instruction Master
<input checked="" type="checkbox"/>		jtag_uart_0 clk reset avalon_jtag_slave irq	JTAG UART Clock Input Reset Input Avalon Memory Mapped Slave Interrupt Sender
<input checked="" type="checkbox"/>		onchip_memory2_0 clk1 s1 reset1 s1	On-Chip Memory (RAM or ROM) Clock Input Avalon Memory Mapped Slave Reset Input
<input checked="" type="checkbox"/>		sysid_qsys_0 clk reset control_slave	System ID Peripheral Clock Input Reset Input Avalon Memory Mapped Slave

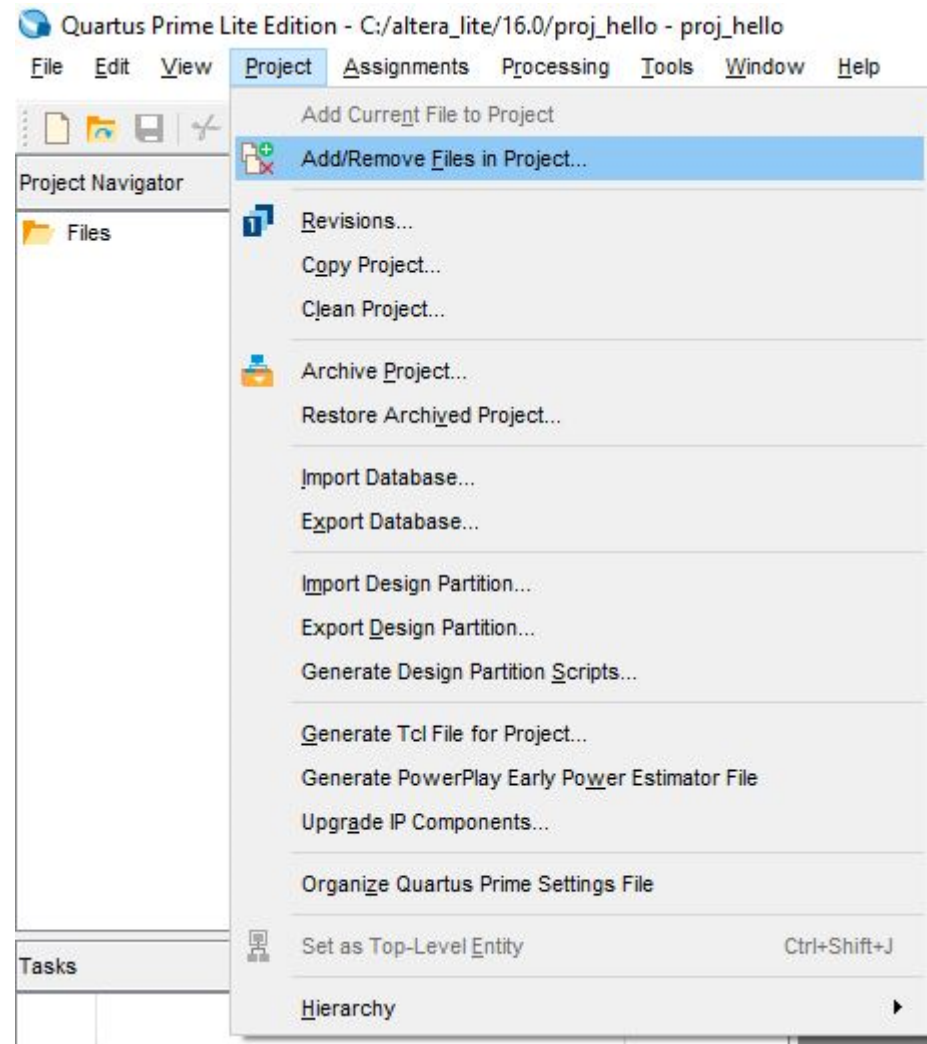
Generating HDL



Tutorial: Programming the FPGA

■ Back to Quartus Prime

- Add the QIP file to the project in Quartus, it contains the Verilog files generated by QSYS
- Now select Processing -> Start Analysis & Synthesis.
- A number of warnings will appear during the check. This is normal.



Quartus: Analysis & Synthesis

The screenshot displays the Quartus Prime Lite Edition software interface during the Analysis & Synthesis process. The main window is titled "Quartus Prime Lite Edition - C:/altera_lite/16.0/proj_hello - proj_hello". The interface is divided into several panes:

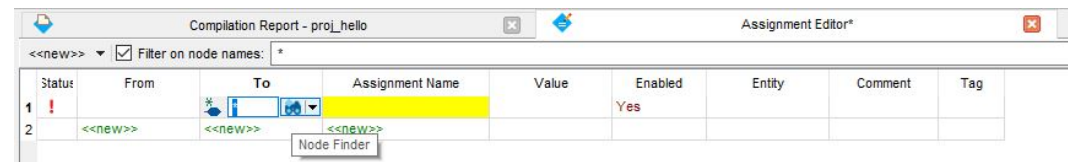
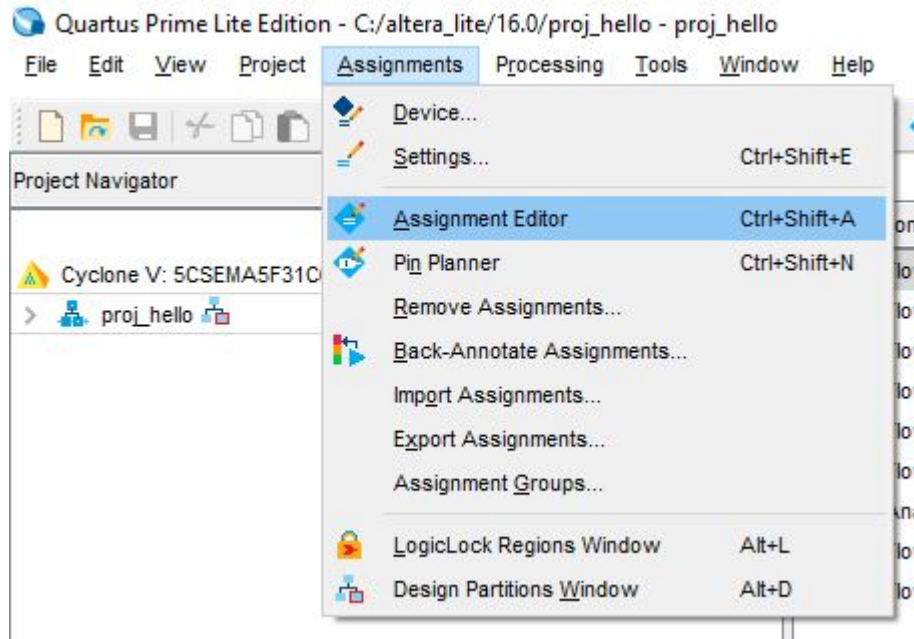
- Project Navigator:** Shows the project hierarchy with "Cyclone V: 5CSEMA5F31C6" and "proj_hello".
- Table of Contents:** Lists the project files, including "Flow Summary", "Flow Settings", "Flow Non-Default Global Settings", "Flow Elapsed Time", "Flow OS Summary", "Flow Log", "Analysis & Synthesis", "Flow Messages", and "Flow Suppressed Messages".
- Flow Summary:** Displays the current status of the Analysis & Synthesis process. It shows "Flow Status" as "In progress - Wed Dec 09 16:32:51 2020", "Quartus Prime Version" as "16.0.0 Build 211 04/27/2016 SJ Lite Edition", "Revision Name" as "proj_hello", "Top-level Entity Name" as "proj_hello", and "Family" as "Cyclone V".
- Tasks:** A table showing the progress of various tasks. The "Analysis & Synthesis" task is highlighted with a green progress bar and a time of 00:00:11.
- Messages:** A list of messages generated during the process, including "12128 Elaborating entity 'proj_hello_irq_mapper' for hierarchy 'proj_hello_irq_mapper:irq_mapper'", "12128 Elaborating entity 'altera_reset_controller' for hierarchy 'altera_reset_controller:rst_controller'", "12128 Elaborating entity 'altera_reset_synchronizer' for hierarchy 'altera_reset_controller:rst_controller|altera_reset_synchronizer:alt_rst_sync_uq1'", "12128 Elaborating entity 'altera_reset_synchronizer' for hierarchy 'altera_reset_controller:rst_controller|altera_reset_synchronizer:alt_rst_req_sync_uq1'", "11170 Start IP generation for the debug fabric within sld_hub.", "11172 2020.12.09.16:33:06 Progress: Loading sld32f20633/alt_sld_fab_wrapper_hw.tcl", "11172 Alt_sld_fab.alt_sld_fab: SLD fabric agents which did not specify prefer_host were connected to JTAG", and "11172 Alt_sld_fab: Generating alt_sld_fab 'alt_sld_fab' for QUARTUS_SYNTH".

The status bar at the bottom indicates "40%" completion and "00:00:18" remaining time.

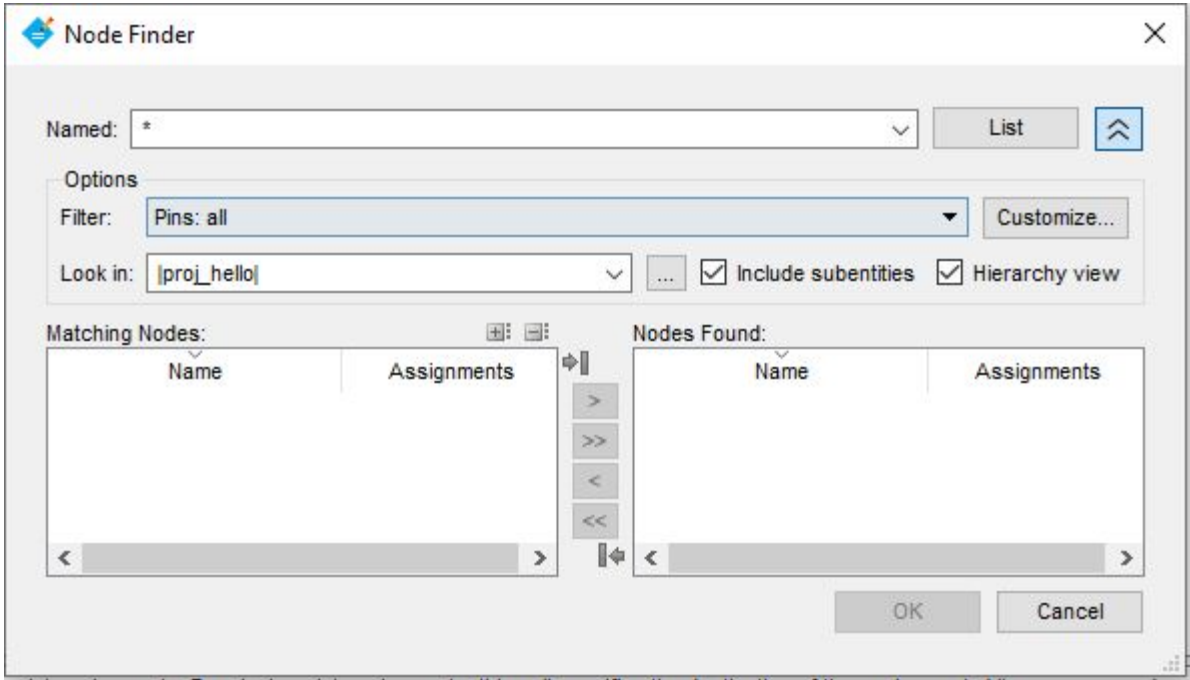
Assigning CLK and Reset Pins

- The pins assignments can be done using Assignment Editor in Assignments -> Assignment Editor
- Find the entry corresponding to the clock, assign PIN_AF14 to it. doing so will connect the clock in our design to the 50 MHz oscillator on the DE1-SoC board.
- Now assign the reset input signal to any of the SW[x] pins. This will connect the reset signal to one of the switches found on the DE1-SoC board.
- Now select Processing -> Start Compilation. If compilation is successful, a programming file to be written to the FPGA will be generated.

Assigning CLK and Reset Pins



Assigning CLK and Reset Pins



<<new>> <input checked="" type="checkbox"/> Filter on node names: *									
Status	From	To	Assignment Name	Value	Enabled	Entity	Comment	Tag	
1 ✓		in clk_clk	Location	PIN_AF14	Yes				
2 ✓		in reset_reset_n	Location	PIN_AB12	Yes				
3	<<new>>	<<new>>	<<new>>						

Compiling

Quartus Prime Lite Edition - C:/altera_lite/16.0/proj_hello - proj_hello

File Edit View Project Assignments Processing Tools Window Help

Search altera.com

Project Navigator

Entity/Instance

Cyclone V: SCSEMA5F31C6

proj_hello

Table of Contents

- Flow Summary
- Flow Settings
- Flow Non-Default Global Settings
- Flow Elapsed Time
- Flow OS Summary
- Flow Log
- Analysis & Synthesis
- Fitter
- Flow Messages
- Flow Suppressed Messages

Flow Summary

Flow Status: In progress - Wed Dec 09 17:12:01 2020

Quartus Prime Version: 16.0.0 Build 211 04/27/2016 SJ Lite Edition

Revision Name: proj_hello

Top-level Entity Name: proj_hello

Family: Cyclone V

Device: SCSEMA5F31C6

Timing Models: Final

Logic utilization (in ALMs): N/A

Total registers: 868

Total pins: 2

Total virtual pins: 0

Total block memory bits: 44,032

Total DSP blocks: 0

Total HSSI RX PCSs: 0

Total HSSI PMA RX Deserializers: 0

Total HSSI TX PCSs: 0

Total HSSI PMA TX Serializers: 0

Total PLLs: 0

Total DLLs: 0

Tasks

Compilation

Task	Time
27% Compile Design	00:00:48
> Analysis & Synthesis	00:00:27
5% Fitter (Place & Route)	00:00:21
0% Assembler (Generate programming files)	00:00:00
0% TimeQuest Timing Analysis	00:00:00
0% EDA Netlist Writer	00:00:00
Edit Settings	
Program Device (Open Programmer)	

Messages

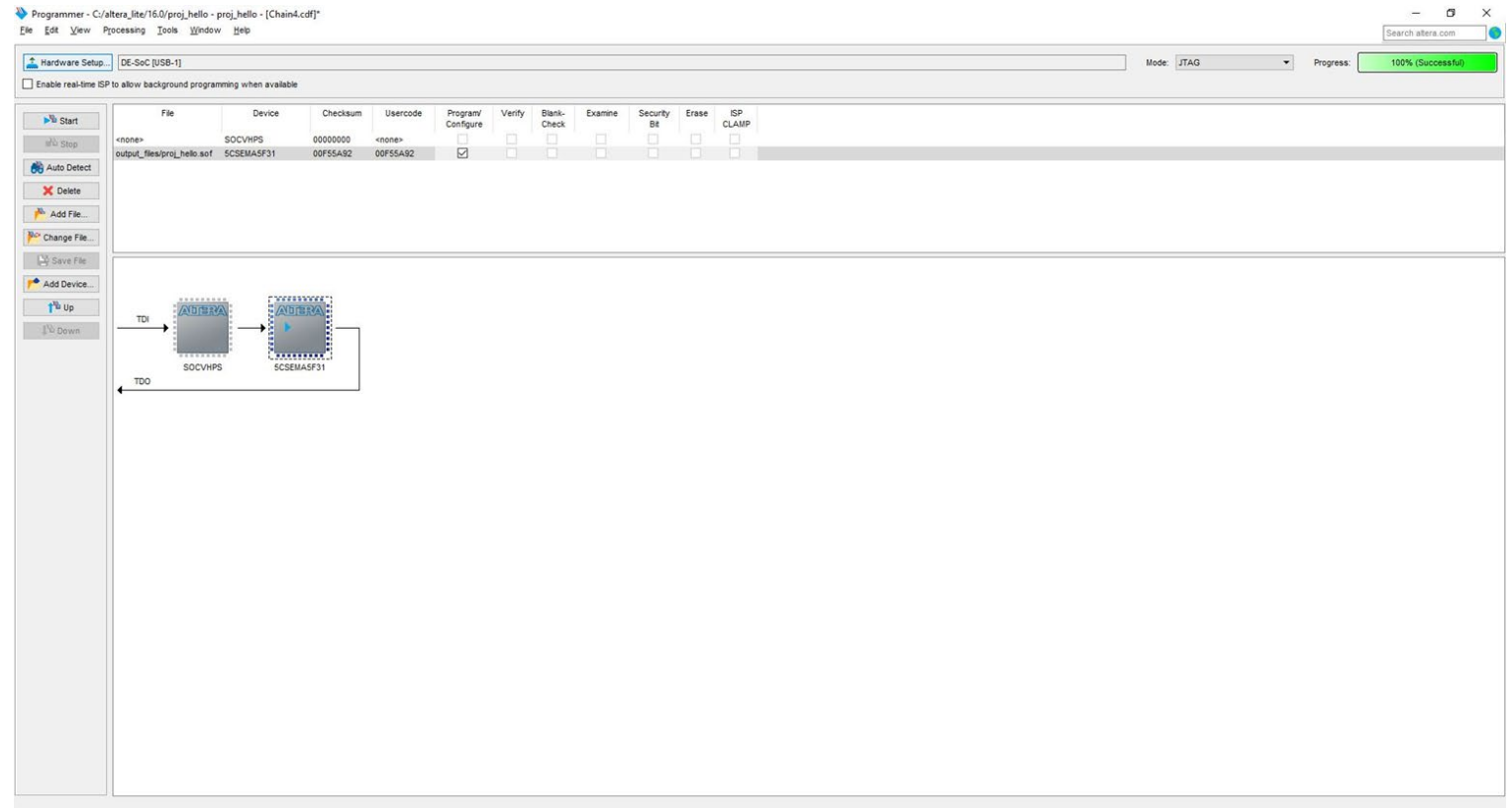
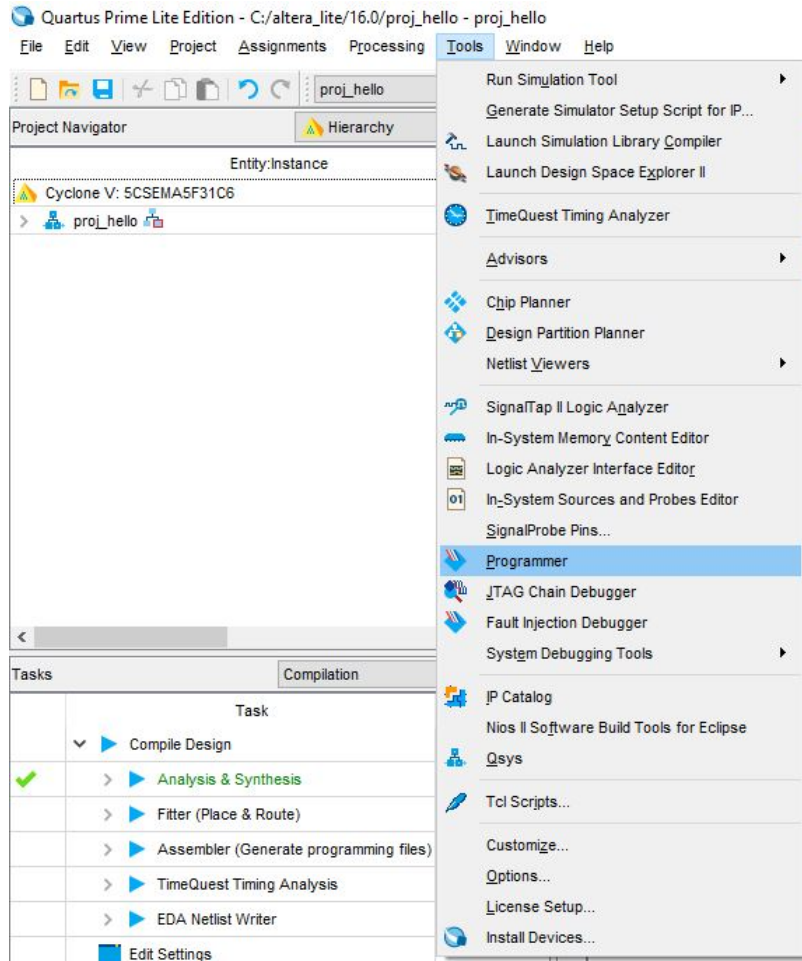
System (9) Processing (205)

27% 00:00:49

Programming the FPGA

- Select Tools -> Programmer. Now, select Auto detect, a new dialogue box opens up, choose “5CSEMA5”, you can find two entries, Right click on the 5CSEMA5 entry, change the file to the target SOF file. Be sure that DE1 SoC is connected to the computer via the provided USB cable.

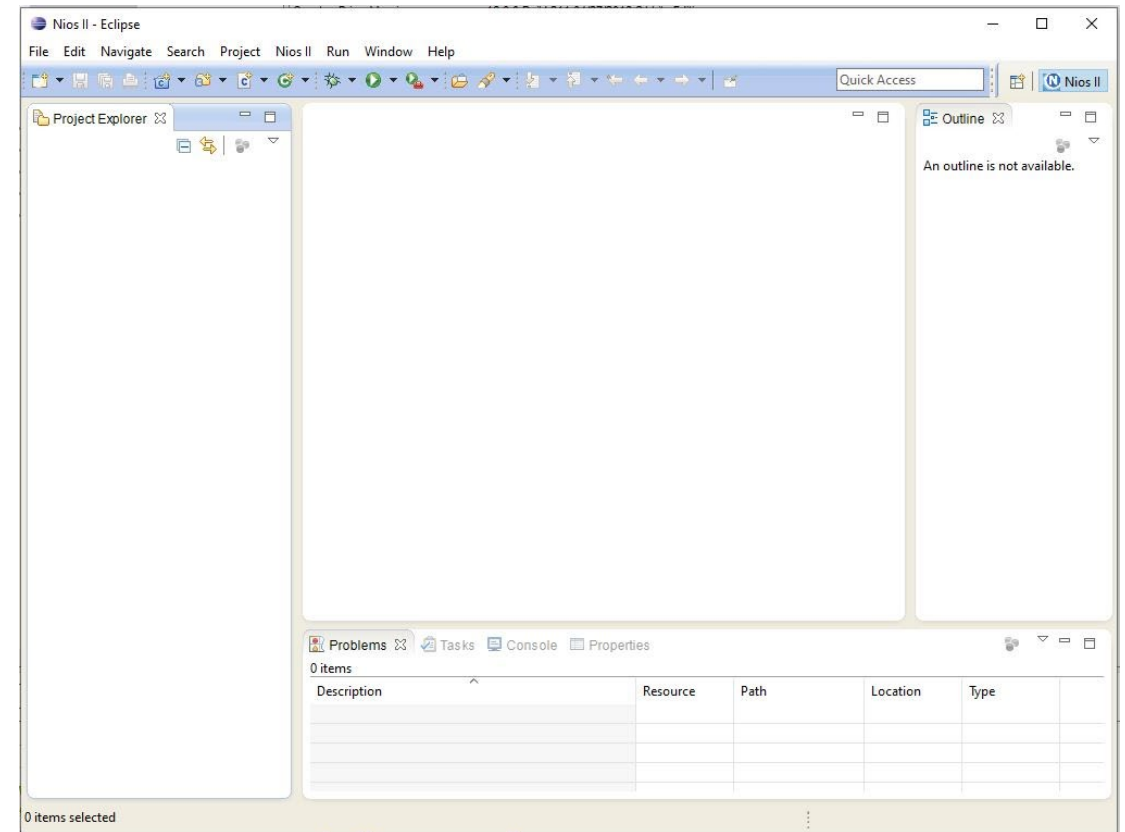
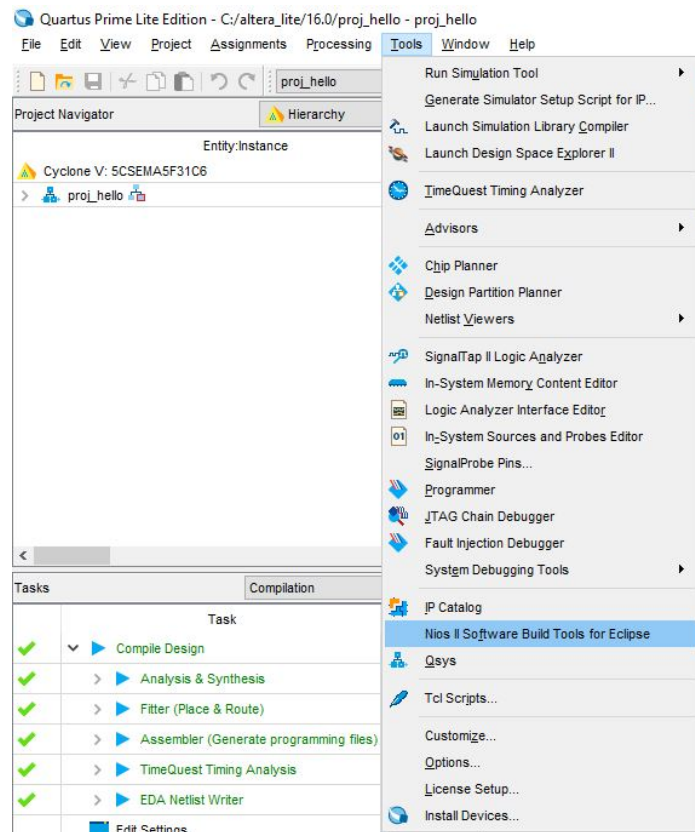
Programming the FPGA



Tutorial: Using the NIOS II IDE

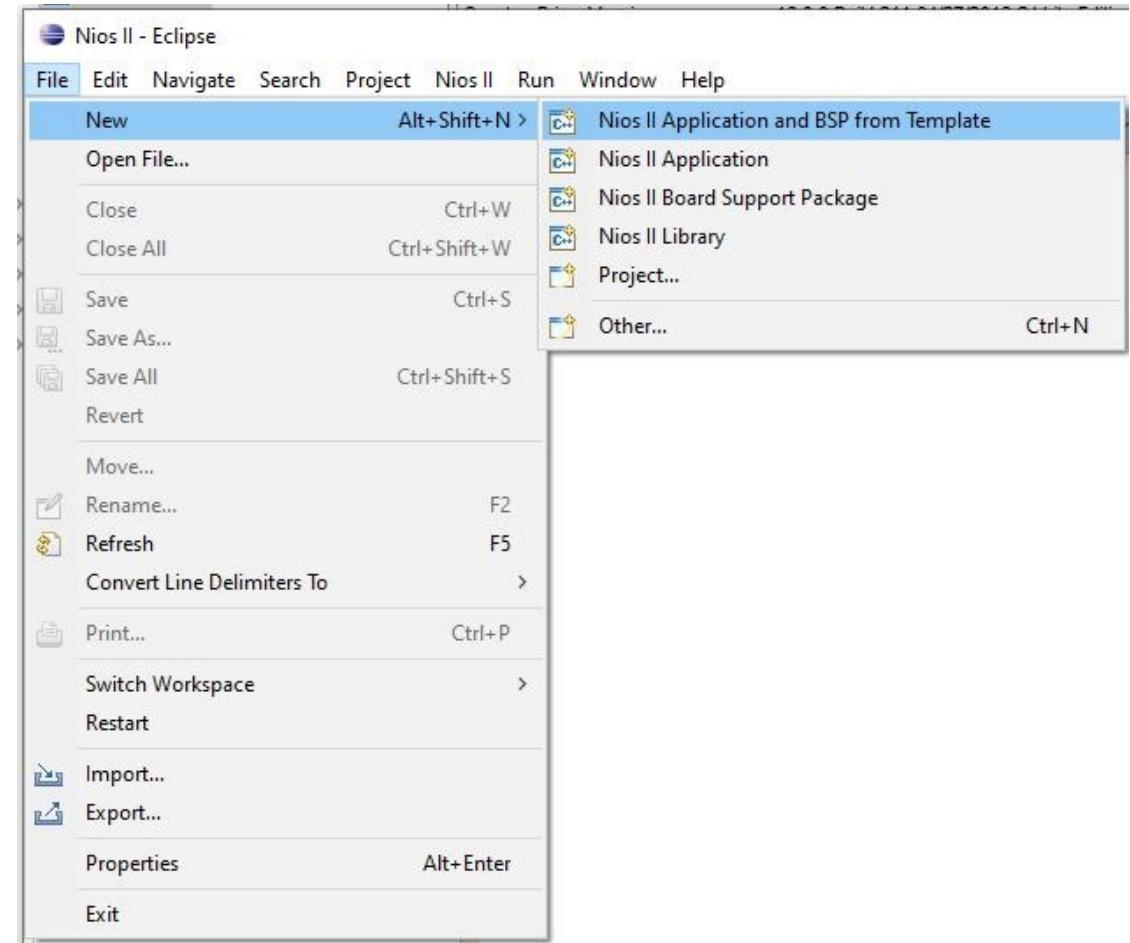
- Now that you have successfully developed an QSYS system, we will write a very simple program to run on our new processor.
- Select Tools -> NIOS II Software Build Tools for Eclipse.
- Create a new workspace. Make sure that there are no spaces in path directory names.
- Disable Anti-Virus for NIOS to detect connected board
- Make sure that your reset switch is logic HIGH (Reset Input is active when it is low)

Tutorial: Using the NIOS II IDE

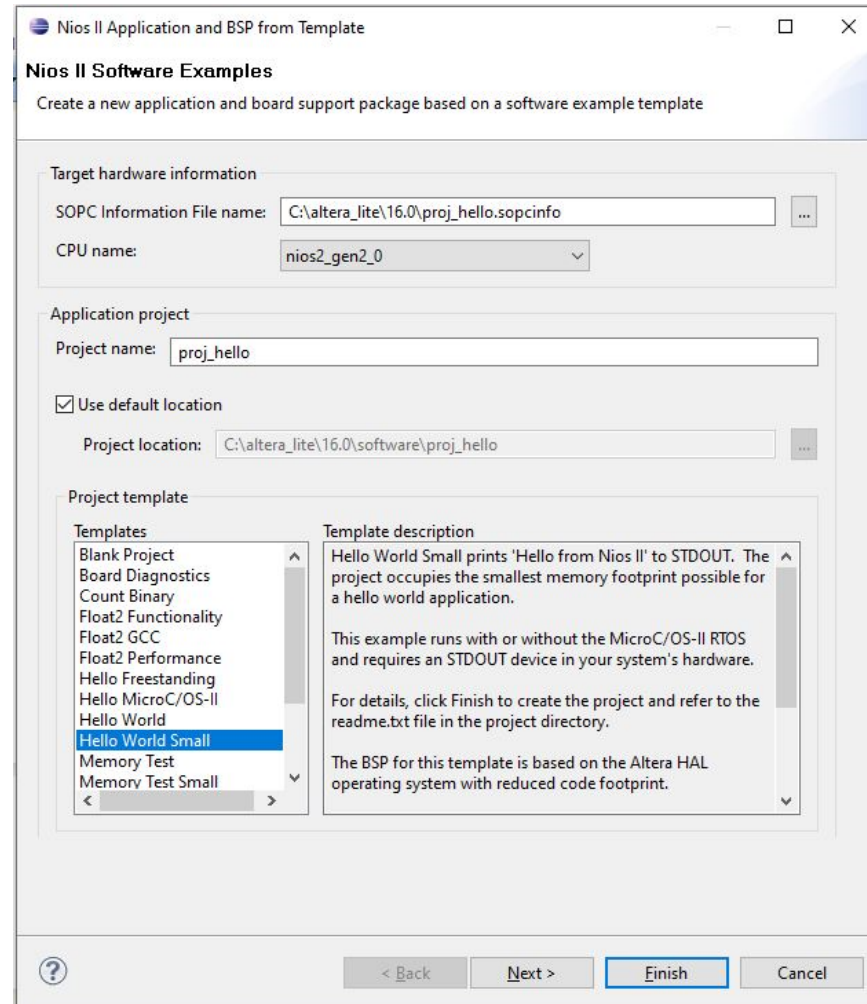


Tutorial: Using the NIOS II IDE

- Select File -> New -> NIOS II Application and BSP from template. A new dialogue box should open.
- A variety of project templates are provided as a starting point. We will be using the “Hello World Small” template.
- In order to develop a NIOS project, the IDE needs a .sopcinfo file that indicates various peripherals unique to our design.

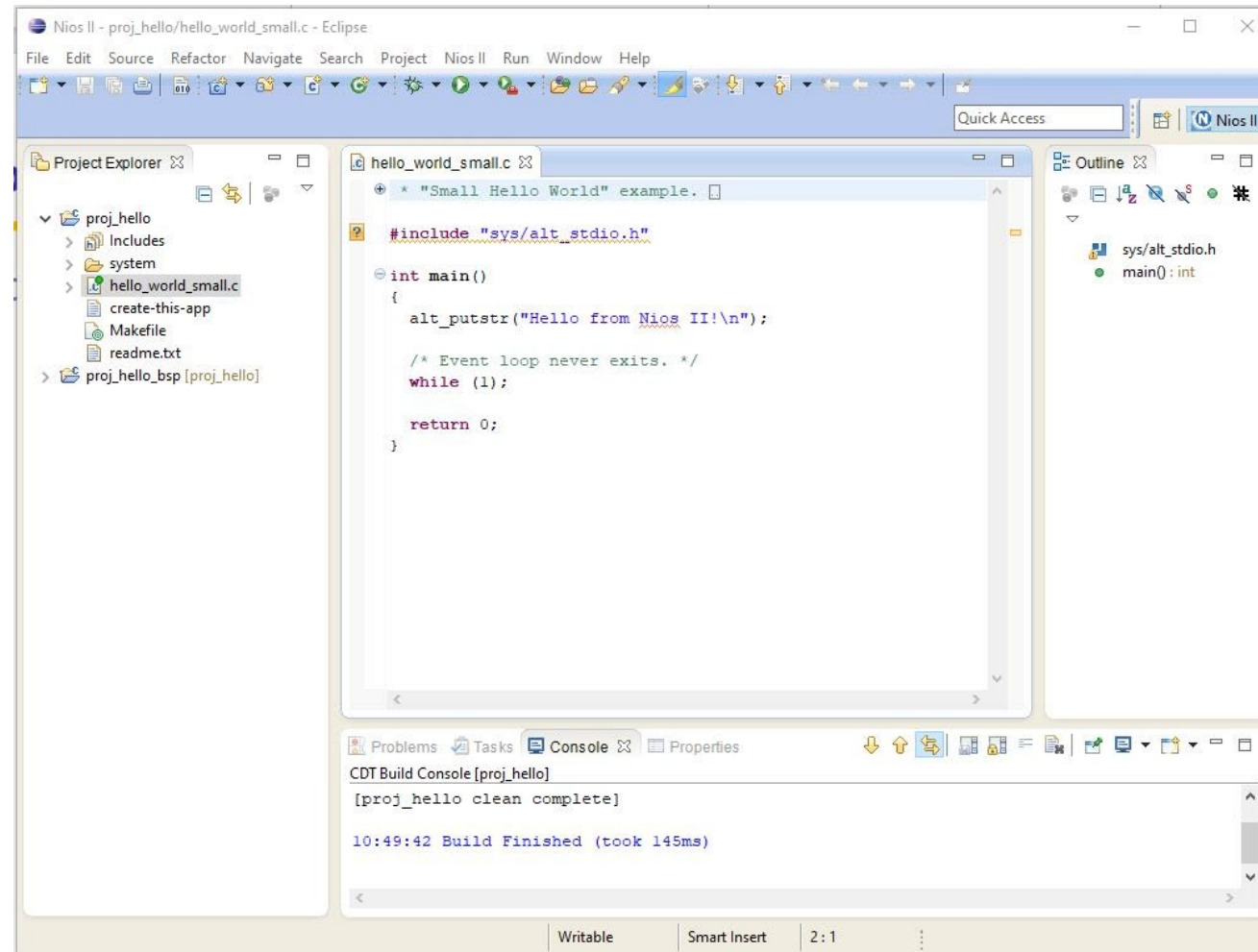


Tutorial: Using the NIOS II IDE



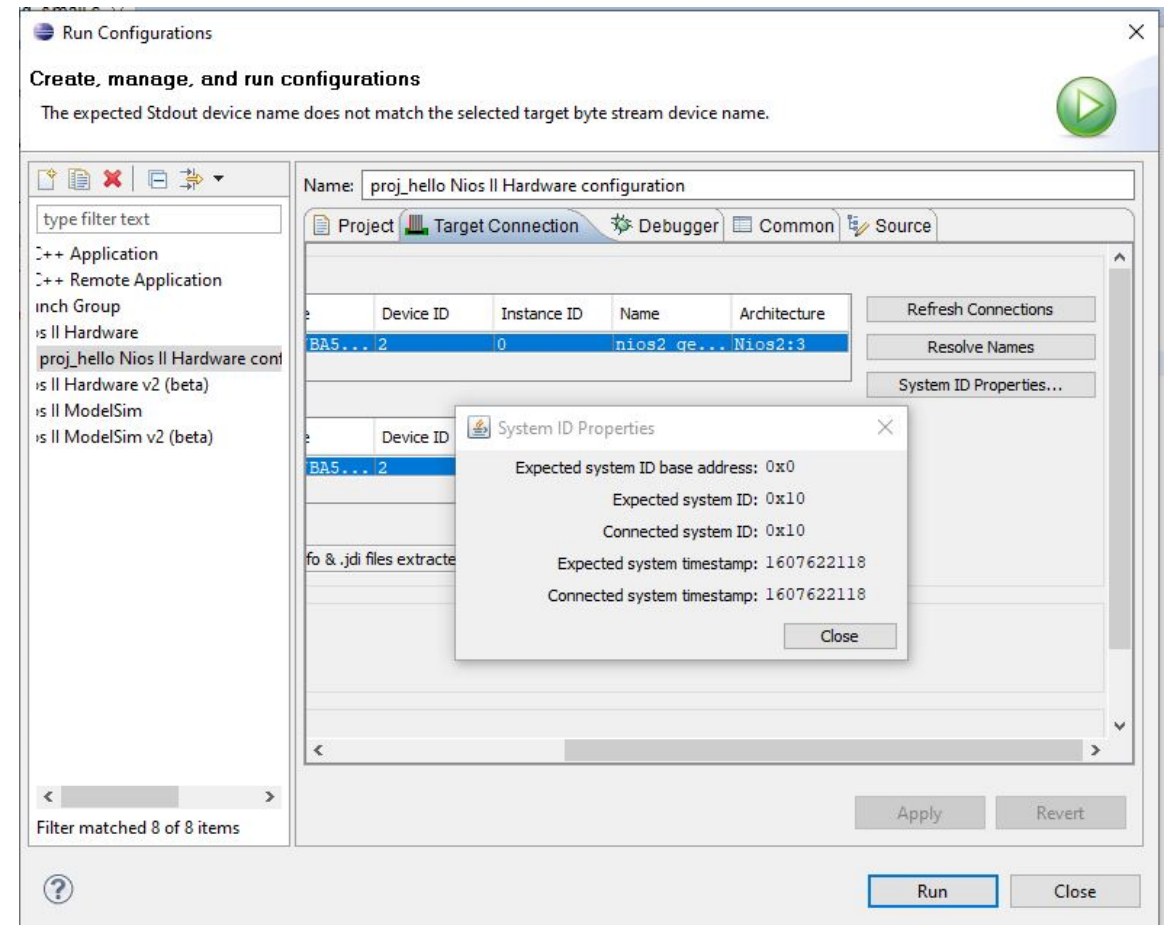
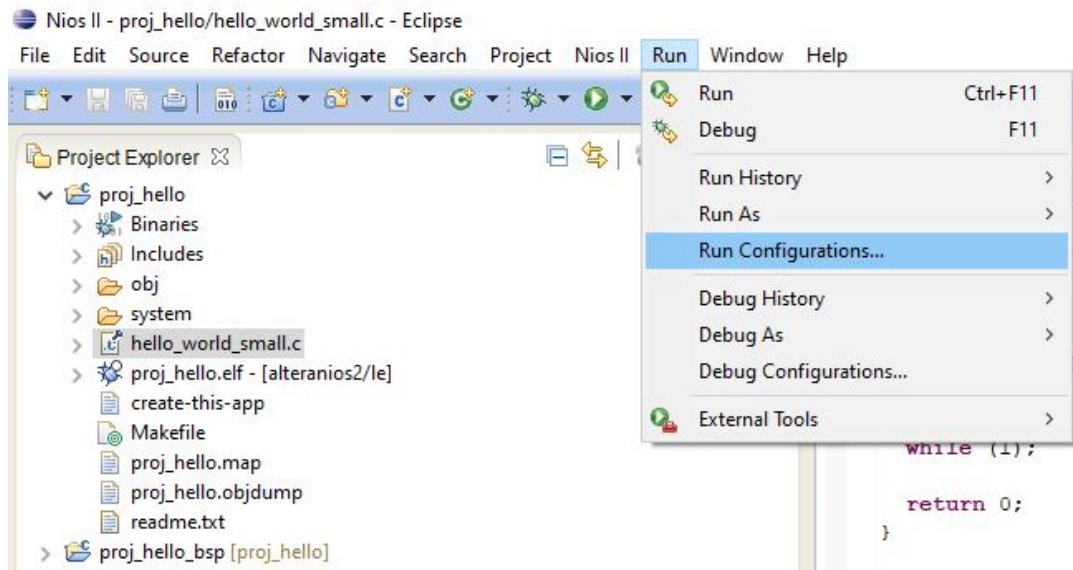
Tutorial: Using the NIOS II IDE

- You should now be looking at a window like this:



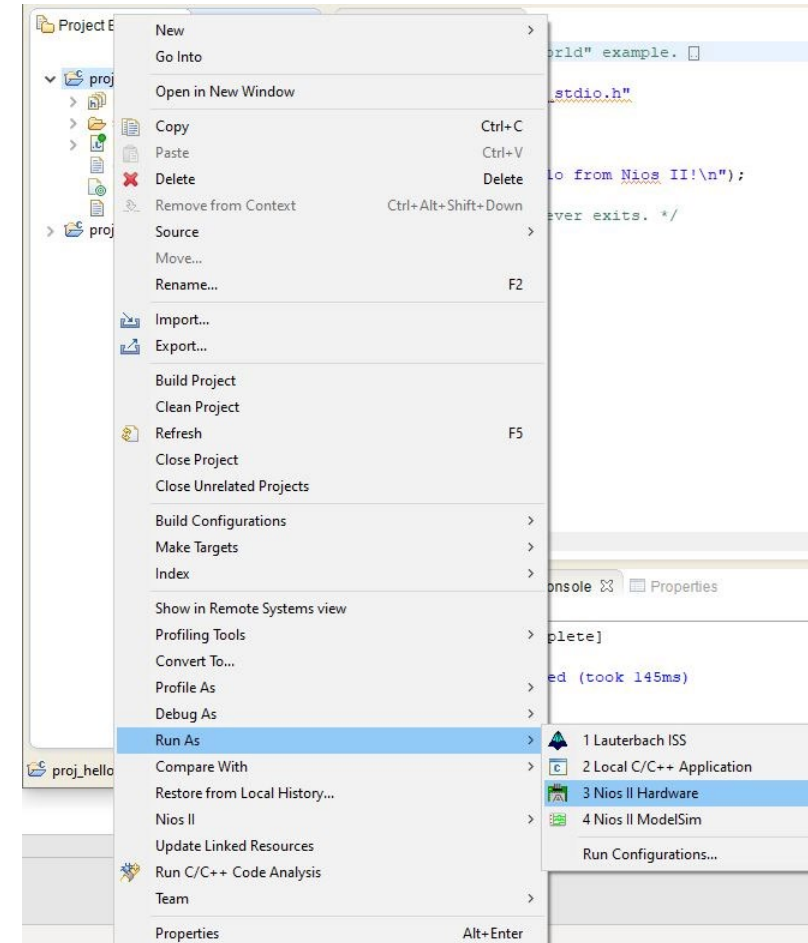
Tutorial: Using the NIOS II IDE

- Check expected and connected system id are same:

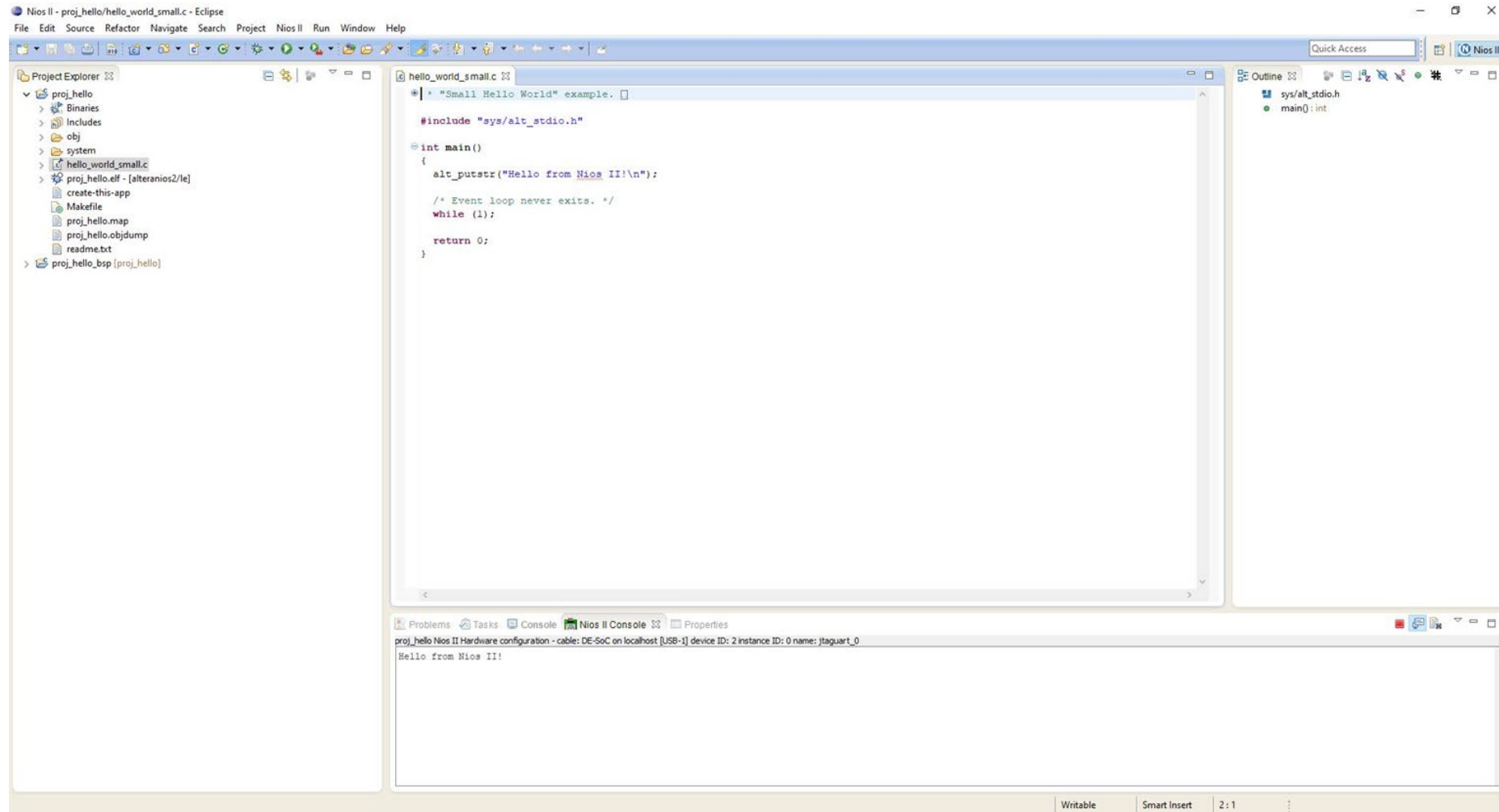


Tutorial: Using the NIOS II IDE

- Under the “Project Explorer” tab, right-click on the application. This time select Run As -> NIOS II Hardware.
- This option will compile and write the program to the on-chip memory we specified in QSYS.



Hello From NIOS II!



Checkpoint: Lab1 (Part I)

- A NIOS system in the Quartus Prime QSYS
- Use the NIOS II IDE to run a very simple C program on the system defined in QSYS.

Part II

- You will use external memory
- You will use other devices (LED, seven segment, and hex display.)
- Please read lab instructions on class website

Getting Started with Part II (QSYS)

- Add the SDRAM PLL to drive the system
- Add the SDRAM as the program memory
- Add the required PIOs and name them appropriately

Qsys - count_bin.qsys (C:\Users\ECS-ECELAB23\Documents\ECE354_redesign\count_bin\count_bin.qsys)

File Edit System Generate View Tools Help

System Contents Address Map Interconnect Requirements

System: count_bin Path: sdr_pll

Use	Connections	Name	Description	Export	Clock	Base	End	IRQ	Tags	Opcode Name
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	sdr_pll	System and SDRAM Clocks for DE-ser...							
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	ref_clk	Clock Input	sdr_pll_ref_clk	exported					
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	ref_reset	Reset Input	sdr_pll_ref_reset						
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	sys_clk	Clock Output							
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	sdram_clk	Clock Output	sdram_clk						
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	reset_source	Reset Output							
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	nios_cpu	Nios II Processor							
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	clk	Clock Input							
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	reset	Reset Input							
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	data_master	Avalon Memory Mapped Master							
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	instruction_master	Avalon Memory Mapped Master							
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	irq	Interrupt Receiver							
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	debug_reset_request	Reset Output							
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	debug_mem_slave	Avalon Memory Mapped Slave							
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	custom_instruction_m...	Custom Instruction Master							
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	SDRAM	SDRAM Controller							
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	clk	Clock Input							
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	reset	Reset Input							
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	s1	Avalon Memory Mapped Slave							
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	wire	Conduit							
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	jtag_uart	JTAG UART							
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	clk	Clock Input							
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	reset	Reset Input							
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	avalon_jtag_slave	Avalon Memory Mapped Slave							
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	irq	Interrupt Sender							
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	timer	Interval Timer							
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	clk	Clock Input							
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	reset	Reset Input							
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	s1	Avalon Memory Mapped Slave							
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	irq	Interrupt Sender							
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	button_pio	PIO (Parallel I/O)							
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	clk	Clock Input							
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	reset	Reset Input							

Current filter:

Messages

Type	Path	Message
2 Info Messages		
count_bin.button_pio		PIO inputs are not hardwired in test bench. Undefined values will be read from PIO inputs during simulation.
count_bin.jtag_uart		JTAG UART IP input clock need to be at least double (2x) the operating frequency of JTAG TCK on board. PIO inputs are not hardwired in test bench. Undefined values will be read from PIO inputs during simulation.

0 Errors, 0 Warnings

Generate HDL... Finish

Pin assignments viewed from Pin Planner

Pin Planner - C:/Users/ECS-ECELAB23/Documents/ECE354_redesign/count_bin/count_bin - count_bin

File Edit View Processing Tools Window Help

Report

Report not available

Groups Report

Tasks

- Early Pin Planning
 - Early Pin Planning...
 - Run IO Assignment Analysis
 - Export Pin Assignments...
- Highlight Pins
 - IO Banks
 - VREF Groups

Top View - Wire Bond
Cyclone V - 5C5EMAS5F31C6

Named

Node Name	Direction	Location	IO Bank	VREF Group	Filter Location	IO Standard	Reserved	Current Strength	Slew Rate	Differential Pair	ver Analog Settings	_GXB/VCCCT_GXB \	ceiver IO Pin Term	Dedicated Refclk Pi	Common Mode Dri	mitter Slew Rate C	sr Differential Outp
CLOCK_50	Input	PN_AF14	3B	B3B_NO	PN_AF14	2.5 V		12mA (default)									
DRAM_ADDR[12]	Output	PN_AJ14	3B	B3B_NO	PN_AJ14	2.5 V		12mA (default)	1 (default)								
DRAM_ADDR[11]	Output	PN_AH13	3B	B3B_NO	PN_AH13	2.5 V		12mA (default)	1 (default)								
DRAM_ADDR[10]	Output	PN_AG12	3B	B3B_NO	PN_AG12	2.5 V		12mA (default)	1 (default)								
DRAM_ADDR[9]	Output	PN_AG13	3B	B3B_NO	PN_AG13	2.5 V		12mA (default)	1 (default)								
DRAM_ADDR[8]	Output	PN_AH15	3B	B3B_NO	PN_AH15	2.5 V		12mA (default)	1 (default)								
DRAM_ADDR[7]	Output	PN_AF15	3B	B3B_NO	PN_AF15	2.5 V		12mA (default)	1 (default)								
DRAM_ADDR[6]	Output	PN_AD14	3B	B3B_NO	PN_AD14	2.5 V		12mA (default)	1 (default)								
DRAM_ADDR[5]	Output	PN_AC14	3B	B3B_NO	PN_AC14	2.5 V		12mA (default)	1 (default)								
DRAM_ADDR[4]	Output	PN_AB15	3B	B3B_NO	PN_AB15	2.5 V		12mA (default)	1 (default)								
DRAM_ADDR[3]	Output	PN_AE14	3B	B3B_NO	PN_AE14	2.5 V		12mA (default)	1 (default)								
DRAM_ADDR[2]	Output	PN_AG15	3B	B3B_NO	PN_AG15	2.5 V		12mA (default)	1 (default)								
DRAM_ADDR[1]	Output	PN_AH14	3B	B3B_NO	PN_AH14	2.5 V		12mA (default)	1 (default)								
DRAM_ADDR[0]	Output	PN_AK14	3B	B3B_NO	PN_AK14	2.5 V		12mA (default)	1 (default)								
DRAM_BA[1]	Output	PN_AJ12	3B	B3B_NO	PN_AJ12	2.5 V		12mA (default)	1 (default)								
DRAM_BA[0]	Output	PN_AF13	3B	B3B_NO	PN_AF13	2.5 V		12mA (default)	1 (default)								
DRAM_CAS_N	Output	PN_AF11	3B	B3B_NO	PN_AF11	2.5 V		12mA (default)	1 (default)								
DRAM_CKE	Output	PN_AK13	3B	B3B_NO	PN_AK13	2.5 V		12mA (default)	1 (default)								
DRAM_CLK	Output	PN_AH12	3B	B3B_NO	PN_AH12	2.5 V		12mA (default)	1 (default)								
DRAM_CS_N	Output	PN_AG11	3B	B3B_NO	PN_AG11	2.5 V		12mA (default)	1 (default)								
DRAM_DQ[15]	Bidir	PN_AJ5	3B	B3B_NO	PN_AJ5	2.5 V		12mA (default)	1 (default)								
DRAM_DQ[14]	Bidir	PN_AJ6	3B	B3B_NO	PN_AJ6	2.5 V		12mA (default)	1 (default)								
DRAM_DQ[13]	Bidir	PN_AH7	3B	B3B_NO	PN_AH7	2.5 V		12mA (default)	1 (default)								
DRAM_DQ[12]	Bidir	PN_AH8	3B	B3B_NO	PN_AH8	2.5 V		12mA (default)	1 (default)								
DRAM_DQ[11]	Bidir	PN_AH9	3B	B3B_NO	PN_AH9	2.5 V		12mA (default)	1 (default)								
DRAM_DQ[10]	Bidir	PN_AJ9	3B	B3B_NO	PN_AJ9	2.5 V		12mA (default)	1 (default)								
DRAM_DQ[9]	Bidir	PN_AJ10	3B	B3B_NO	PN_AJ10	2.5 V		12mA (default)	1 (default)								
DRAM_DQ[8]	Bidir	PN_AH10	3B	B3B_NO	PN_AH10	2.5 V		12mA (default)	1 (default)								
DRAM_DQ[7]	Bidir	PN_AJ11	3B	B3B_NO	PN_AJ11	2.5 V		12mA (default)	1 (default)								

Filter: Pins: all

0% 00:00:00

Questions