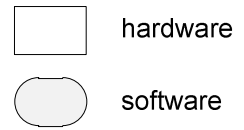
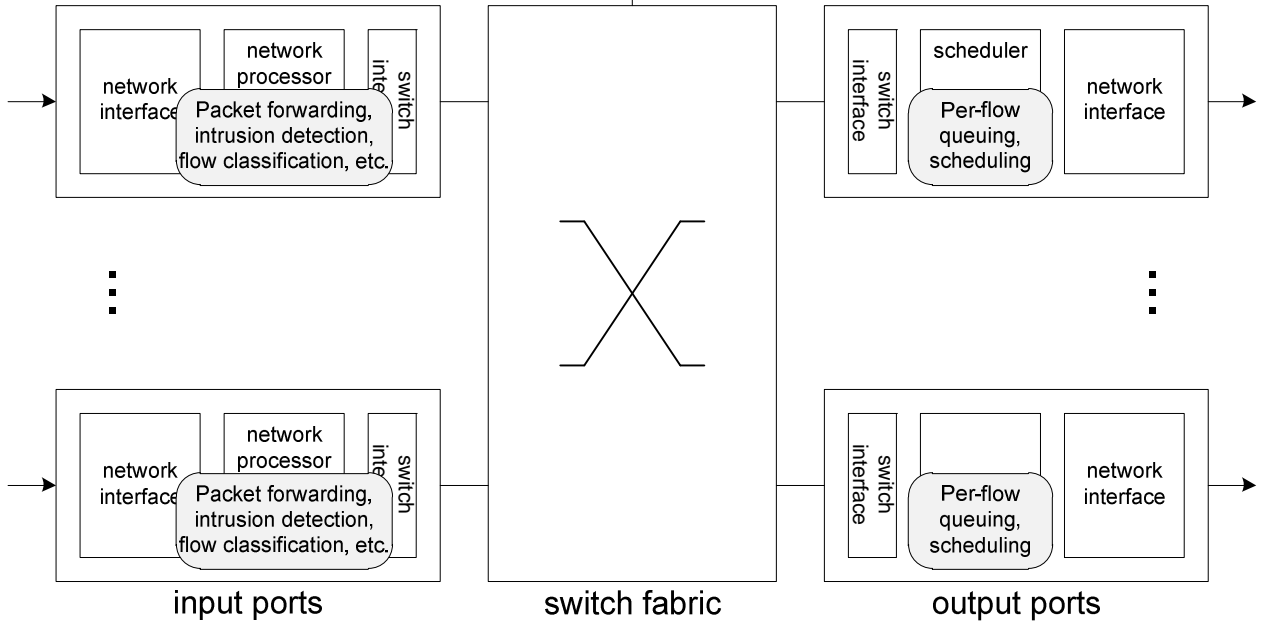


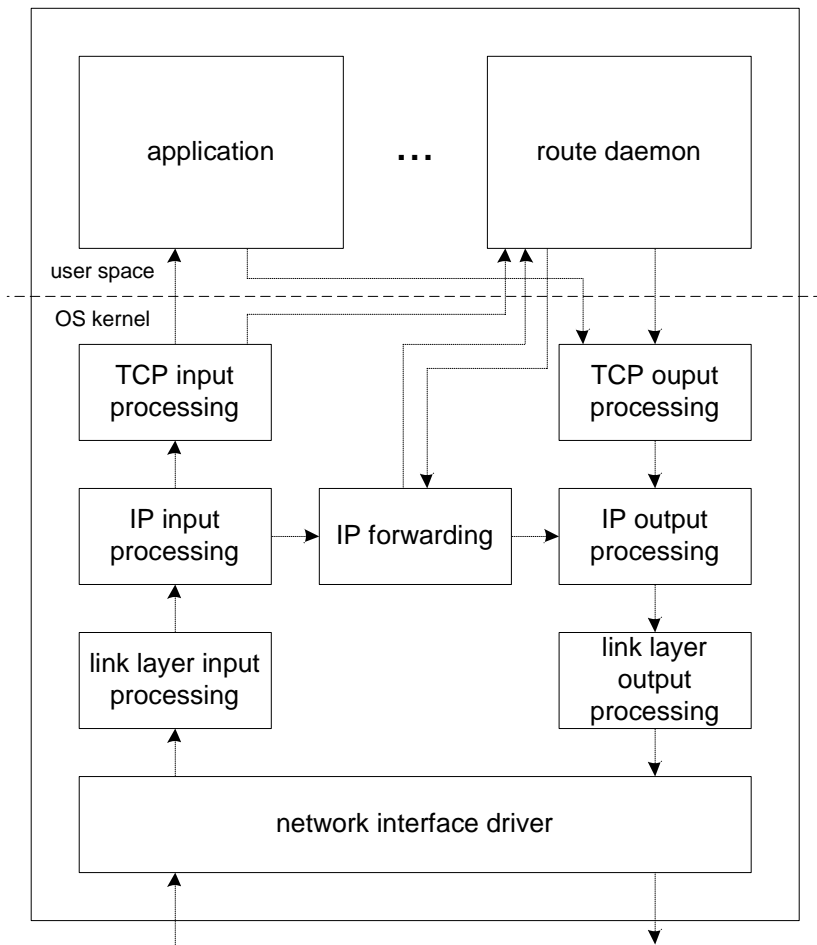
control processor



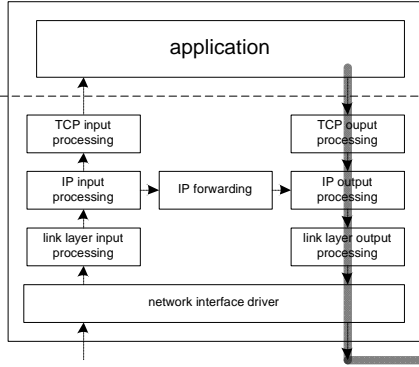
control plane

data plane

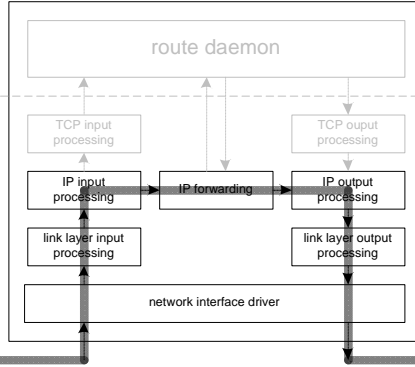




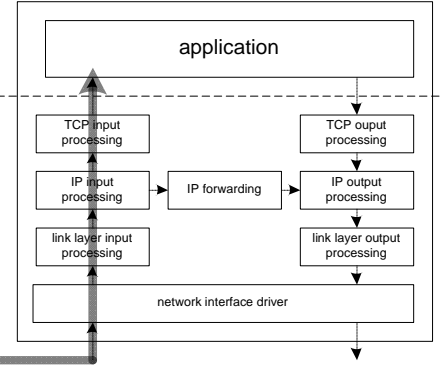
end-system

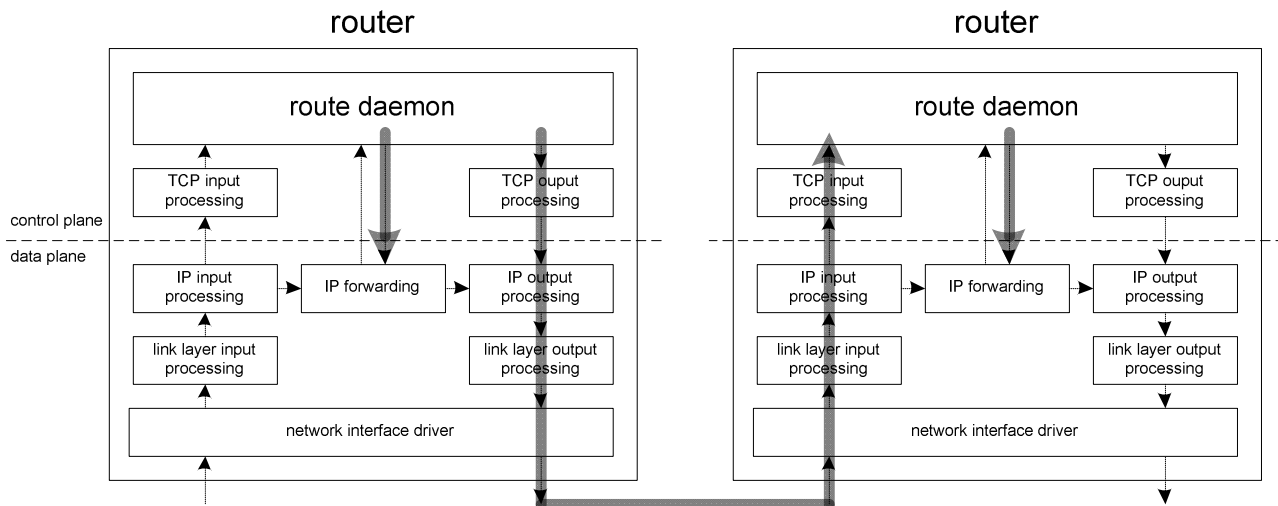


router

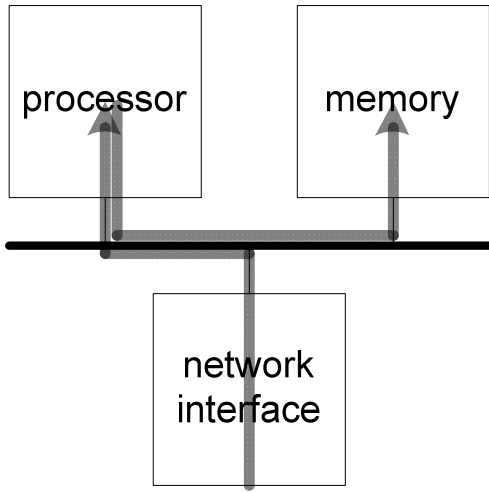


end-system

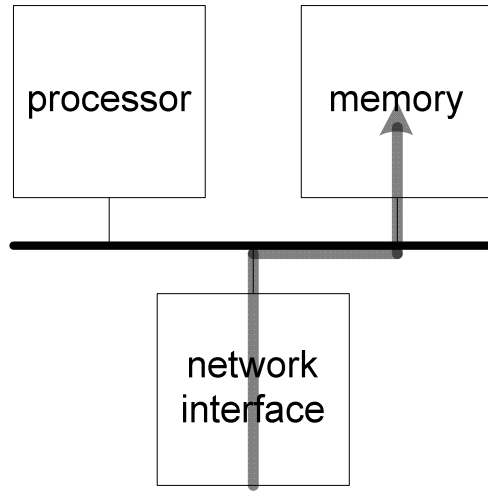


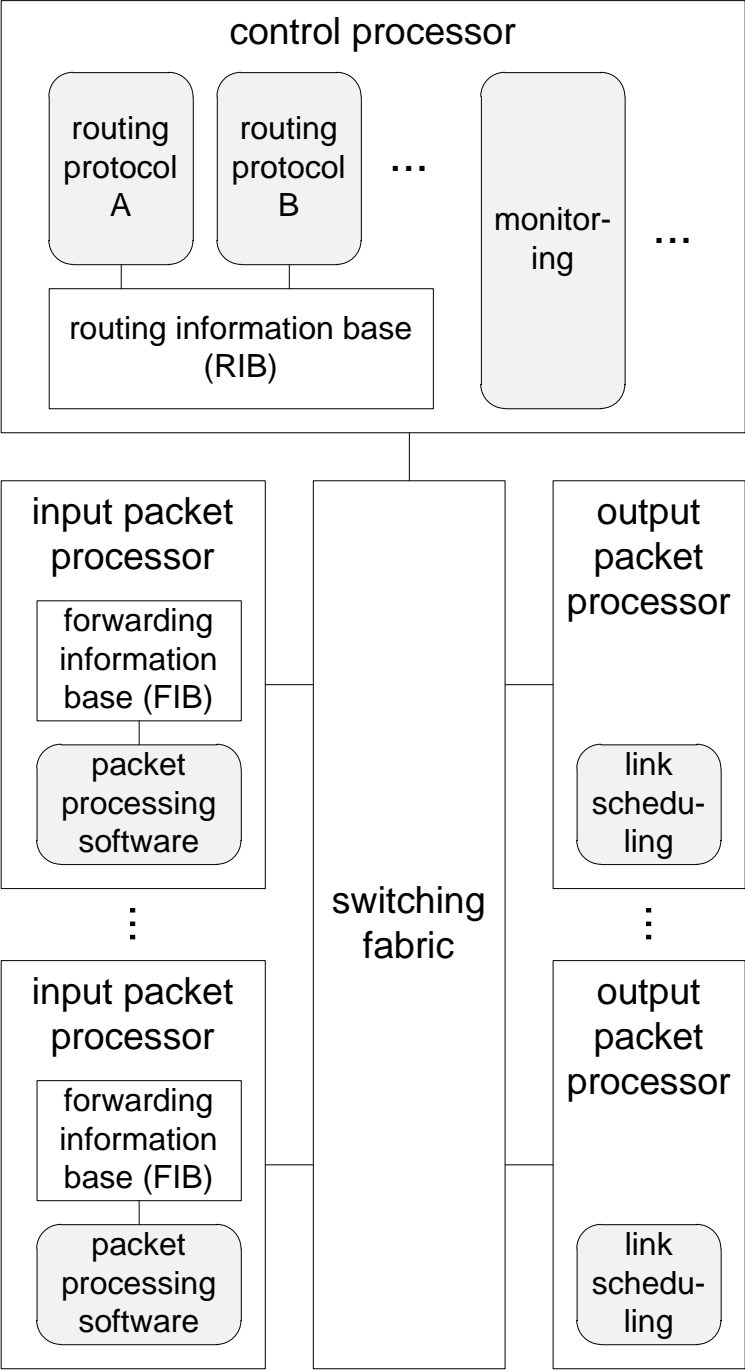


without DMA

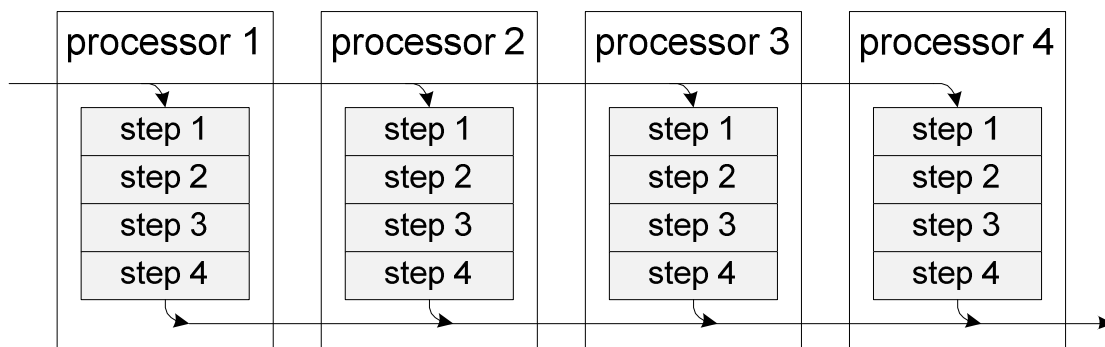


with DMA





Run-to-completion



Pipelining

