
ECE 697J – Advanced Topics in Computer Networks

Next Generation Network Processors

11/25/03

Overview

- Next generation NPs
 - What should they look like?
 - What are current bottlenecks?
 - What features would be nice?
 - What are limitations on scalability?
- Next generation IXA NPs
 - IXP2400
 - Other IXA NPs

Next Generation NPs

- What market will they be used in?
 - Where can NPs make money?
- What should they look like?
 - Architectural features?
- What are current bottlenecks?
 - Performance limitations
- What features would be nice?
 - What functions need hardware support
- What are limitations on scalability?

Performance Bottlenecks

- Memory
 - Increasing delay for off-chip memory
 - More on-chip memory
 - Bandwidth available, but access time too slow
- I/O
 - High-speed interfaces available
 - Cost problem with optical interfaces
 - Otherwise no problem
- Processing power
 - Individual cores are getting more complex
 - Problems with memory delay and access to shared resources
 - Control processor can become bottleneck

New NP Features

- Hardware support for
 - Flow classification
 - Crypto support
- Software
 - Simple programming environment (high-level abstractions)
 - Accurate simulator
 - Tools for testing
- NP start looking more and more like general-purpose workstation processors
 - Why not totally?
 - Heterogeneity of processors
 - Workload characteristics

NP Architectures

- How can processors be arranged on NP?
 - Consider heterogeneity of processing resources and workload
- Multiprocessor
 - Parallel processors with shared interconnect
 - Problems?
- Pipeline
 - Multiple processors per data path
 - Problems?
- Data Flow Architecture
 - Extreme form of pipelining
 - Problems?
- Heterogeneous Architectures

Limitations on Scalability

- What are the limitations on how fast NPs can get?
 - Parallelism in networks
 - Power consumption
 - Chip area
- What are the limitations on how fast NPs need to get?
 - Link rates (optical bandwidth limits)
 - Application complexity (core vs. edge)

Novel Areas of NP Use

- TCP/IP offloading on high-performance servers
- Security processing: SSL offloading
- Storage Area Networks
- More next class

New IXA NPs

- Different NPs for different markets
 - IXP2400 replacement for IXP1200
 - IXP2800 high-performance version
 - IXP2850 includes crypto co-processor
 - IXP425 low-end for access routers
- Configuration for market is crucial to make money
 - Still uniform architecture
 - Common software development tools

IXP2400

- XScale (ARM compliant) embedded control processor
 - Instruction and data caches
- 8 microengines
 - 400 or 600 MHz
- 8 threads per microengine
- Multiple instruction stores with 4k instructions
- 256 general purpose registers
- 512 transfer registers
- 2GB addressable DDR-DRAM memory (19.2 Gbps)
- 32MB addressable QDR-SRAM memory (12 Gbps r+w)
- 16 words of Next Neighbor Registers
- 16kB scratchpad

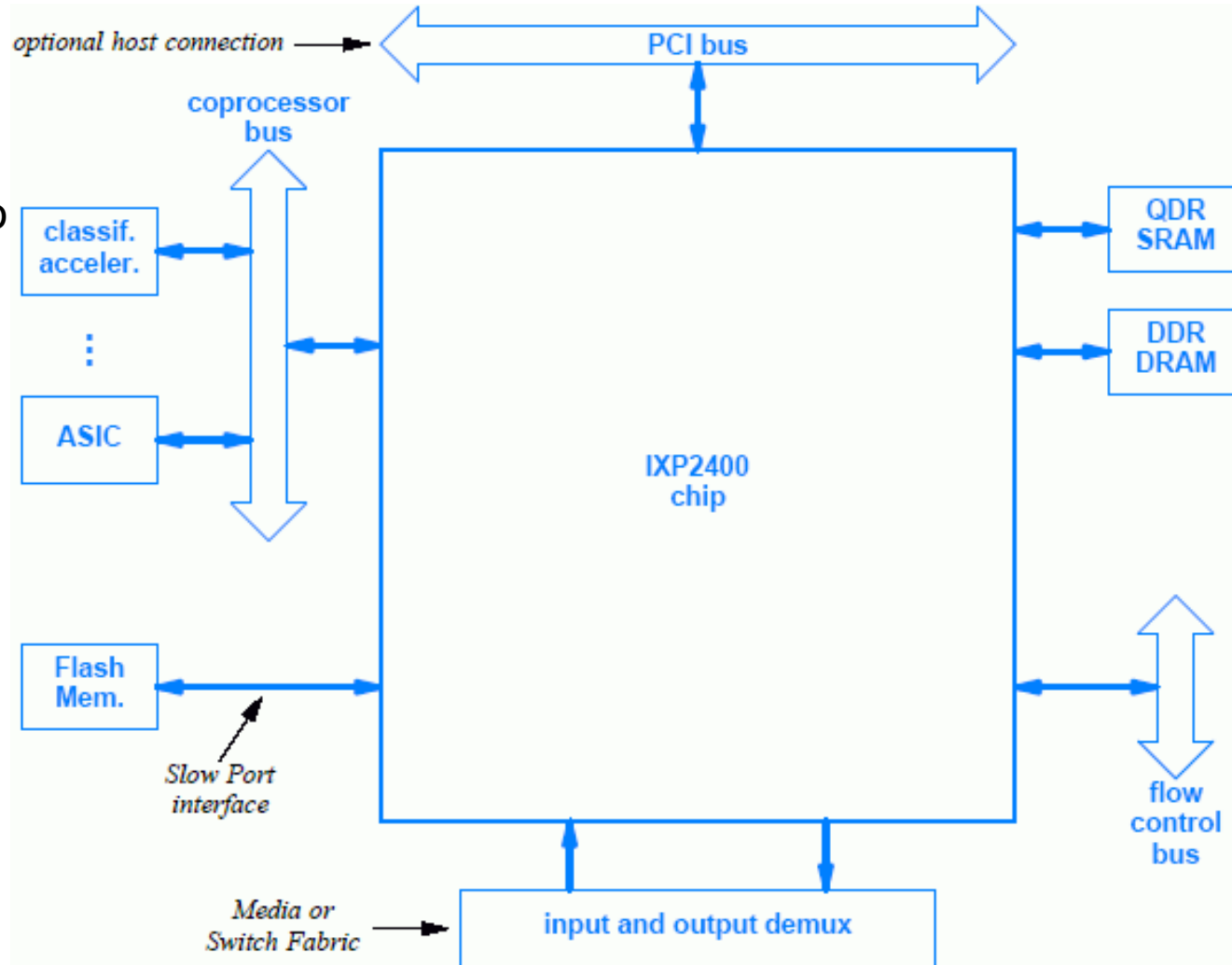
IXP2400

- Interconnects

- Coprocessor bus added (incl. access to T-CAM)
- Flow control bus for two-chip configurations (e.g., ingress and egress)

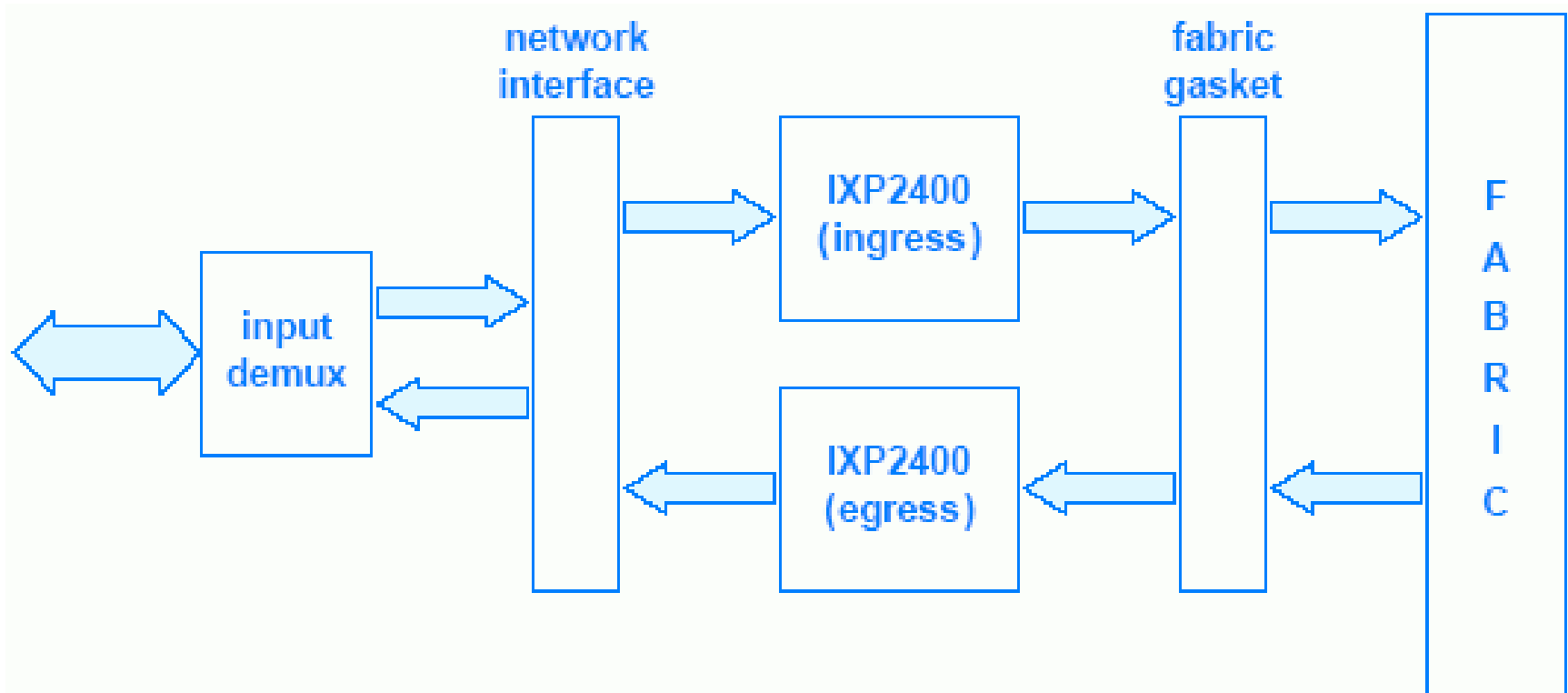
- Switch Fabrics

- No IX bus
- Utopia 1, 2, 3
- CSIX-L1
- SPI-3 (POS-PHY 2/3)

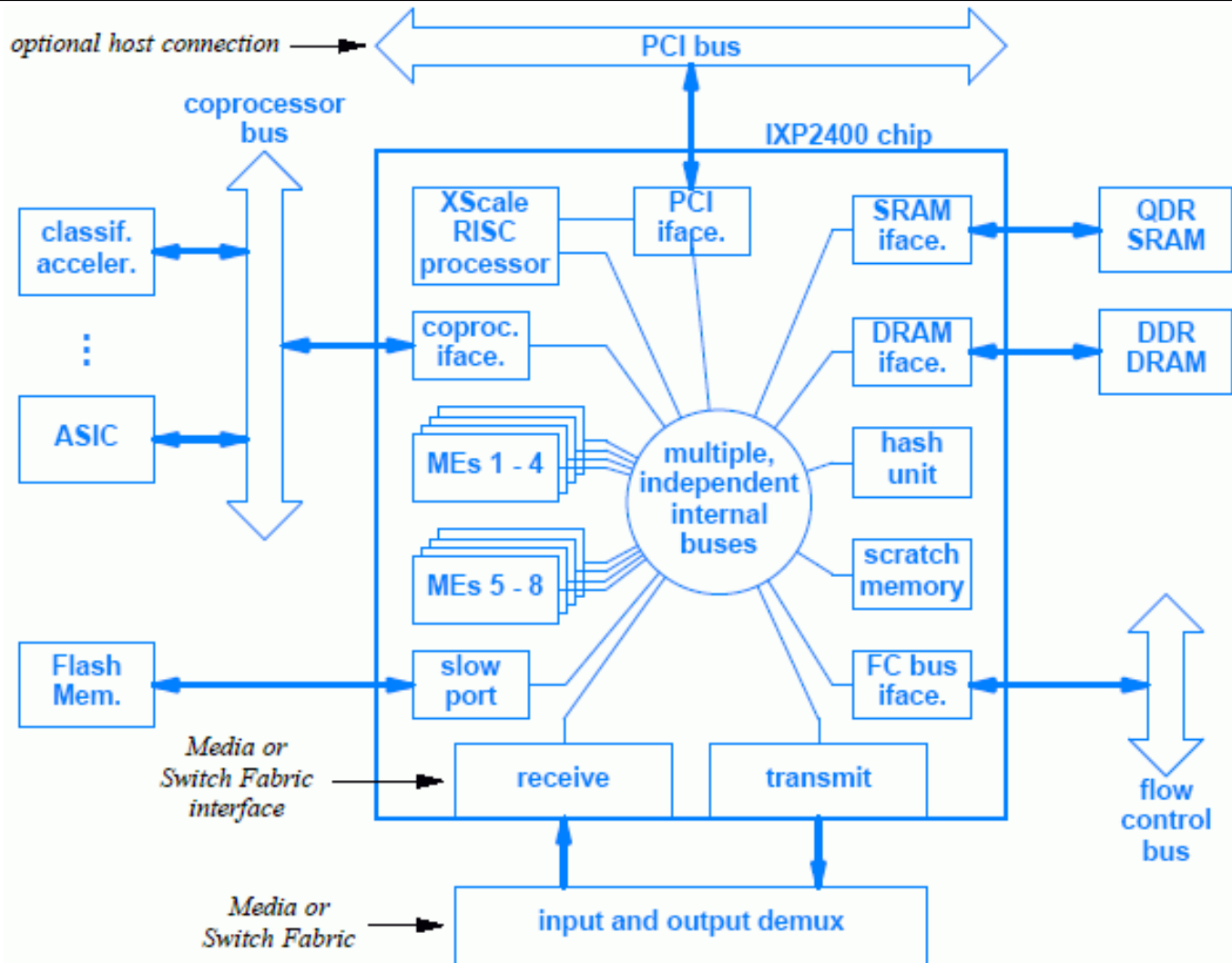


Two-Chip Configurations

- Flow control needed between ingress and egress side
 - 1Gbps over flow control bus (not shown)



IXP2400 Internal Architecture



IXP2400 Microengine

- Enhancements over IXP1200 microengines:
 - Multiplier unit
 - Pseudo-random number generator
 - CRC calculator
 - 4 32-bit timers and timer signaling
 - 16-entry CAM for inter-thread communication
 - Timestamping unit
 - Generalized thread signaling
 - 640 words of local memory
 - Simultaneous access to packet queues without mutual exclusion
 - Functional units for ATM segmentation and reassembly
 - Automated byte-alignment
 - uE divided into two clusters with independent command and SRAM buses

Software

- Support for software pipelining
 - “Reflector Mode Pathways” for communication
 - Next Neighbor Registers as programming abstraction
- SDK 3.1
 - Simulator, debugger, profiler, traffic generator
 - Portable modules
 - Provides better infrastructure support
 - C compiler

Summary

- Network processors are getting more features
- Main architecture characteristic is still parallelism
- Software support is becoming more important

Final Projects

- Final projects:
 - Implement a packet filter on IXP1200 hardware
 - E.g., don't forward telnet packets, but ssh packets
 - Analysis of memory contention on IXP1200
 - Write code to generate different amounts of load on memory
 - Analyze memory latency distribution and model it
 - Packet forwarding processing analysis
 - Count number of instructions spent on various steps of forwarding
 - Analyze impact of different # of uEs and threads
 - Compare to layer 2 bridging
 - Anything else?
- Project report ~10 pages with many interesting graphs and illustrations
- Final presentation: 15-20 minutes on 12/9/03

Lab 3

- Use of IXP1200 Hardware
- No (or not much) programming
- Measurement of forwarding performance
 - Direct wire
 - wwwbump (see book Chapter 26)
 - IPv4 forwarding
- Discussion of various measurement tools next week

Next Class

- Network security
 - General topic as example for network processor applications
- Network measurements
 - How to...
 - Various tools
- Start on your final projects today
- Happy Thanksgiving!