ECE 697J – Advanced Topics in Computer Networks

Commercial Network Processor Architectures

10/21/03

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Network Processors

- Commercial NPs
  - Large variety of architectures
  - Different application and performance spaces
  - Lots of details and practical issues
- Look for general patterns
  - Type of processors
  - How is parallelism used (parallel vs. pipelining etc.)?
  - Type and size of memories
  - Internal interconnect
  - Generality vs. specialization
  - Software environment (if discussed)
- At end of class, you'll have to decide which to buy
  - We'll look at different applications and you choose NP

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NP Application

- High-speed IPv4 forwarding
- Cheap, low-speed IPv4 forwarding
- Ipv6 forwarding
- Firewalling
- VPN termination
- Scanning of payload for viruses
- TCP/IP offloading / web switching
- Active networking

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Agere FPP

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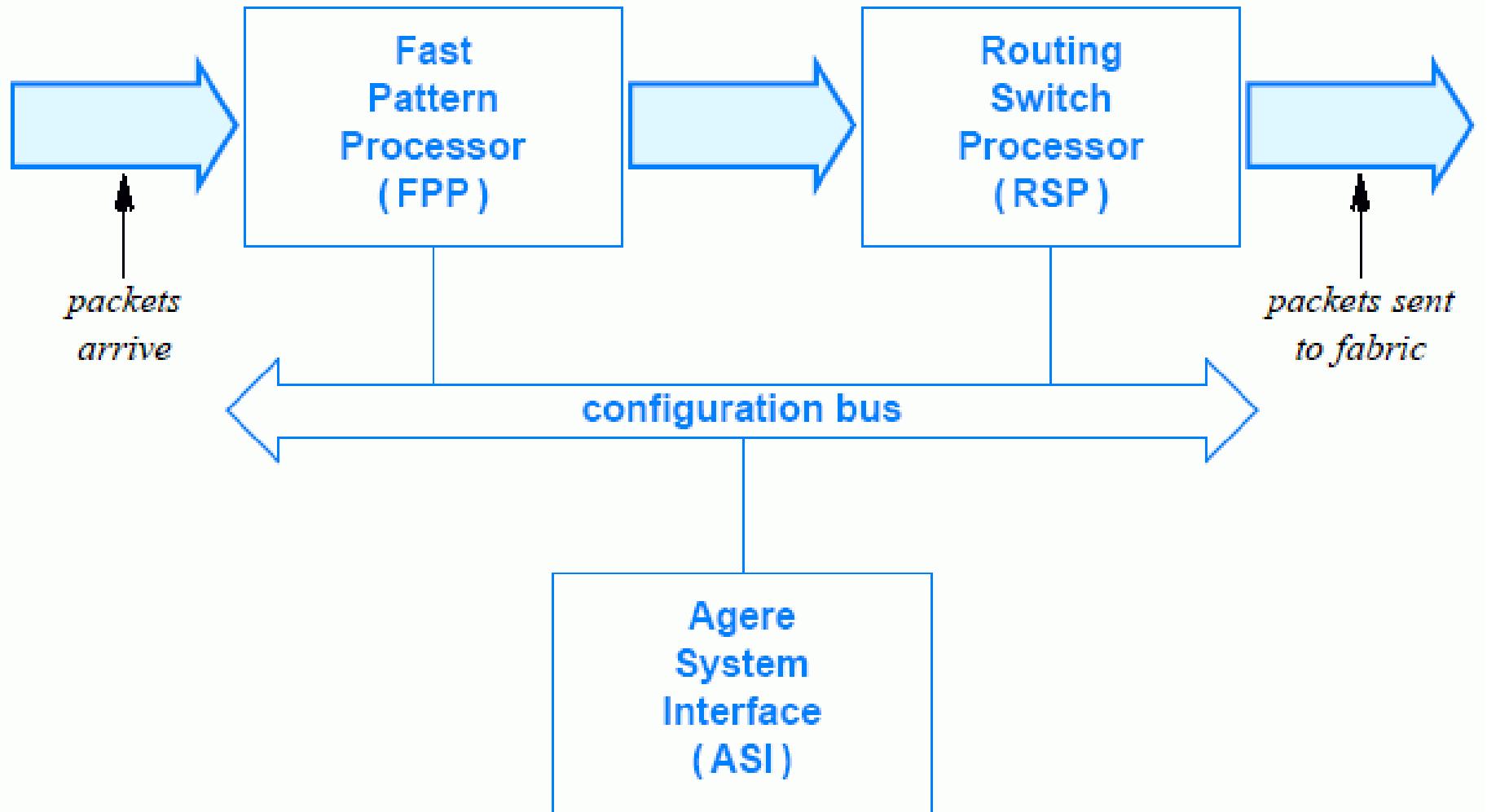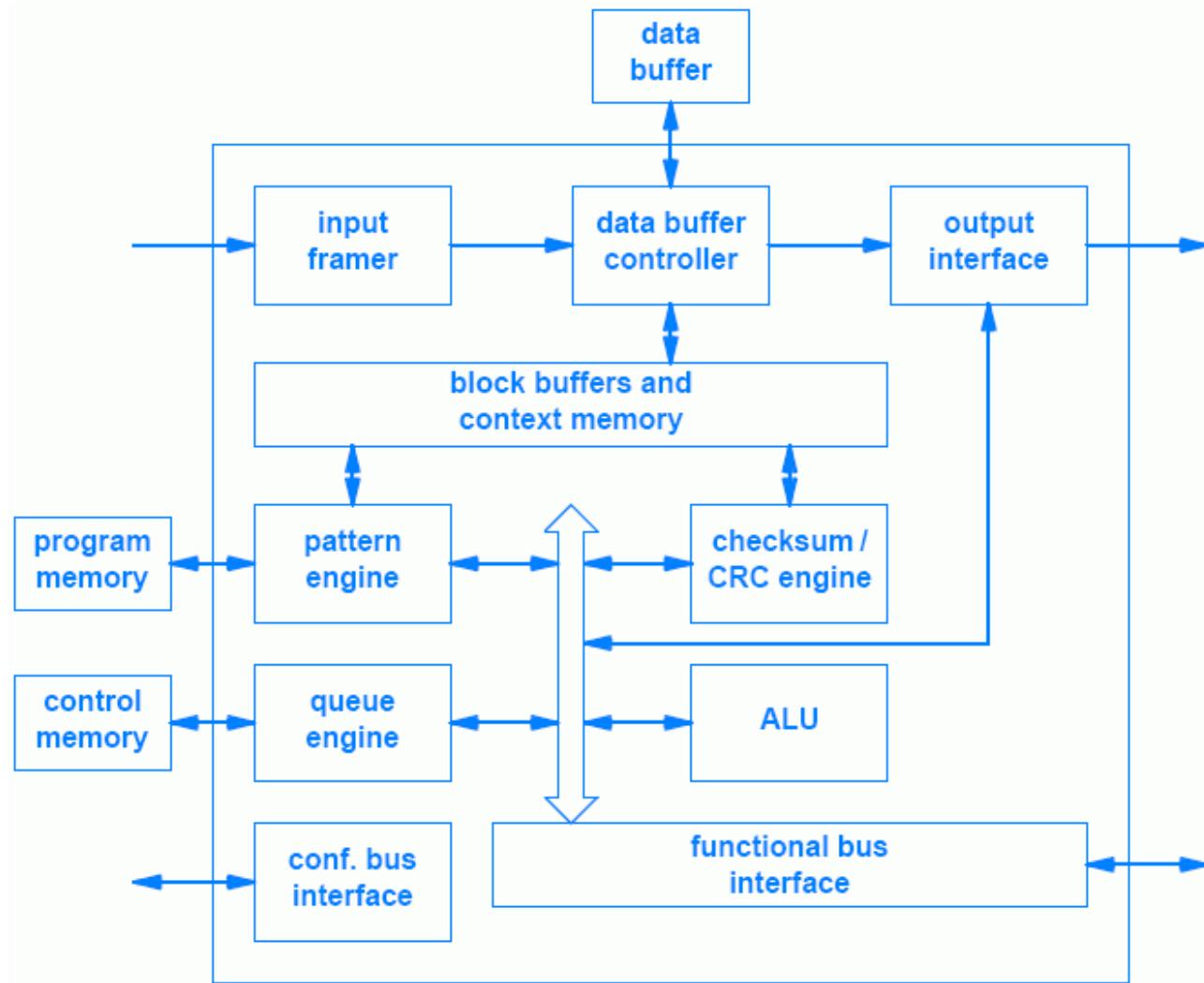
Agere FPP Functional Units

| Processor Or Unit	Purpose
Pattern processing engine	Perform pattern matching on each packet
Queue engine	Control packet queueing
Checksum/CRC engine	Compute checksum or CRC for a packet
ALU	Conventional operations
Input interface and framer	Divide incoming packet into 64-octet blocks
Data buffer controller	Control access to external data buffer
Configuration bus interface	Connect to external configuration bus
Functional bus interface	Connect to external functional bus
Output interface	Connect to external RSP chip

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Agere RSP

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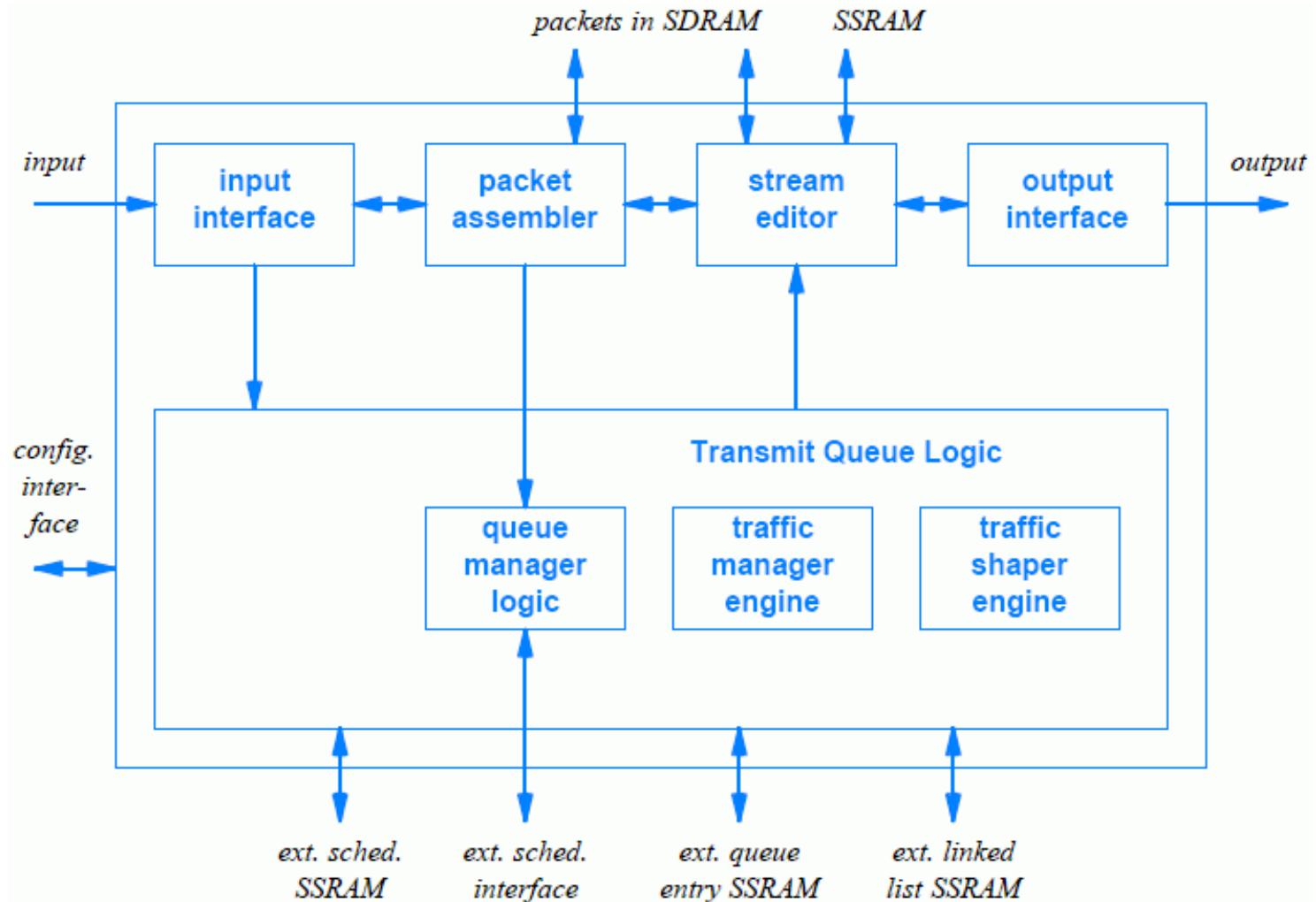
Agere RSP Functional Units

| Processor Or Unit	Purpose
Stream editor engine	Perform modifications on packet
Traffic manager engine	Police traffic and keep statistics
Traffic shaper engine	Ensure QoS parameters
Input interface	Accept packet from FPP
Packet† assembler	Store incoming packet in memory
Queue manager logic	Interface to external traffic scheduler
Output interface	External connection for outgoing packets
Configuration bus interface	Connect to external configuration bus

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Alchemy Au1000

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AMCC nP7510

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Cisco PXF

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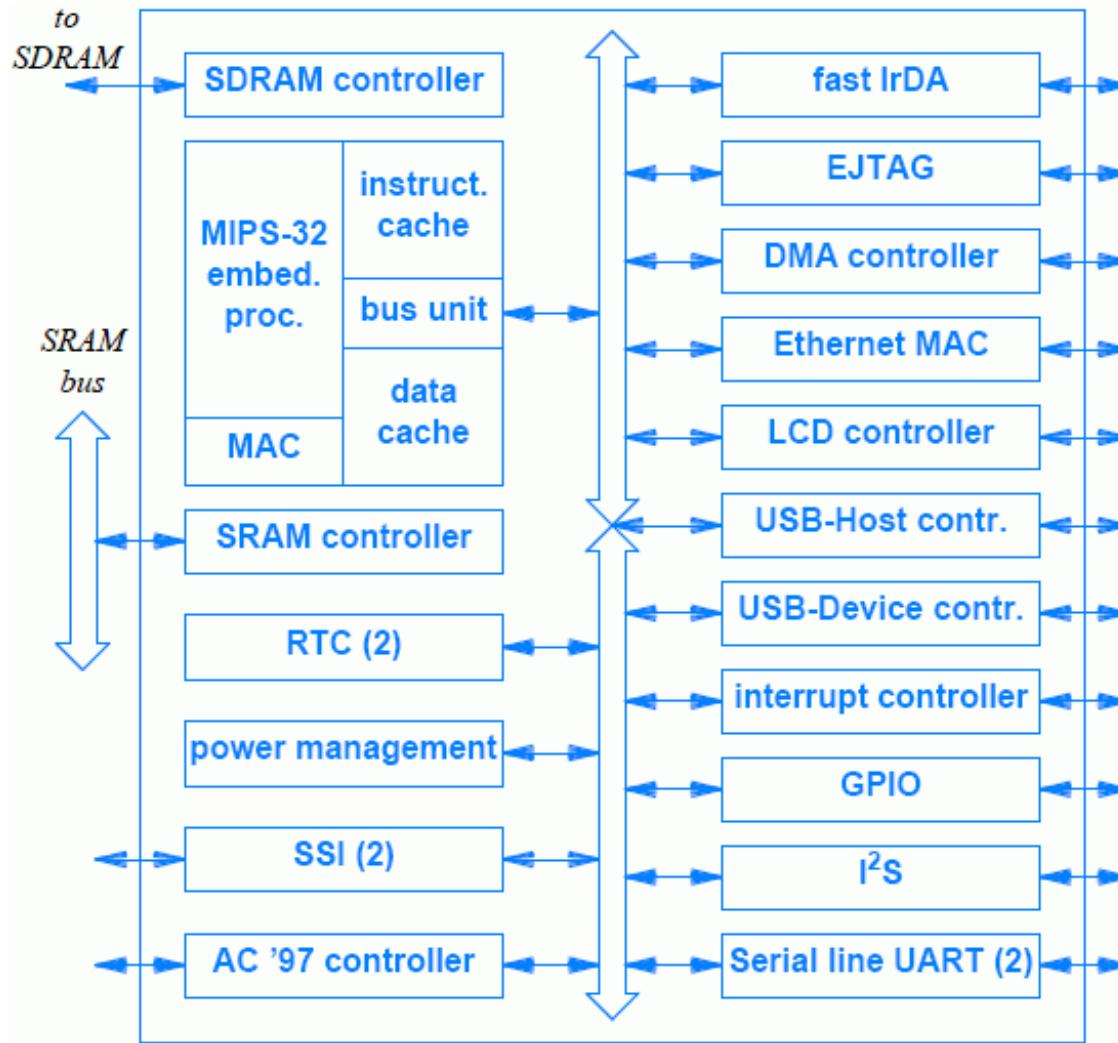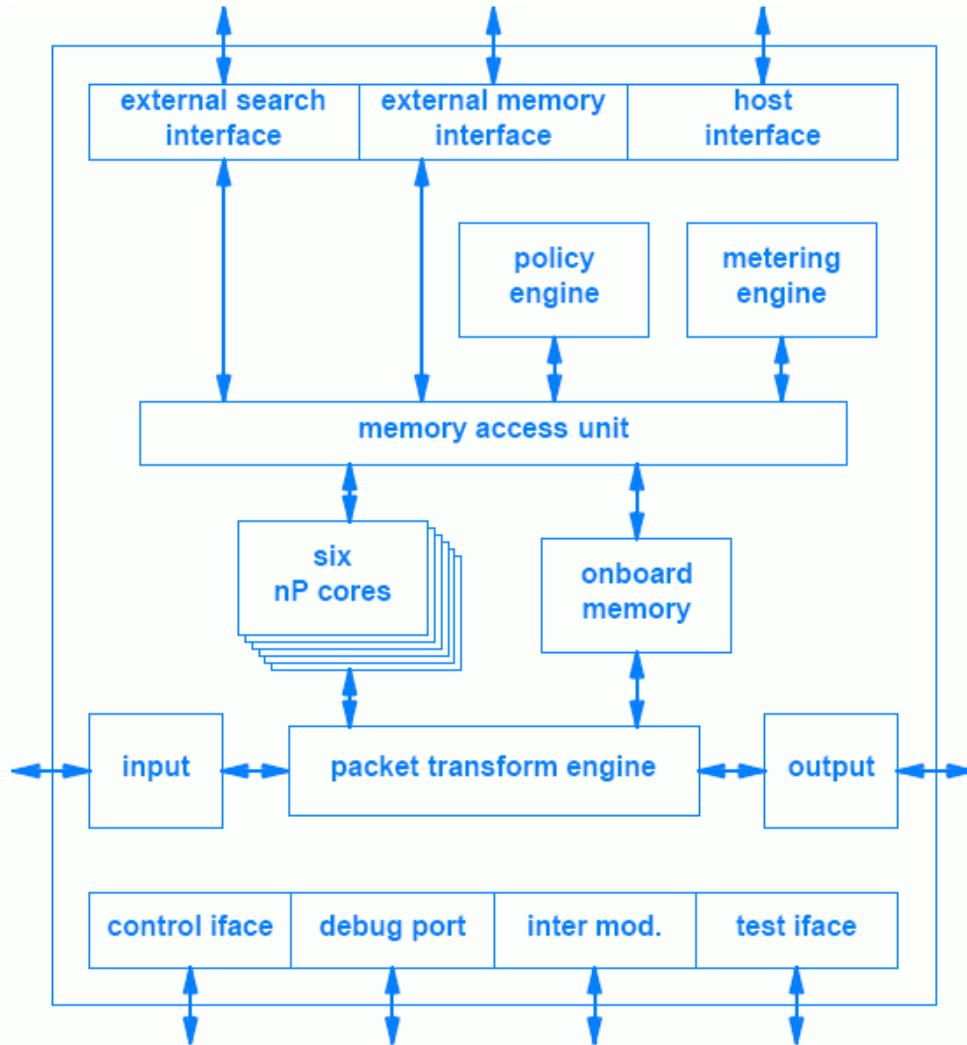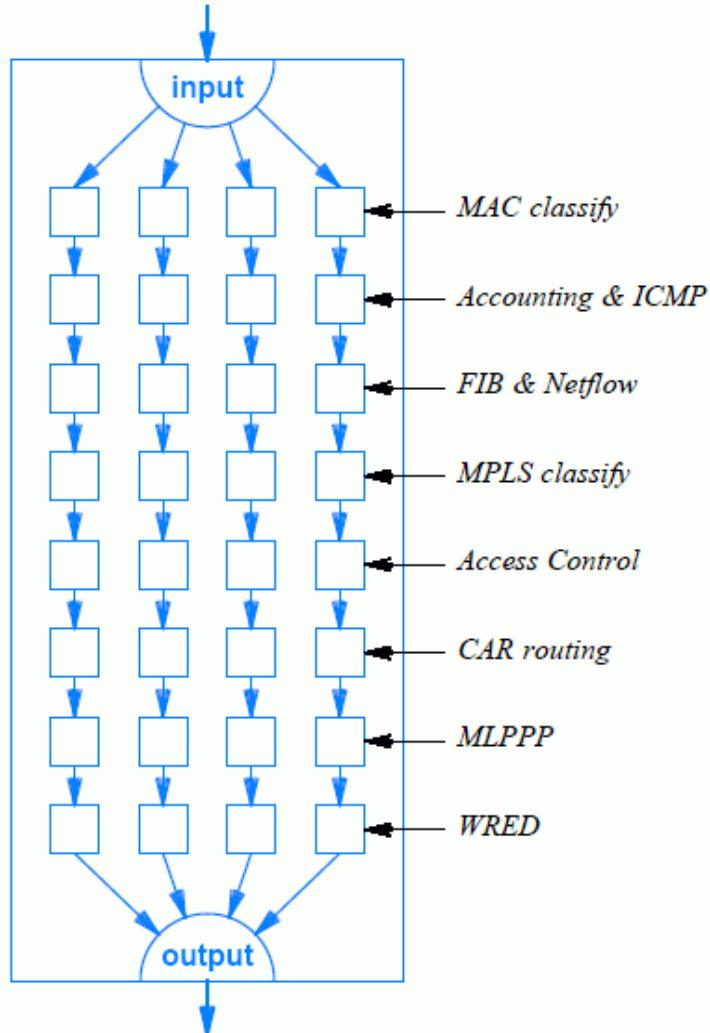
Cognigine RCU
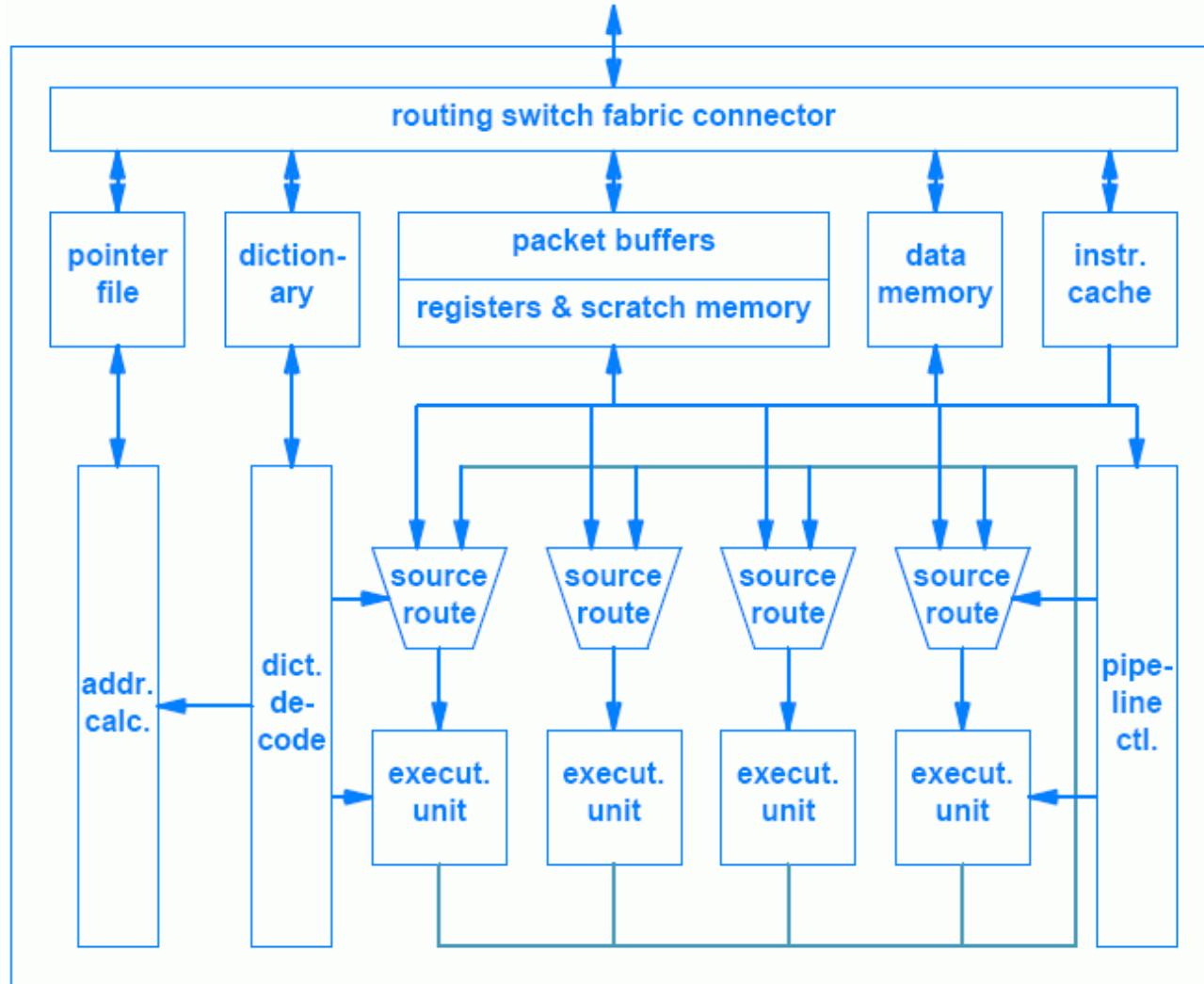
EZchip NP-1
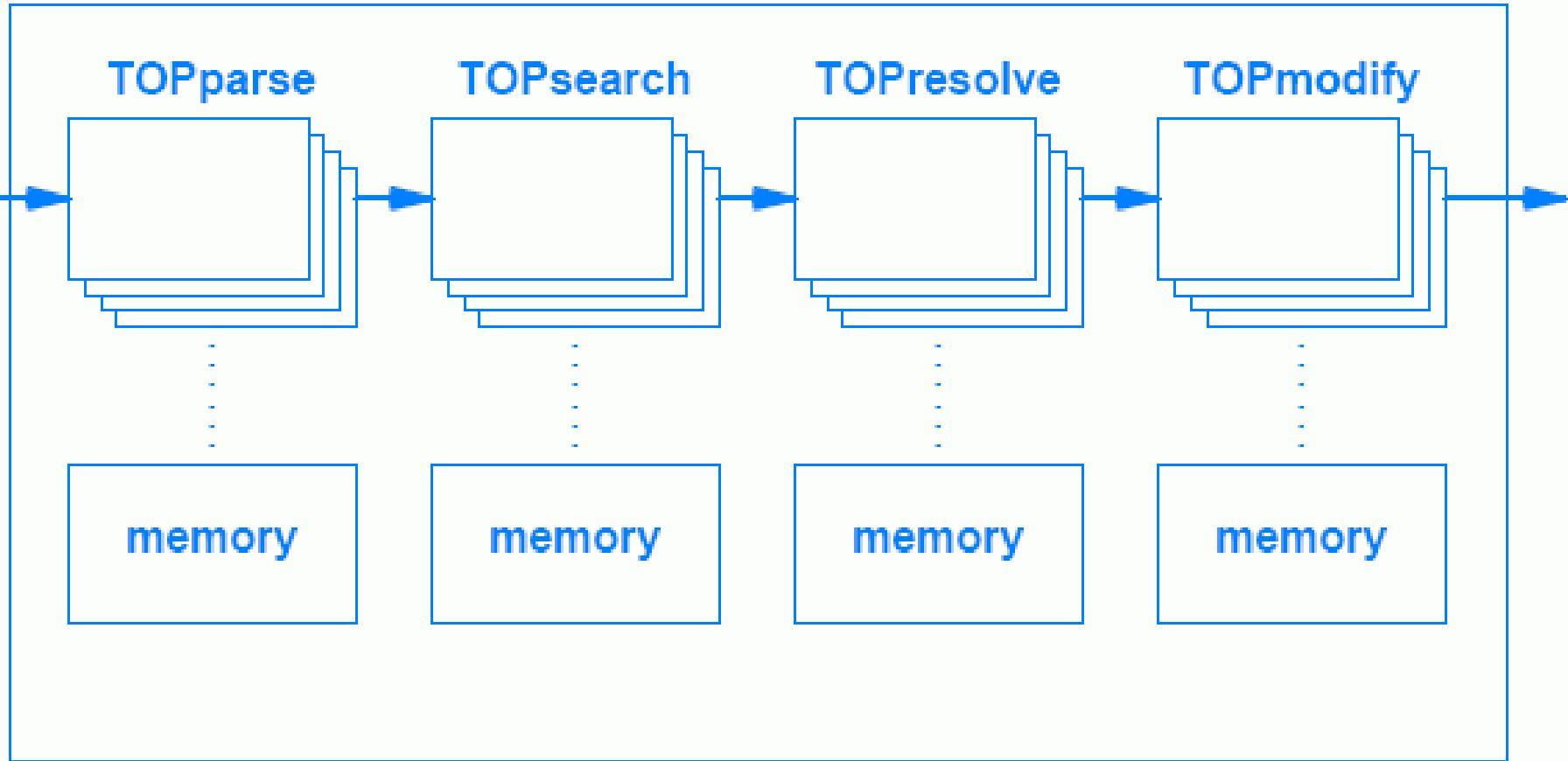
EZchip Processor Types

| Processor Type	Optimized For
TOPparse	Header field extraction and classification
TOPsearch	Table lookup
TOPresolve	Queue management and forwarding
TOPmodify	Packet header and content modification

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IBM PowerNP
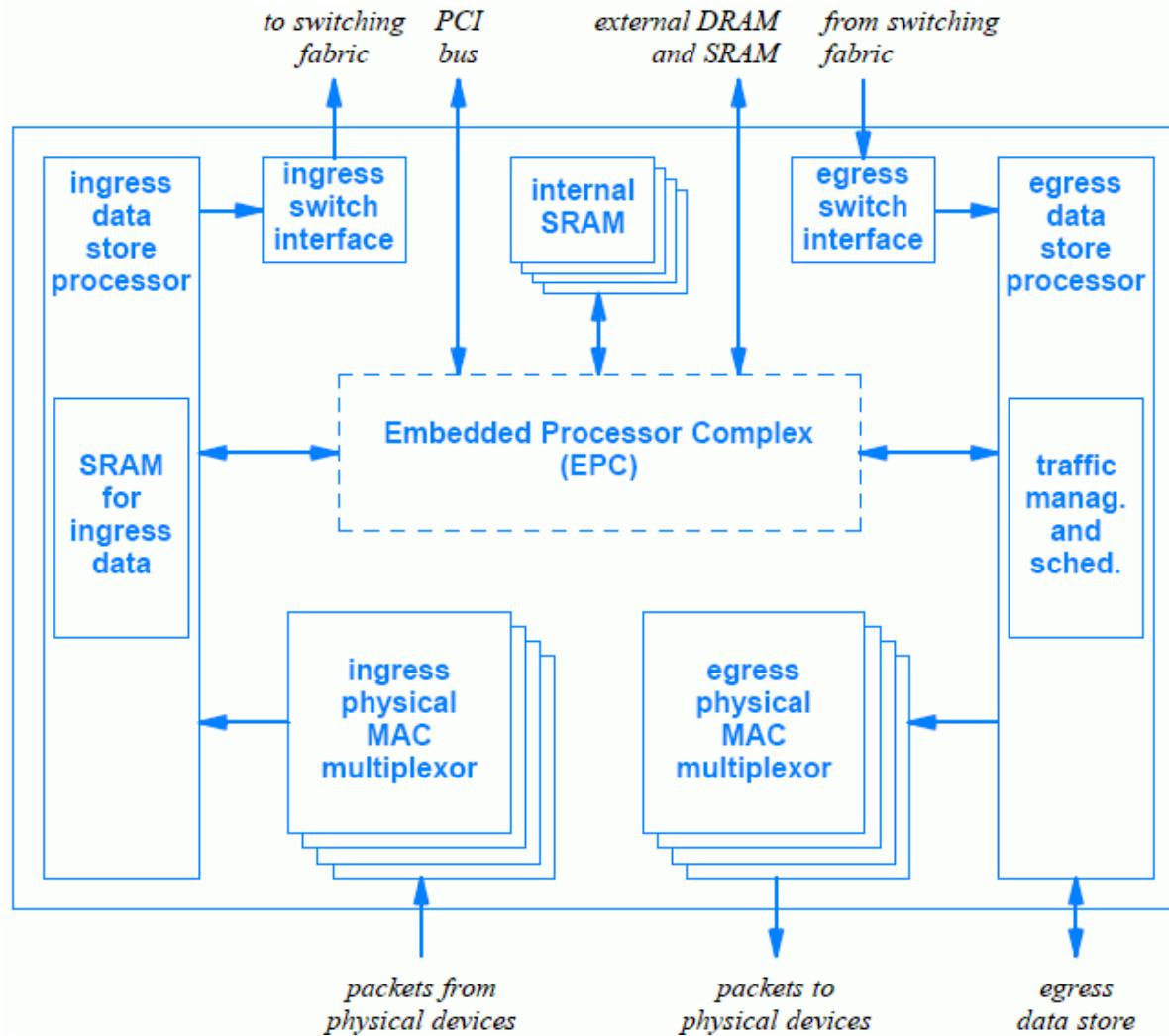
IBM Embedded Processor Complex

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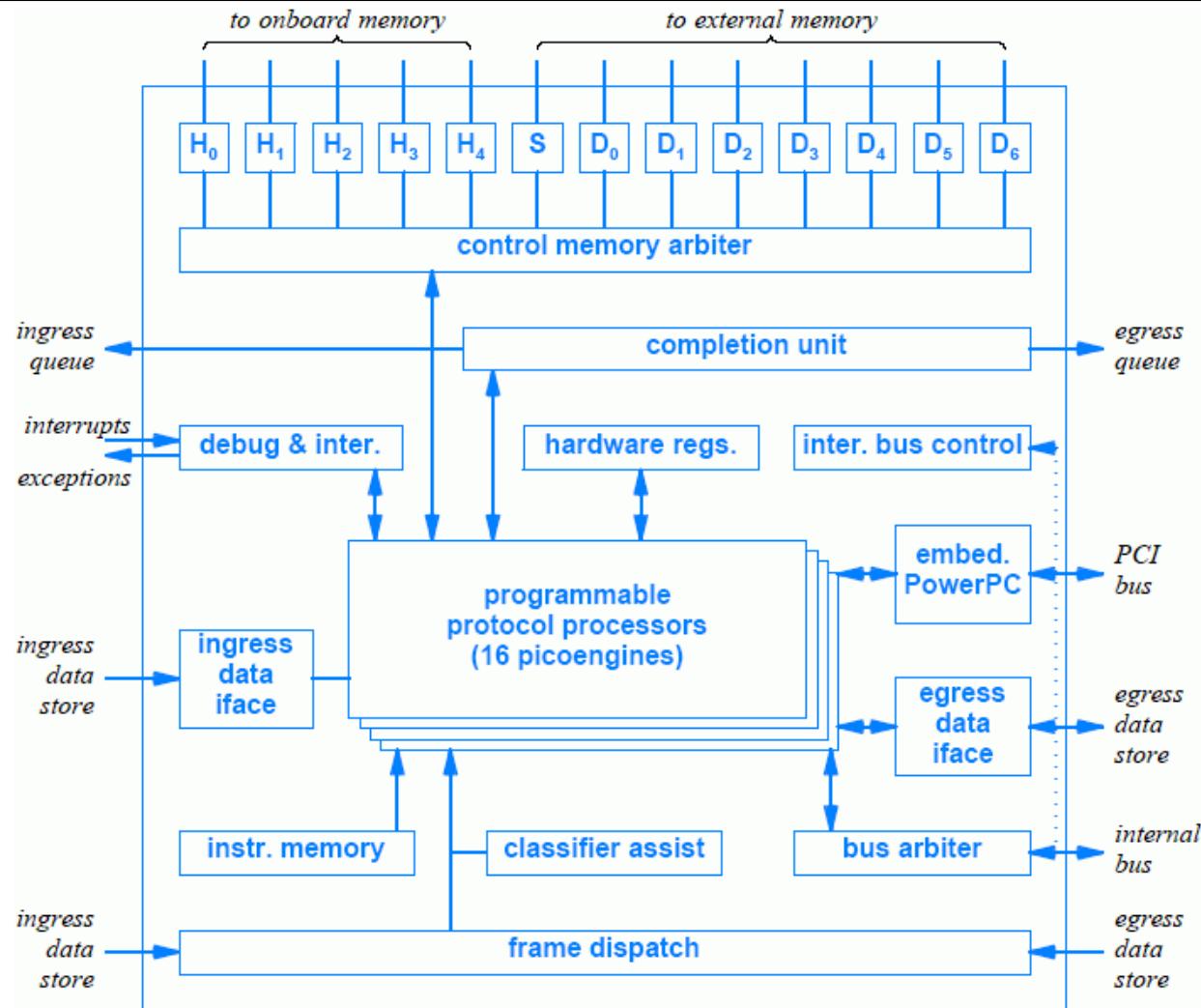
IBM Coprocessors

| Coprocessor	Purpose
Data Store	Provides frame buffer DMA
Checksum	Calculates or verifies header checksums
Enqueue	Passes outgoing frames to switch or target queues
Interface	Provides access to internal registers and memory
String Copy	Transfers internal bulk data at high speed
Counter	Updates counters used in protocol processing
Policy	Manages traffic
Semaphore	Coordinates and synchronizes threads

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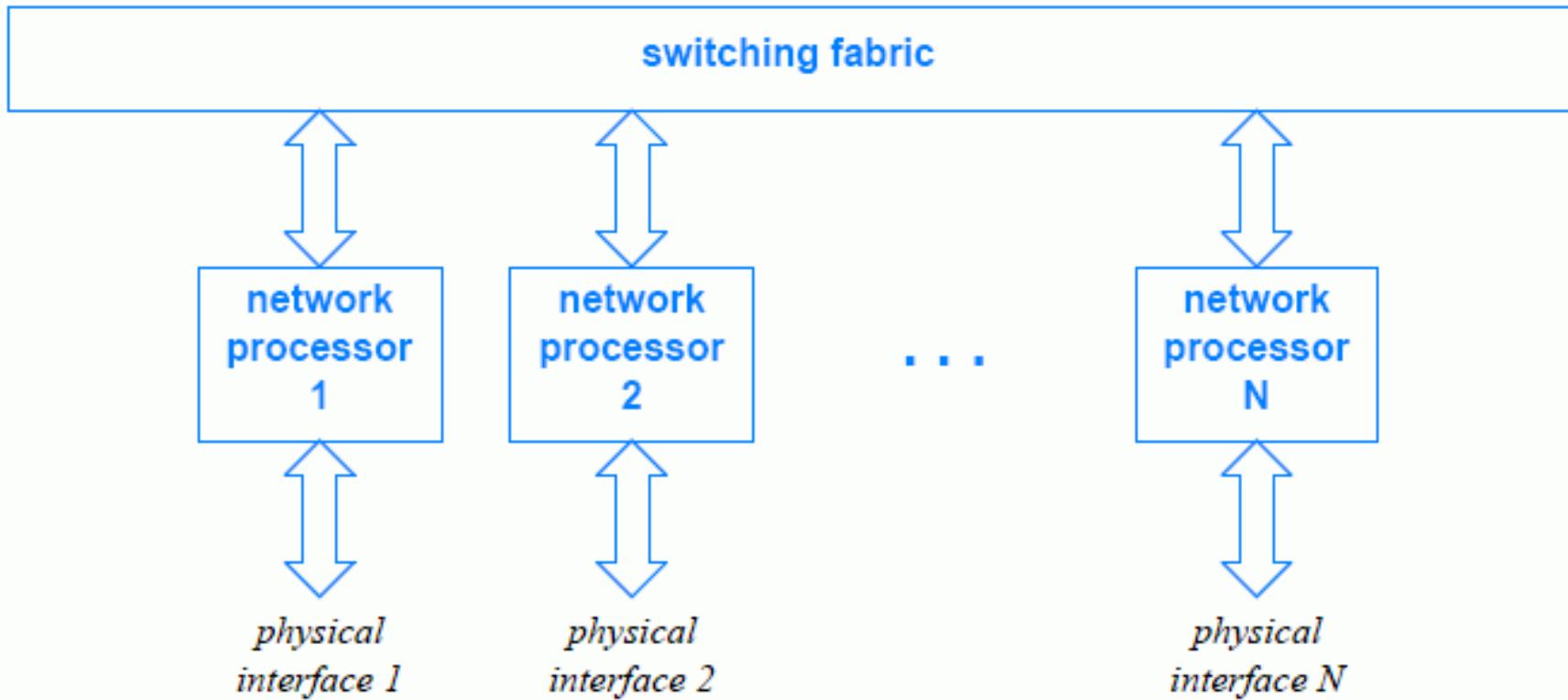
Motorola C-Port

Motorola C-Port
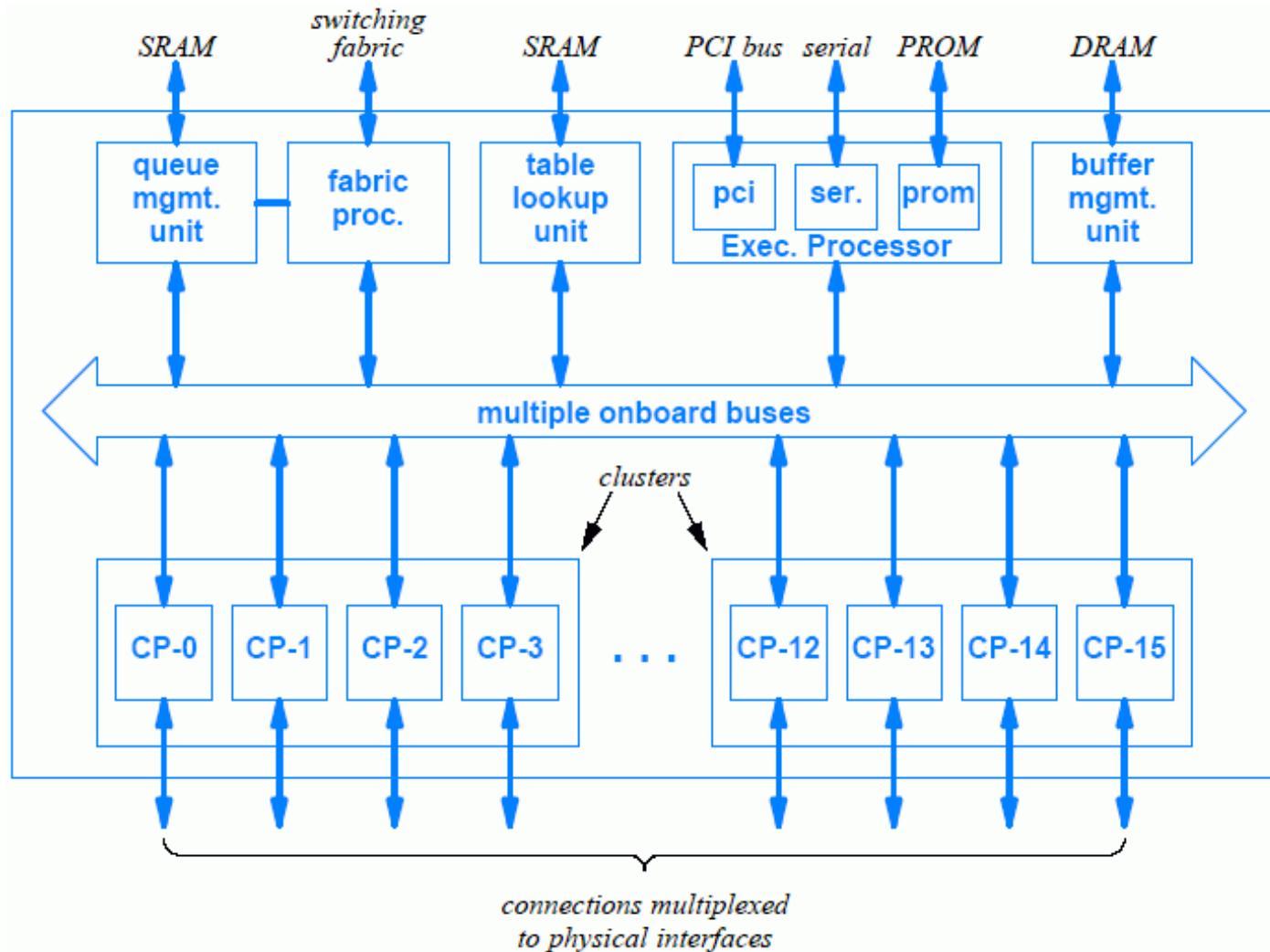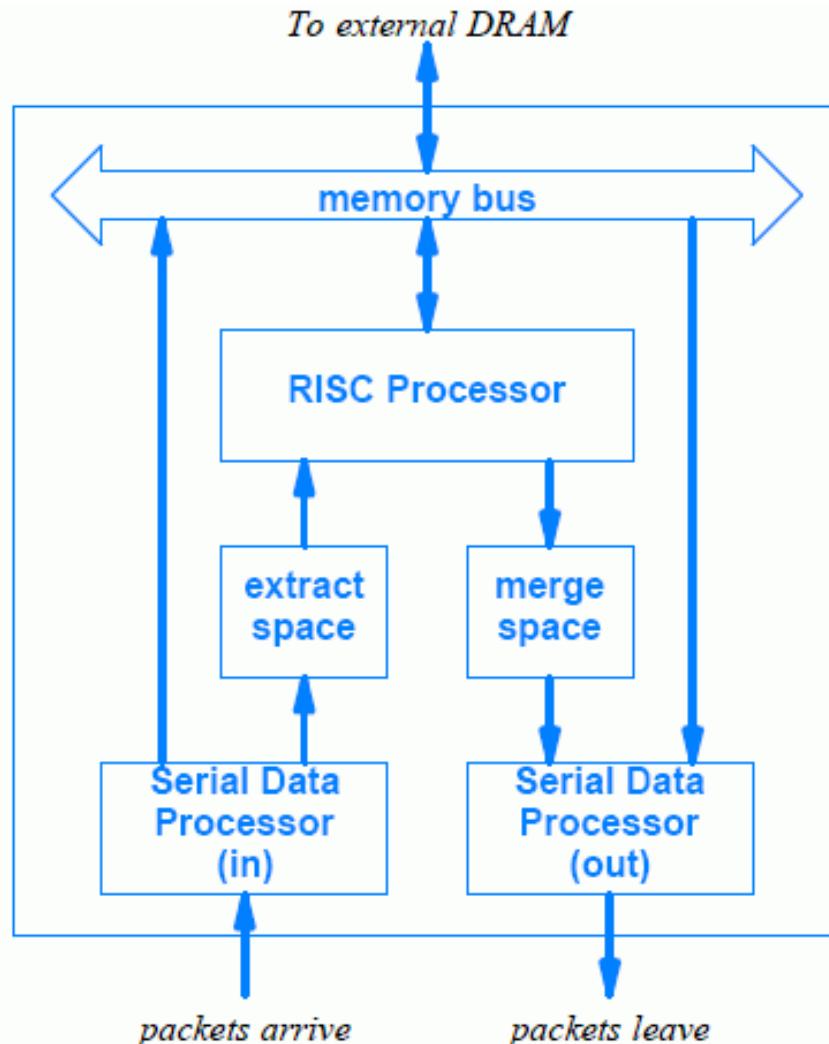
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Motorola C-Port CP

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Next Class

- Design Tradeoffs
  - How can the optimal configuration of a NP be determined?
- We are skipping Chapter 16
- Read
  - Chapter 17
  - Paper "A network processor performance and design model with benchmark parameterization."

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