Commercial Network Processors

ECE 697J

December 5th, 2002

AMCC nP7250 Network Processor

Presenter: Jinghua Hu

AMCC nP7250

- Released in April 2001
- Packet and cell processing
- Full-duplex OC-48c Network Processor

- Nominated for Microprocessor Report Analysts' Choice Award

General Features

- Offers layer 2, 3, 4 and above packet/cell processing at wire speed
- Supports multi-service cell/packet switching/routing in
  - Clear Channel Mode
  - Multi-Channel Modes
- Wide range of applications

Hardware: nPcore

- nPcore Model
  - Hardware multi-threading
  - Optimized Network Instruction Set Computing
  - Zero-cycle context switching
  - Four On-chip Coprocessors

  - Dual nPcores offer OC-48c bandwidth

Hardware: Co-processors

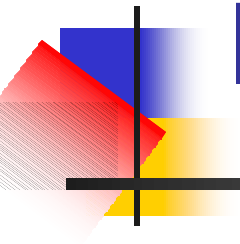
- Four Embedded co-processors
  - Packet Transform Engine
  - Policy Engine
  - Statistics Engine
  - Special Purpose Engine

Programming Model

- Fundamentally simplified multi-processor programming model
  - Single-stage, run to completion
  - Each packet/cell executes in a single thread on a single core
  - Facilitate software developers

AMCC solution set

- nP7250 OC-48c Network Processor
- nPX5700 10Gbps Traffic Manager
- nPX5800 40-320Gbps Switch Fabric



Motorola C-5E Network Processor

ECE697J: Active Network

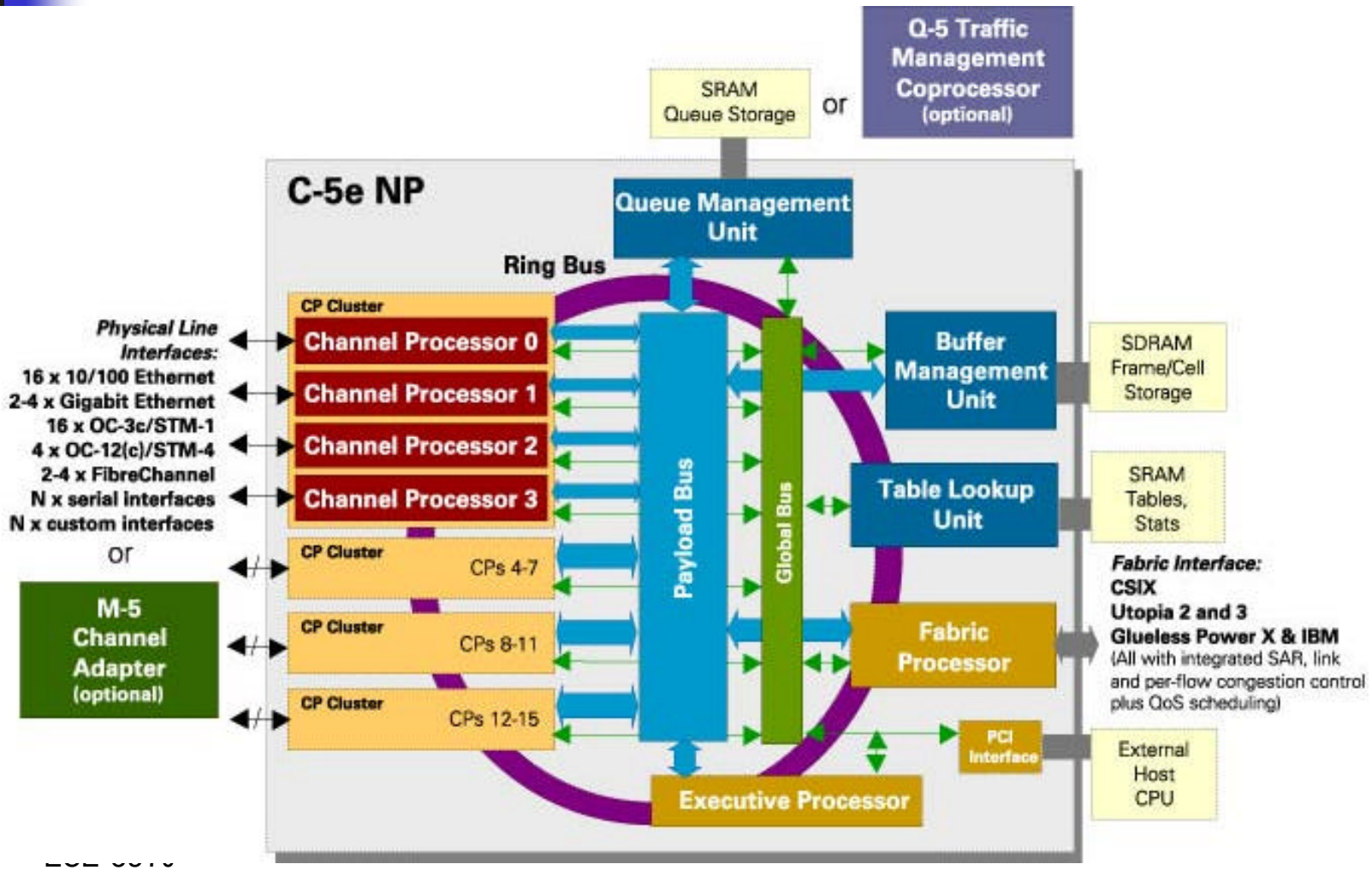
Presenter: Jianhong Xia

12/05/2002

Product Picture

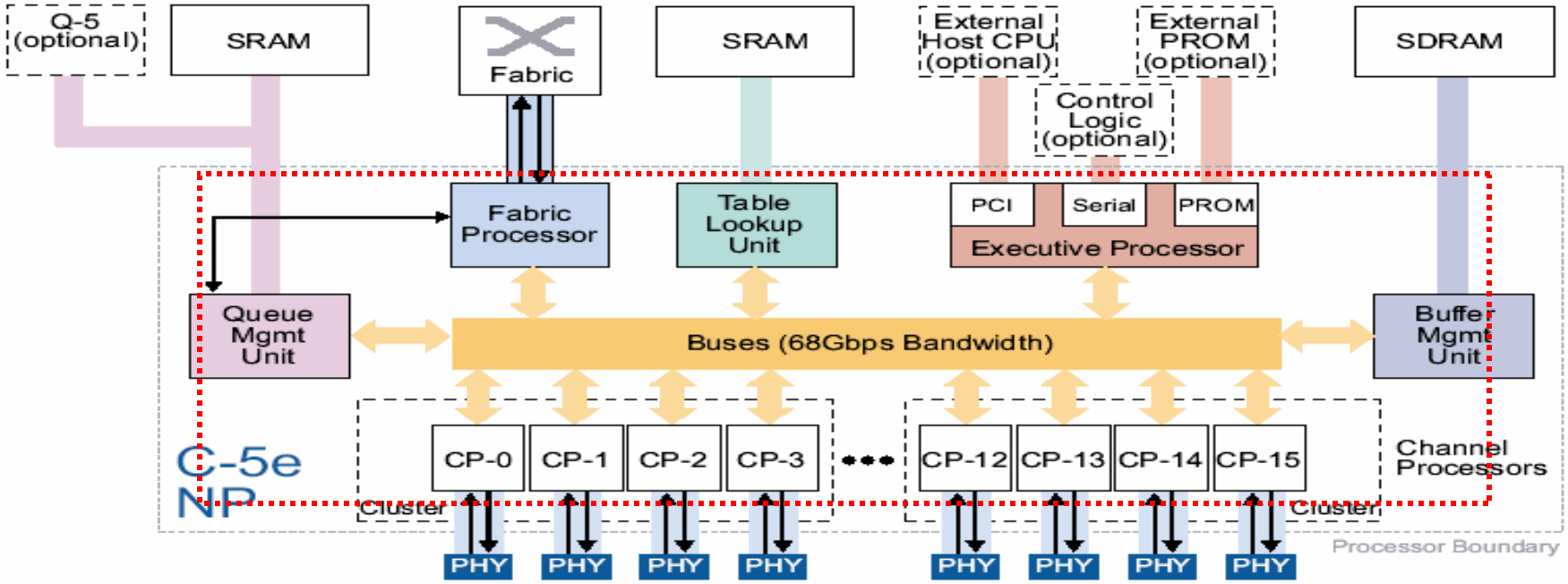
- The C-5e™ Network Processor (NP)
  - Second generation of the C-Port™ family of network processors
  - Most integrated, flexible, and functionally-rich processor

Block Diagram



Block Diagram

Figure 1 C-5e Network Processor Block Diagram



PHY Interface Examples:

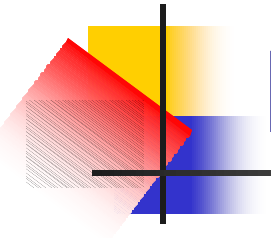
10/100 Ethernet

Gigabit Ethernet - Aggregated

OC-3

OC-12

1xOC-48c or 48x STS-1 with M-5 Companion Device

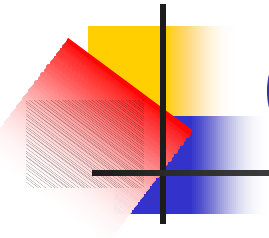


Features (1)

- Processor & Power Consumption
  - 266MHZ, 9W, 1.2V typical
- Bandwidth & Computing Power
  - 5GBPS, non-blocking throughput, 4,500 MIPS
- RISC Cores & Co-Processors
  - 17 programmable RISC Cores for cell/packet forwarding
  - 32 programmable Serial Data Processors for processing bit streams
- On-chip classification coprocessor
  - supporting over 46 million IPv4 lookups/second

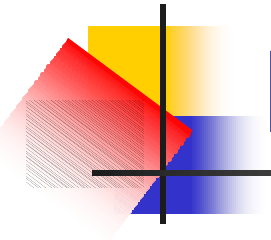
Features (2)

- Flexible interfaces
  - any serial or parallel protocol
  - individual port data rate from DS1 to OC-48c/STM-16
- External C-Port Q-5 TMC (Traffic Management Coprocessor)
  - advanced QoS
- Simple and efficient programming
  - C-language with standard APIs
- Royalty-free reference applications
- Key alliances in
  - fabrics, coprocessors, network software, and design services



Channel Processor

- Consists of
  - Dedicated RISC Core
  - Dual Serial Data Processors (SDPs)
    - Data encoding/decoding
    - Framing / Formatting / Parsing
    - Error checking (CRCs)
    - Control programmable external pin logic



Executive Processor

- Centralized computing resource
- Manages the system interfaces
- Conventional supervisory tasks
  - Reset and initialization of the C-5e NP
  - Program loading and control of CPs
  - Centralized exception handling
  - Management of a host interface through the PCI
  - Management of system interfaces (PCI, Serial Bus, PROM)

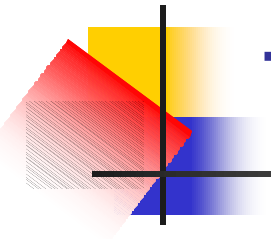
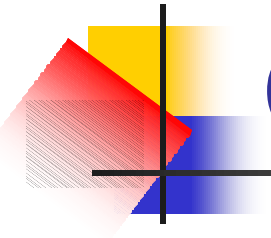


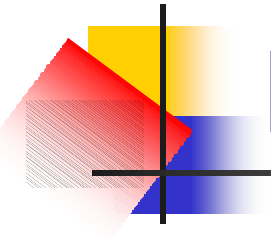
Table Lookup Unit

- Classification Engine
  - High-speed, Flexible
  - 46 million IPv4 lookups per second



Queue Management Unit

- Support QoS Management
  - Up to 512 queue to satisfy the traffic management requirements
  - More powerful with Q-5 TMC (Traffic Management Coprocessor)



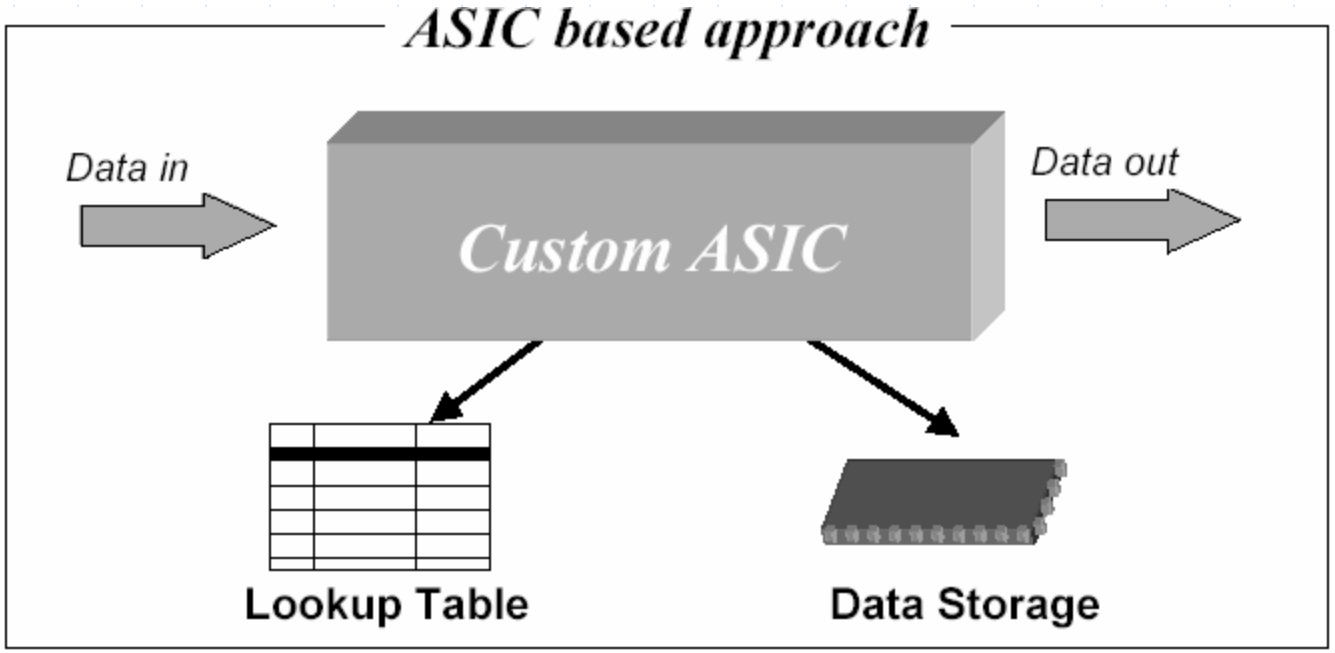
Buffer Management Unit

- Interfaces to Single Data Rate Synchronous DRAM.
  - Used as buffers for receiving and transmitting data between CPs, the FP, and the XP
  - Used as second level storage in the XP memory hierarchy

Agere Payload Plus

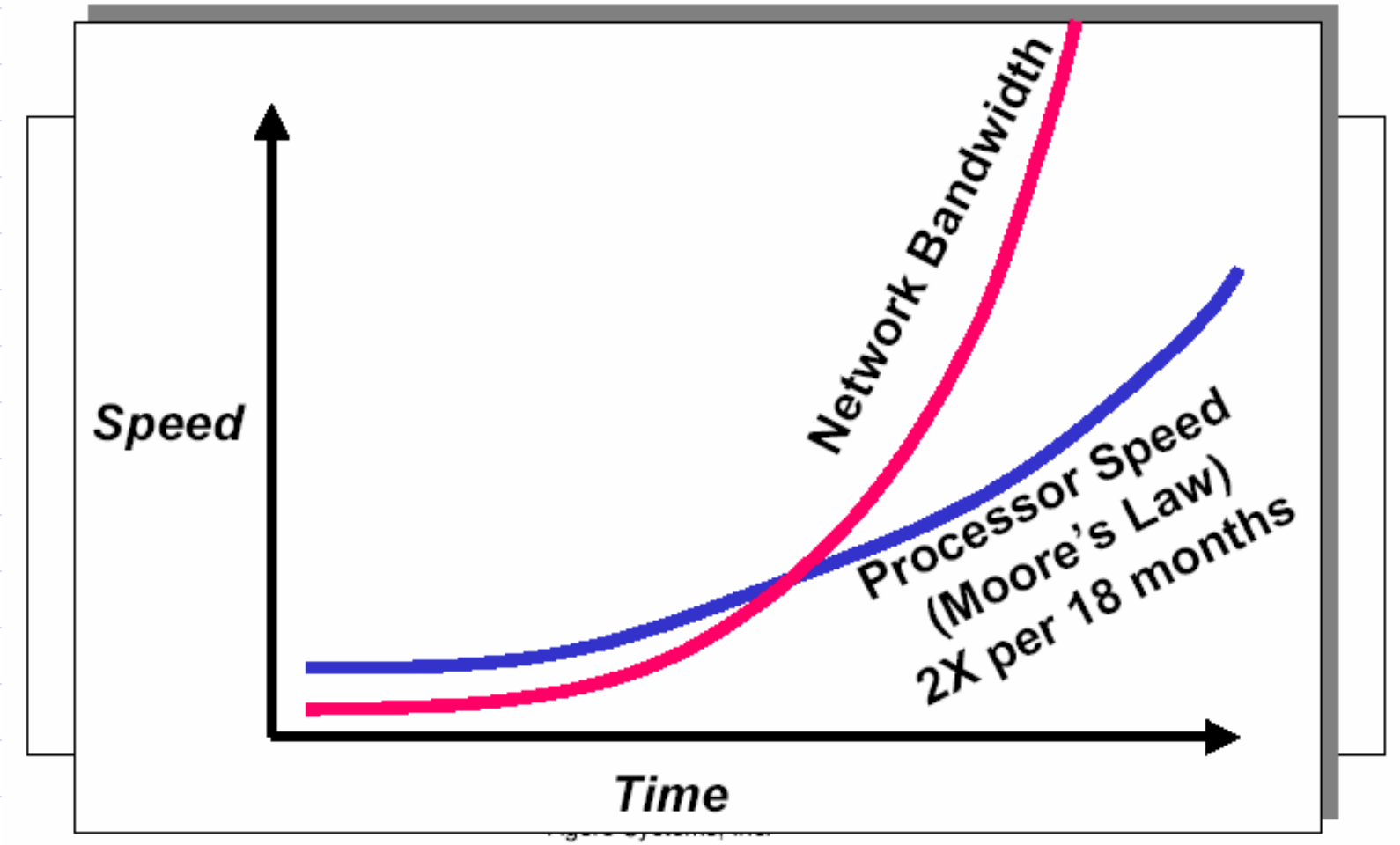
Jayakrishnan Nair

Traditional NP Approach

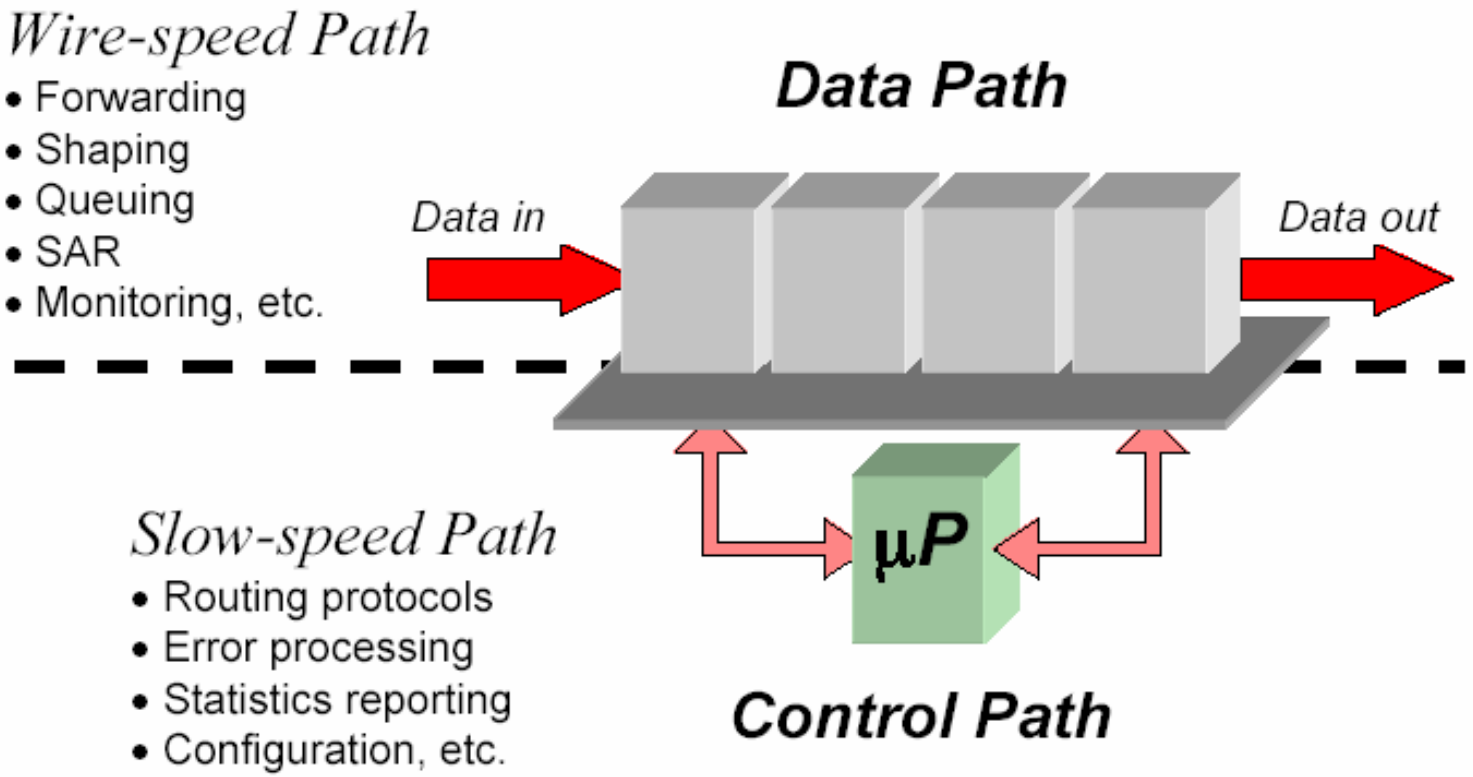


- Custom ICs for wire-speed routing/ queuing
  - High Development Costs
  - Long time to market
  - No Flexibility or scalability to support future enhancements (IPv6)

Traditional Methods Insufficient



The Novel Agere's Approach



- Have a highly pipelined Chipset for fast Data-Path

How is Agere's Approach Novel?

- The Payload Plus is a breakthrough 3-chip solution for handling fast traffic, as in OC-48 or Gbps networks
- Performs all of the classification, policing, traffic management, QoS, traffic shaping and packet modification functions needed for Gbps network platform
- Focus on wire-speed data stream, by working in tandem with physical interface devices, microprocessors, and backplane fabric offerings

The Payload Plus Family

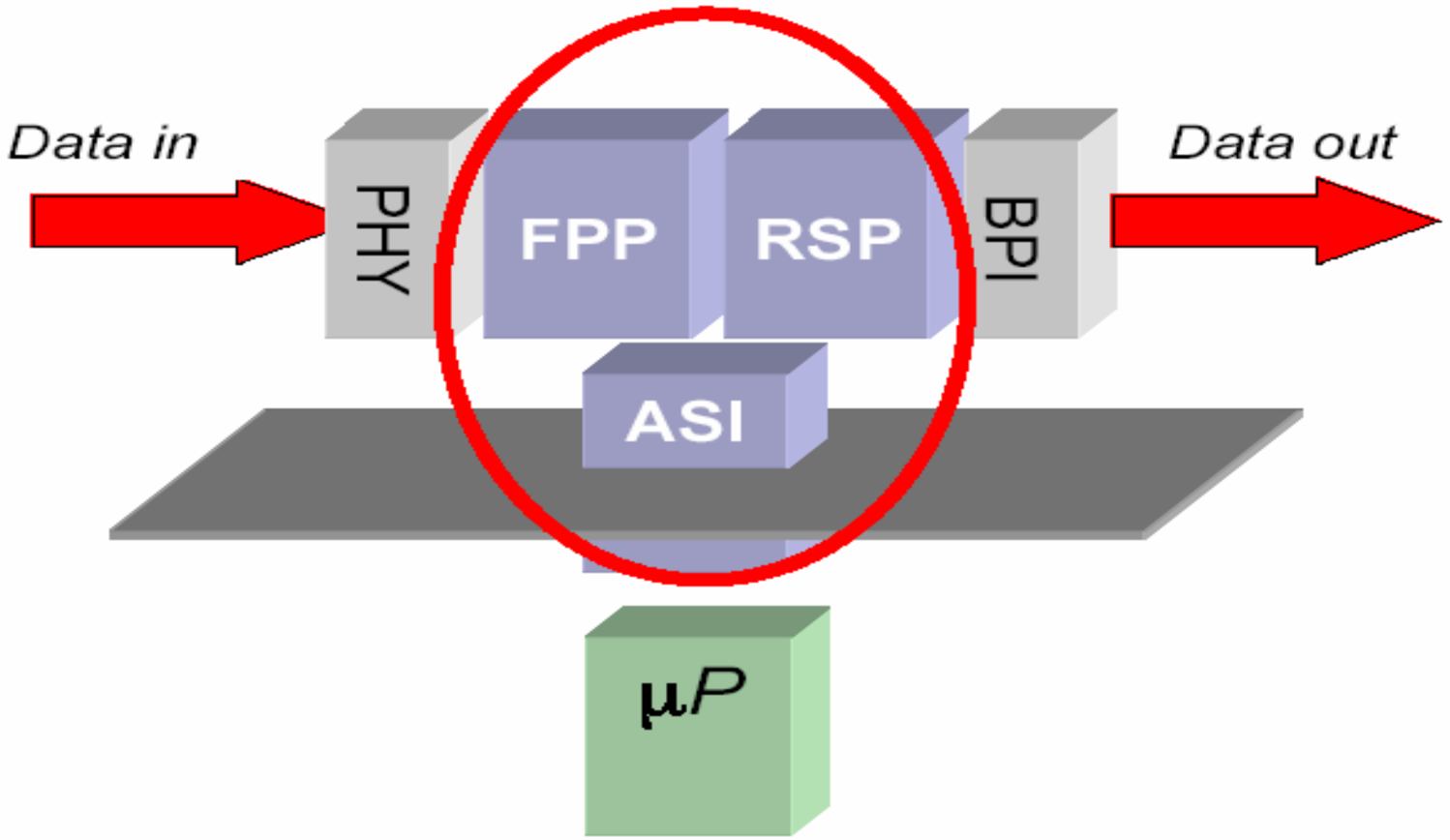
Payload plus NPU family has three chips

- Fast Pattern Processor (FPP)
- Routing Switching Processor (RSP)
- Agere System Interface (ASI)

These chips are connected to:

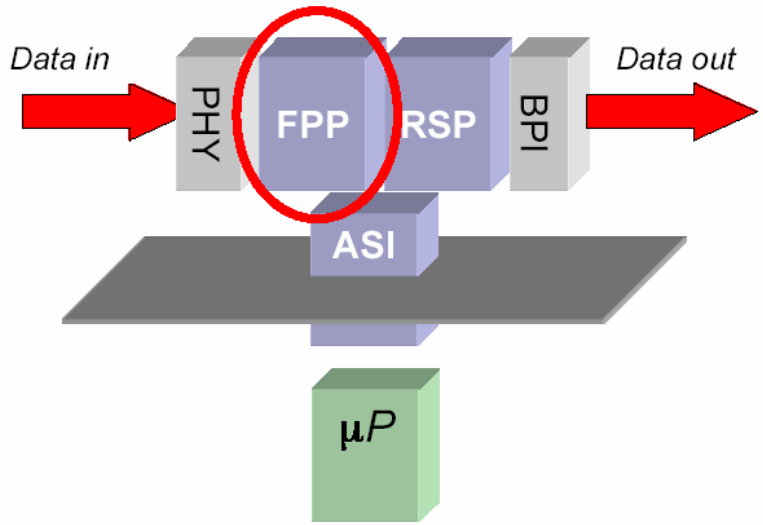
- Physical Layer (PHY) - For Data to Come In
- BackPlane Interface (BPI) – Data Out
- Microprocessor (µP) – For Data Processing

The Payload Plus Chipset



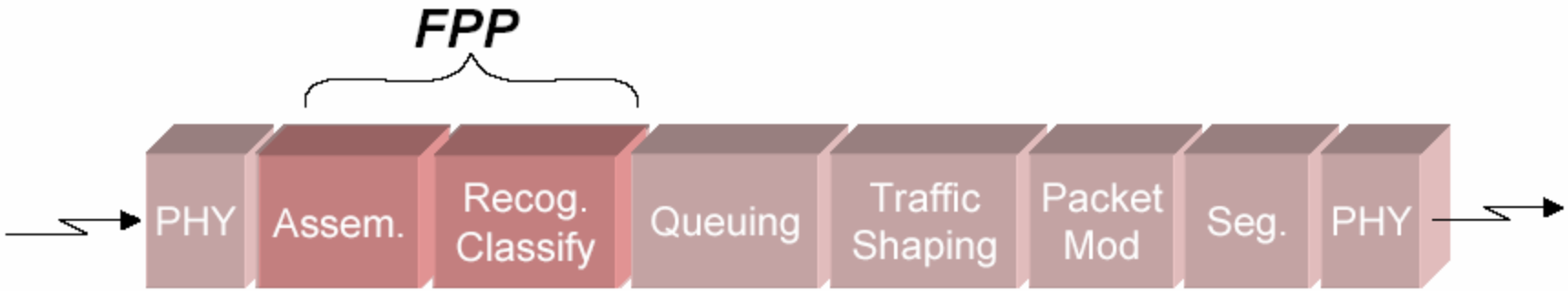
Agere Chipset forms the wire-speed path

Fast Pattern Processor (FPP)



Functions

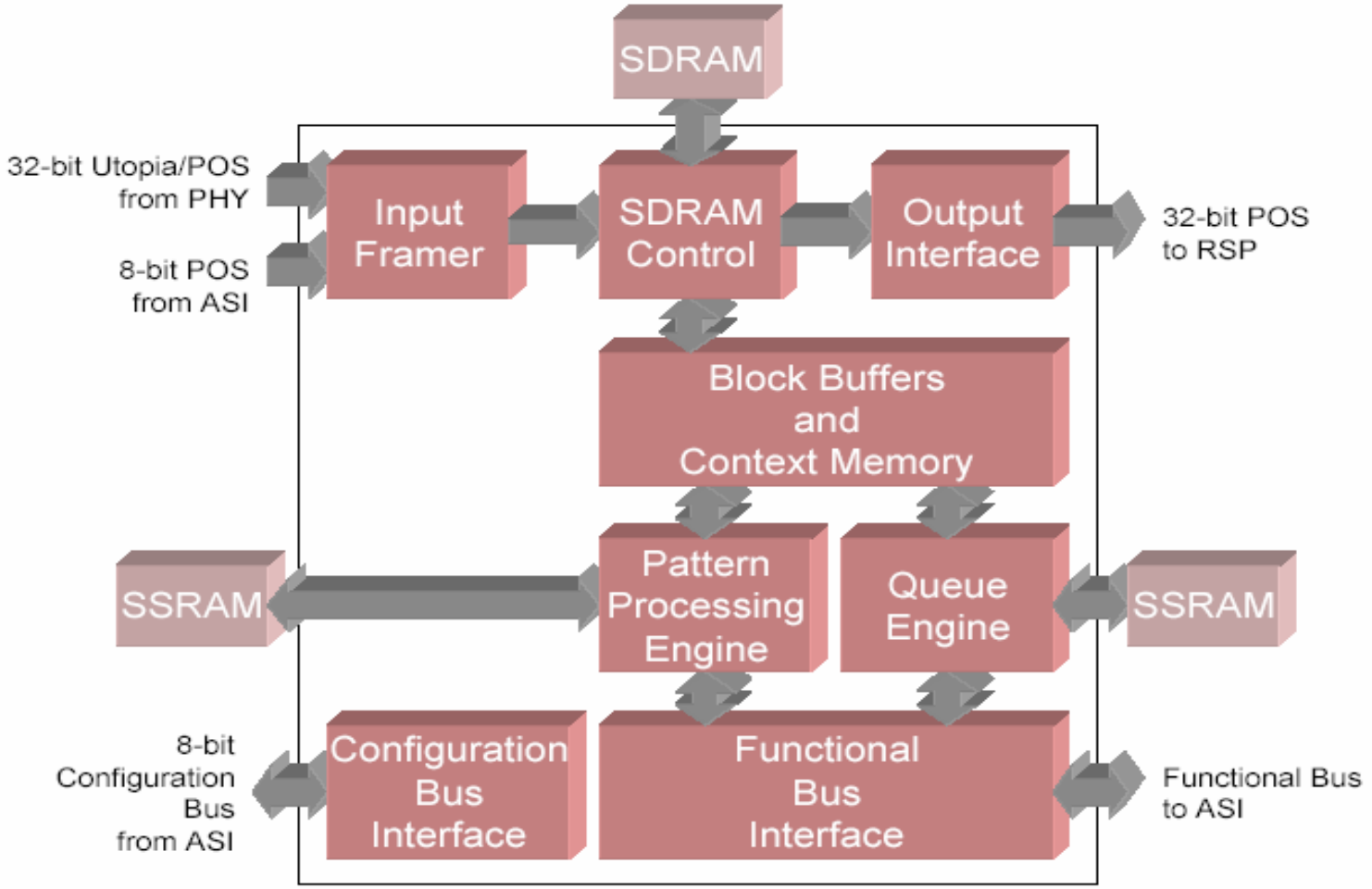
- Recognition, Classification
- Packet Filtering
- Functional Processing
- Assembly if necessary



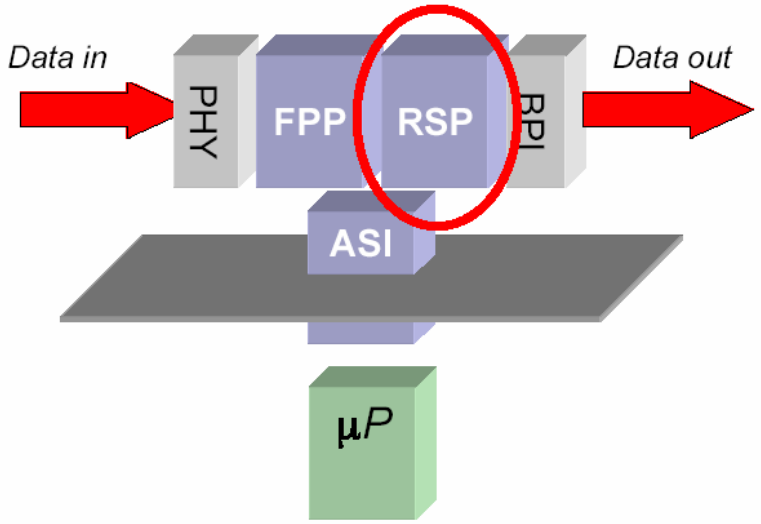
Fast Pattern Processor (FPP)

- Programmable classification up to Layer 7
- High performance scalable architecture
- Highly pipelined multi-threaded processing of PDUs
- Table lookup with millions of entries & variable entry lengths
- Eliminates need for external CAMs;
- Functional Programming Language (FPL) compatible
- Configurable UTOPIA/POS interfaces
- ATM re-assembly at OC-48c rates
- Simplifies design and reduces development cost and time

FPP System Architecture

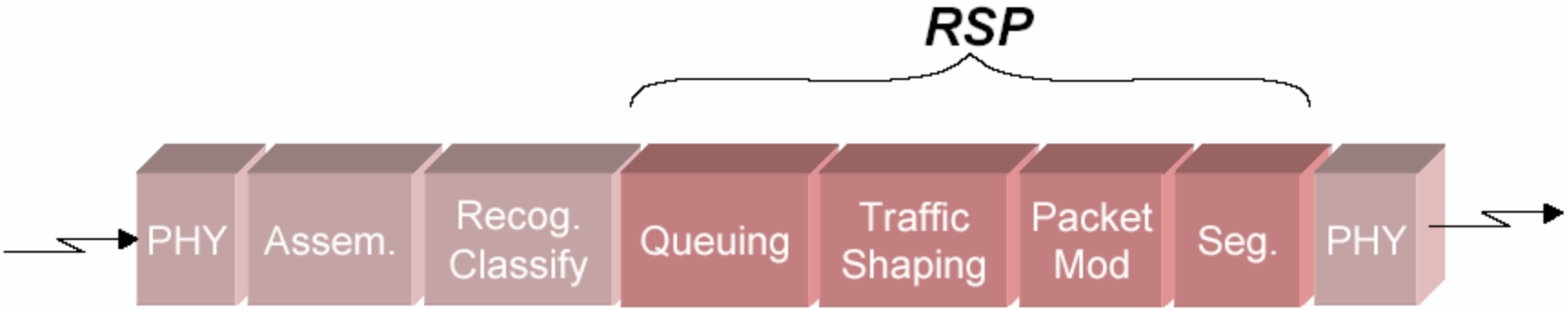


Routing Switch Processor (RSP)



Functions

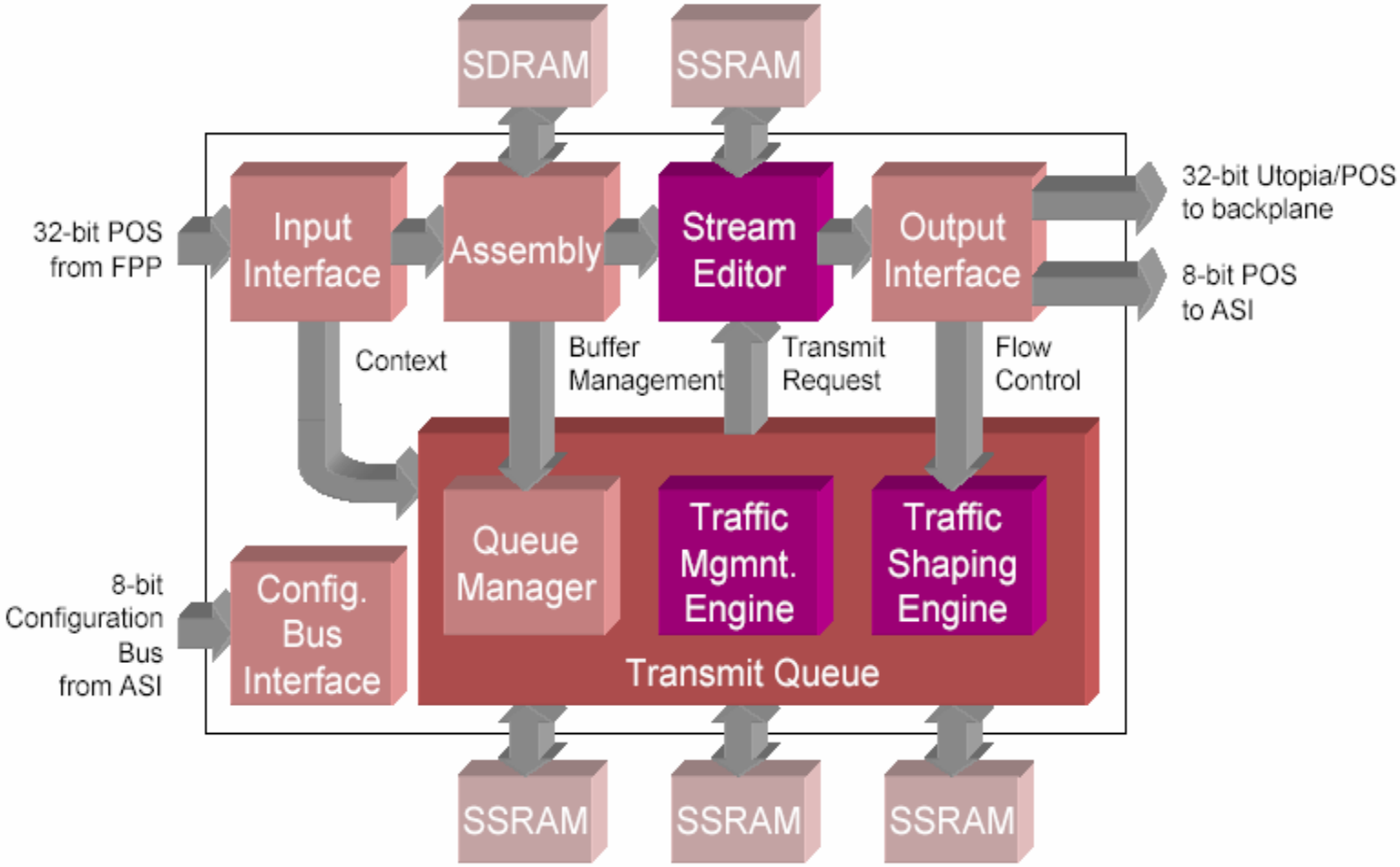
- Transmit queuing
- Quality of Service (QoS)
- Class of Service (CoS)
- Packet Modification including segmentation



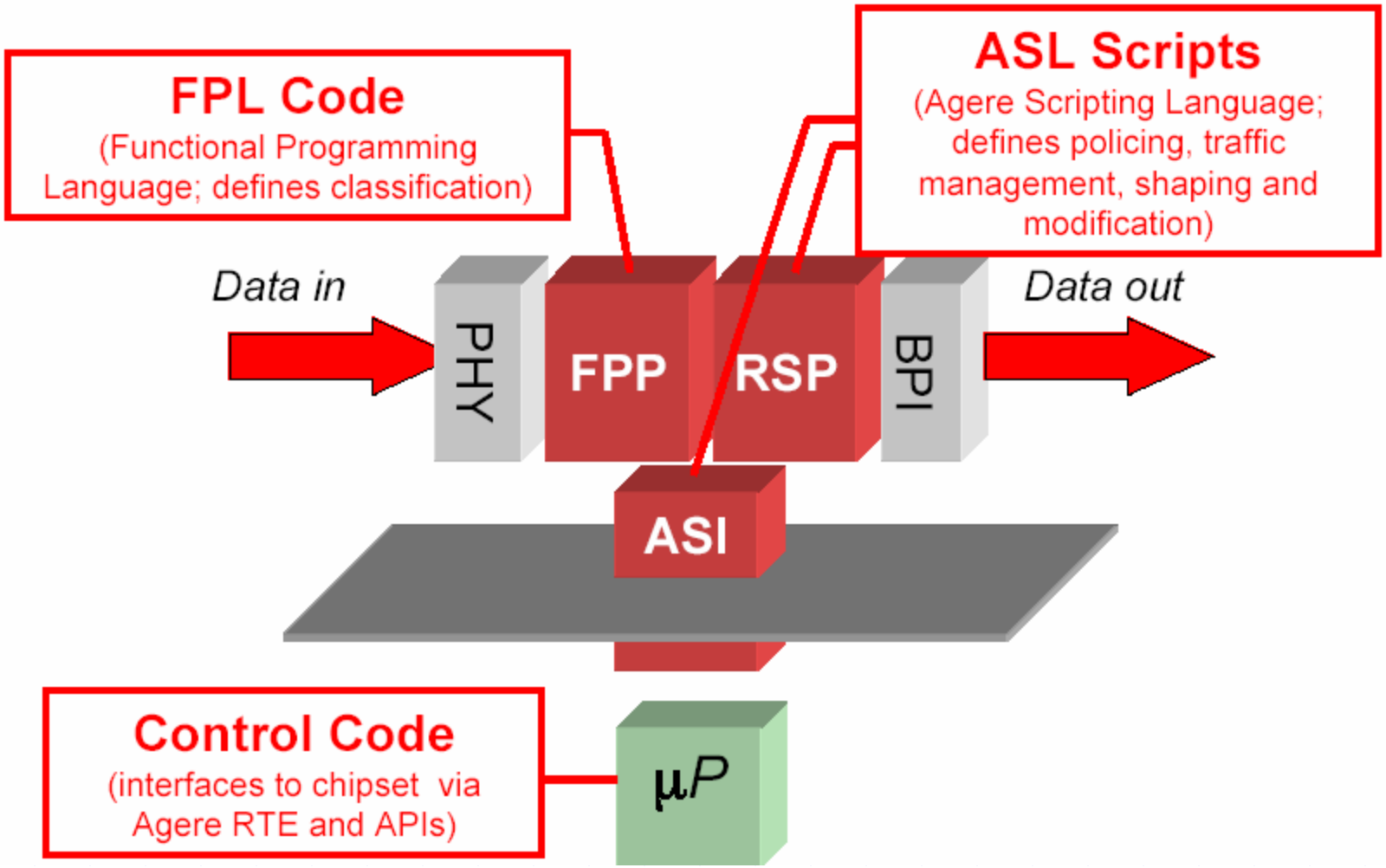
Routing Switch Processor (RSP)

- Programmable packet modifications
  - Discard Policy, QoS, CoS
  - 16 levels of priority
- Support for Multicast
- Generates required CRC/ Checksum
- OC-48c bandwidth
- Support for emerging applications
- High performance architecture – pipelined processing
- Smart processing at very high bandwidths

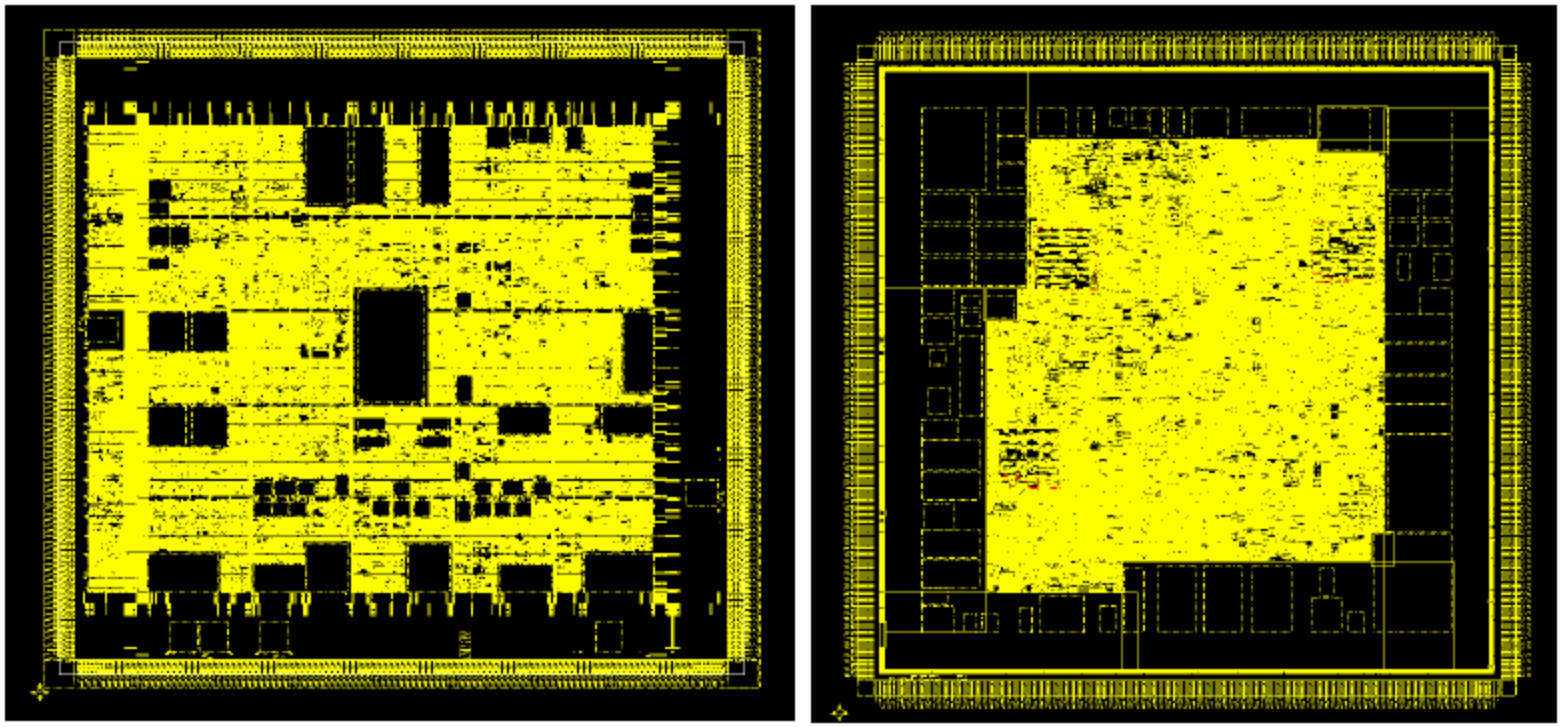
RSP System Architecture



The Software Landscape



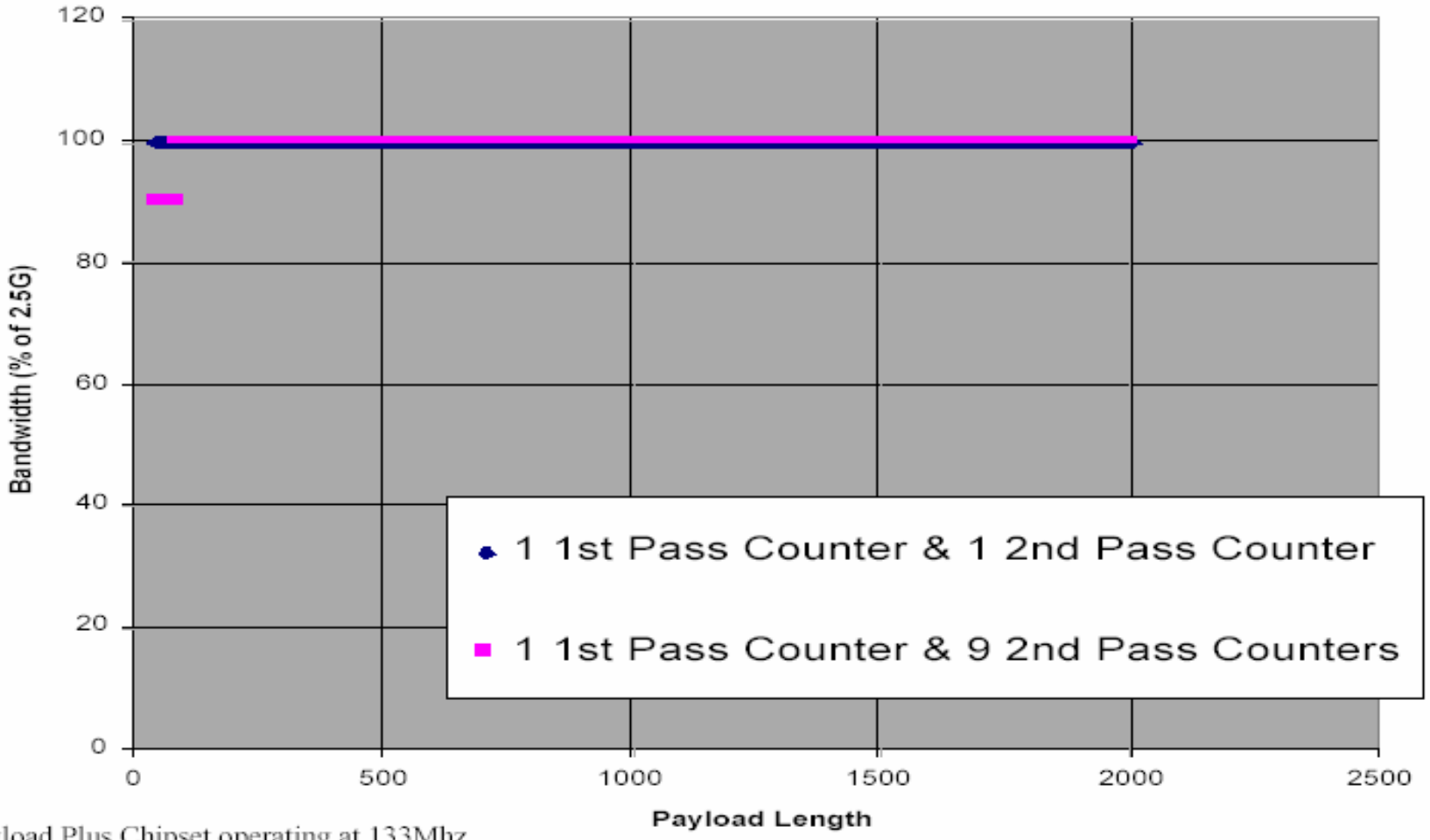
The Chip Details



TSMC 0.18um Technology, Max Power Consumption- 6.2 Watts

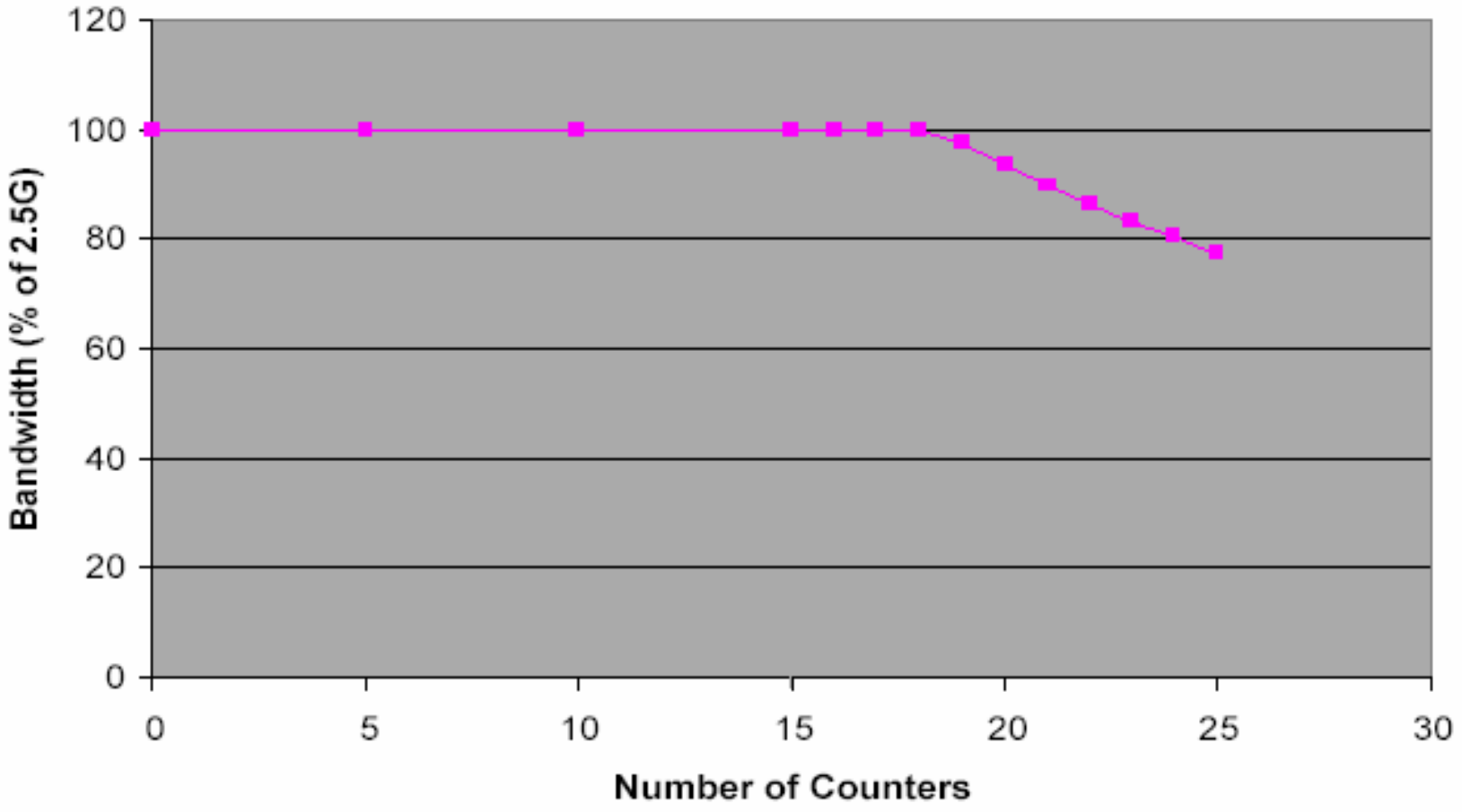
26.4 Million Transistors, 1.33 Million RAM bits

Bandwidth vs. Payload Length



Payload Plus Chipset operating at 133Mhz
IP over ATM over SONET

IPv6 Forwarding (ATM)



Conclusions

- **Value Add Elements:**
  - Classifications
  - Statistics Gathering
  - Buffer Management
  - QoS, CoS Management
  - Data Modifications
- **Overheads:**
  - Linked List and Queue Maintenance
  - Parallel Processing
  - Pipeline Processing

Thank You

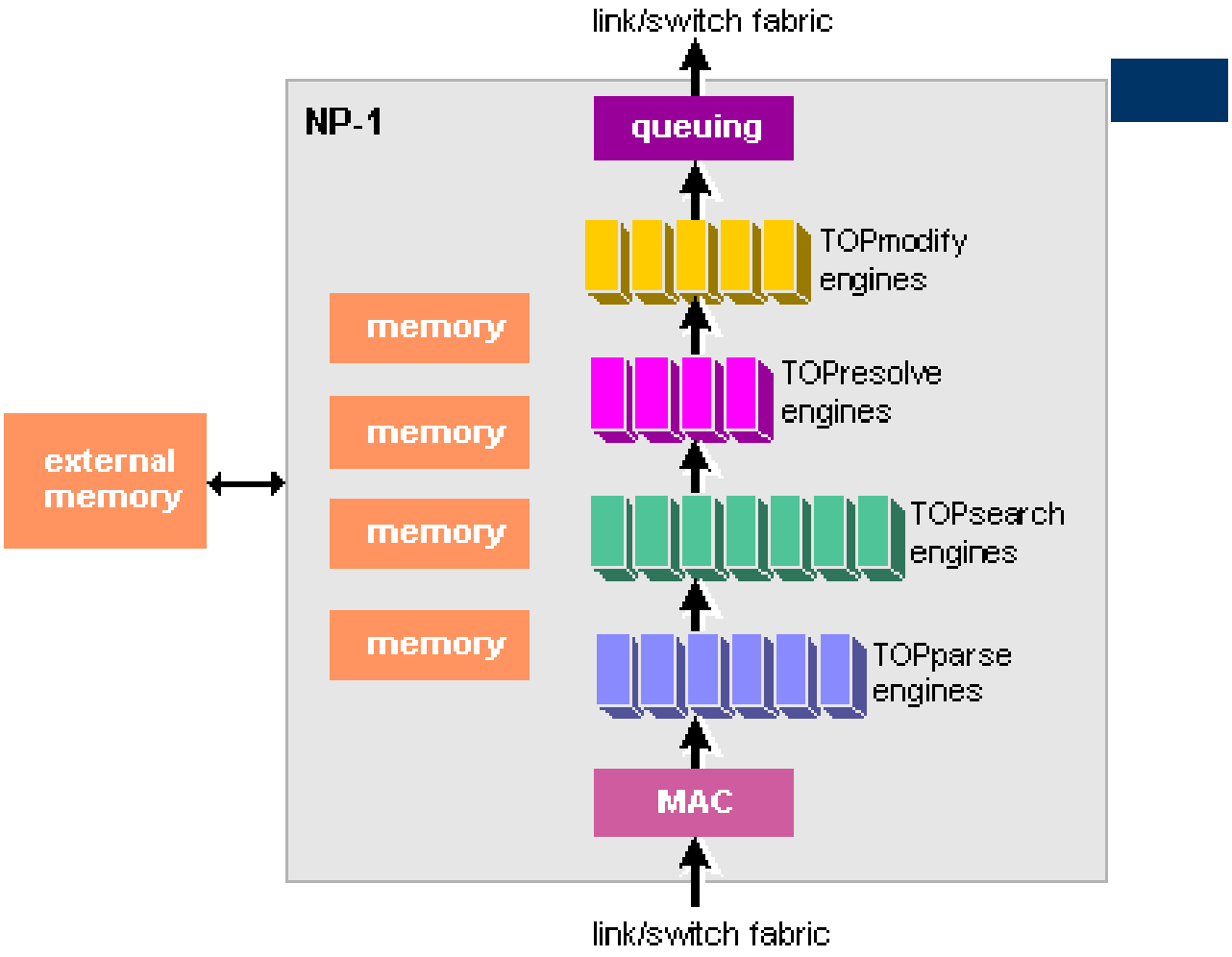
EZchip NP-1

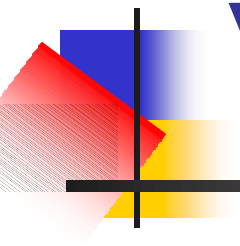
Presented by Hemant Kumar

Ezchip

- Task optimized processors
- 4 types of tasks :parse, search, resolve and modify
- Pipelined
- Superscalar (multiple instances of each processor)
- Multiple Embedded memory cores
- No caches

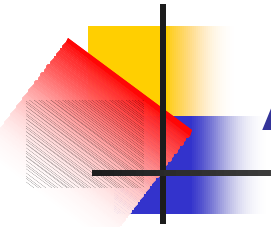
Architecture





Vitesse IQ2000

Youngsuk Jun



Applications

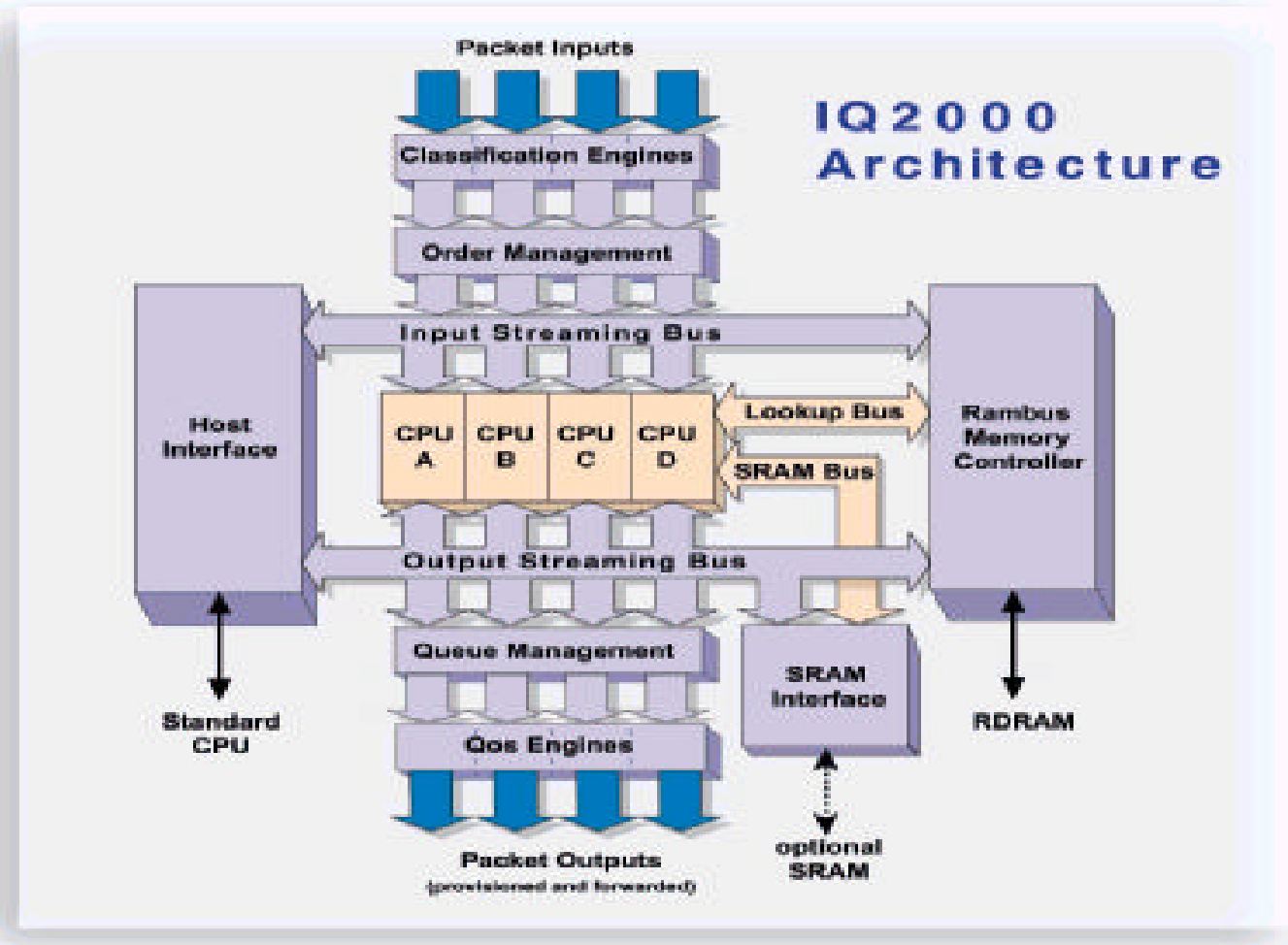
- Complex multi-protocol routing
- QoS
- Classification
- Filtering
- Stateful inspection
- Traffic policing
- Traffic grooming/shaping
- Multicast/stream management
- Address translation

Highlights

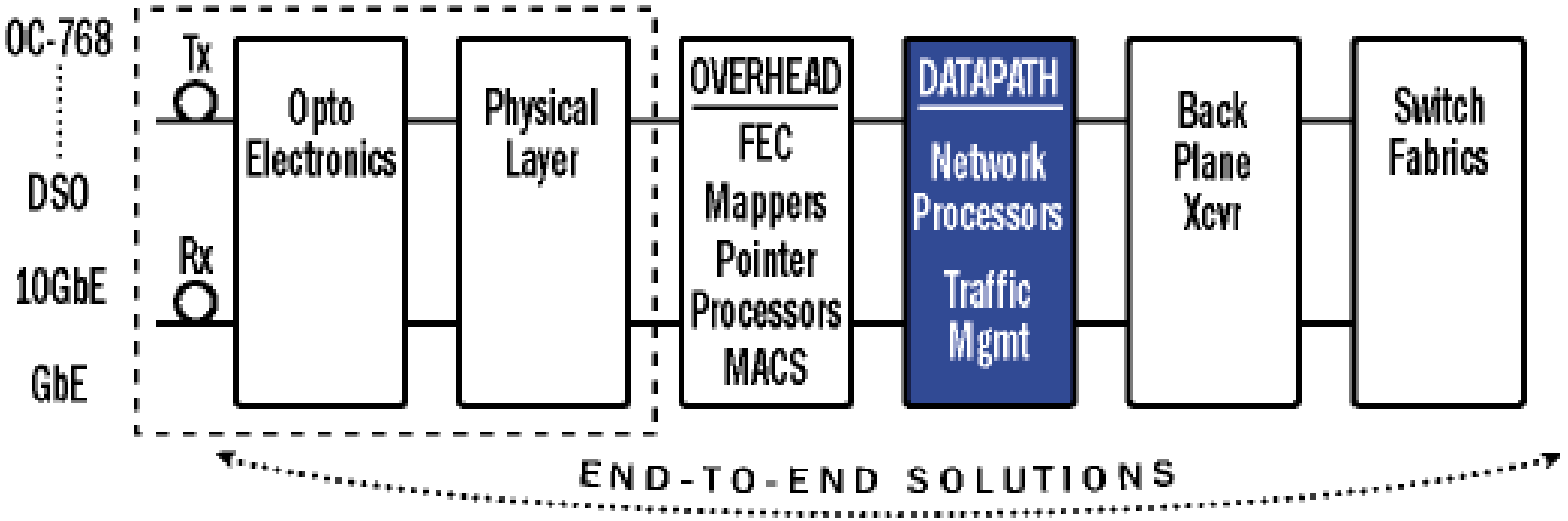
The IQ2000 Family Delivers High Performance Network Processing

Exceptional Processing Capability	**Scaleable Architecture**
■ 4 High Performance CPUs ■ Supports high-speed Interfaces up to OC-48	■ Modular Architecture provides for scaleable growth
Flexibility/Programmability	**Co-Processor**
■ A totally open, programmable solution, for providing next generation services	■ Embedded function specific Co-processors for QoS, Data Movement, Classification, Lookup, and other functions
Headroom	**Open Interconnect**
■ More Headroom than any NPU vendor	■ Open Interconnect via Partner Devices (DS-0 to OC-48) and Fabrics
Control Plane Processor	**Robust Software Development**
■ Match the Standard Processor features/price to meet your requirements	■ Comprehensive Hardware/Software Developers Workbench

Architecture



Solutions


OC-768
DSO
10GbE
GbE
Tx
Rx
Opto Electronics
Physical Layer
OVERHEAD
FEC
Mappers
Pointer Processors
MACS
DATAPATH
Network Processors
Traffic Mgmt
Back Plane Xcvr
Switch Fabrics
END-TO-END SOLUTIONS

Lexra NetVortex

Presented by Ramaswamy Ramaswamy

Lexra
NetVortex PowerPlant (NVP)

ECE 697J, Fall 2002

Features

- OC-192, OC-768 processing (10 Gbps to 40 Gbps)
- 16 LX8380 packet processors (420MHz)
- 128kB on-chip SRAM
- 0.13um process
- 12W typical power dissipation

LX8380 Packet Processing Device

- MIPS ISA based
- Special instructions for packet processing
  - Bit field manipulation
  - Check sum computation
- Hardware multi-threading support (4 threads)
  - Fine grained HMT
- 16 kB I-cache, D-cache
- Crossbar switch allows access of shared resources

LX4580 Processor