Commercial Network Processors

ECE 697J
December 5th, 2002
AMCC nP7250 Network Processor

Presenter: Jinghua Hu
AMCC nP7250

- Released in April 2001
- Packet and cell processing
- Full-duplex OC-48c Network Processor

Nominated for Microprocessor Report Analysts’ Choice Award
General Features

- Offers layer 2, 3, 4 and above packet/cell processing at wire speed
- Supports multi-service cell/packet switching/routing in
  - Clear Channel Mode
  - Multi-Channel Modes
- Wide range of applications
Hardware: nPcore

nPcore Model

- Hardware multi-threading
- Optimized Network Instruction Set Computing
- Zero-cycle context switching
- Four On-chip Coprocessors

- Dual nPcores offer OC-48c bandwidth
Hardware: Co-processors

Four Embedded co-processors

- Packet Transform Engine
- Policy Engine
- Statistics Engine
- Special Purpose Engine
Programming Model

- Fundamentally simplified multi-processor programming model
  - Single-stage, run to completion
  - Each packet/cell executes in a single thread on a single core
  - Facilitate software developers
AMCC solution set

- nP7250 OC-48c Network Processor
- nPX5700 10Gbps Traffic Manager
- nPX5800 40-320Gbps Switch Fabric
Motorola C-5E Network Processor

ECE697J: Active Network

Presenter: Jianhong Xia
12/05/2002
Product Picture

- The C-5e™ Network Processor (NP)
  - Second generation of the C-Port™ family of network processors
  - Most integrated, flexible, and functionally-rich processor
Block Diagram
Features (1)

- Processor & Power Consumption
  - 266MHZ, 9W, 1.2V typical

- Bandwidth & Computing Power
  - 5GBPS, non-blocking throughput, 4,500 MIPS

- RISC Cores & Co-Processors
  - 17 programmable RISC Cores for cell/packet forwarding
  - 32 programmable Serial Data Processors for processing bit streams

- On-chip classification coprocessor
  - supporting over 46 million IPv4 lookups/second
Features (2)

- Flexible interfaces
  - any serial or parallel protocol
  - individual port data rate from DS1 to OC-48c/STM-16
- External C-Port Q-5 TMC (Traffic Management Coprocessor)
  - advanced QoS
- Simple and efficient programming
  - C-language with standard APIs
- Royalty-free reference applications
- Key alliances in
  - fabrics, coprocessors, network software, and design services
Channel Processor

- Consists of
  - Dedicated RISC Core
  - Dual Serial Data Processors (SDPs)
    - Data encoding/decoding
    - Framing / Formatting / Parsing
    - Error checking (CRCs)
    - Control programmable external pin logic
Executive Processor

- Centralized computing resource
- Manages the system interfaces
- Conventional supervisory tasks
  - Reset and initialization of the C-5e NP
  - Program loading and control of CPs
  - Centralized exception handling
  - Management of a host interface through the PCI
  - Management of system interfaces (PCI, Serial Bus, PROM)
Table Lookup Unit

- Classification Engine
  - High-speed, Flexible
  - 46 million IPv4 lookups per second
Queue Management Unit

- Support QoS Management
  - Up to 512 queue to satisfy the traffic management requirements
  - More powerful with Q-5 TMC (Traffic Management Coprocessor)
Buffer Management Unit

- Interfaces to Single Data Rate Synchronous DRAM.
  - Used as buffers for receiving and transmitting data between CPs, the FP, and the XP
  - Used as second level storage in the XP memory hierarchy
Agere Payload Plus

Jayakrishnan Nair
Traditional NP Approach

Custom ICs for wire-speed routing/queuing
- High Development Costs
- Long time to market
- No Flexibility or scalability to support future enhancements (IPv6)
Traditional Methods Insufficient
The Novel Agere's Approach

**Wire-speed Path**
- Forwarding
- Shaping
- Queuing
- SAR
- Monitoring, etc.

**Slow-speed Path**
- Routing protocols
- Error processing
- Statistics reporting
- Configuration, etc.

Have a highly pipelined Chipset for fast Data-Path
How is Agere’s Approach Novel?

- The Payload Plus is a breakthrough 3-chip solution for handling fast traffic, as in OC-48 or Gbps networks.

- Performs all of the classification, policing, traffic management, QoS, traffic shaping and packet modification functions needed for Gbps network platform.

- Focus on wire-speed data stream, by working in tandem with physical interface devices, microprocessors, and backplane fabric offerings.
The Payload Plus Family

Payload plus NPU family has three chips
- Fast Pattern Processor (FPP)
- Routing Switching Processor (RSP)
- Agere System Interface (ASI)

These chips are connected to:
- Physical Layer (PHY) - For Data to Come In
- BackPlane Interface (BPI) – Data Out
- Microprocessor (µP) – For Data Processing
The Payload Plus Chipset

Agere Chipset forms the wire-speed path
Fast Pattern Processor (FPP)

**Functions**
- Recognition, Classification
- Packet Filtering
- Functional Processing
- Assembly if necessary
Fast Pattern Processor (FPP)

- Programmable classification up to Layer 7
- High performance scalable architecture
- Highly pipelined multi-threaded processing of PDUs
- Table lookup with millions of entries & variable entry lengths
- Eliminates need for external CAMs;
- Functional Programming Language (FPL) compatible
- Configurable UTOPIA/POS interfaces
- ATM re-assembly at OC-48c rates
- Simplifies design and reduces development cost and time
FPP System Architecture

- Input Framer
- SDRAM Control
- Output Interface
- Block Buffers and Context Memory
- Pattern Processing Engine
- Queue Engine
- Functional Bus Interface
- Configuration Bus Interface
- SSRAM
- 32-bit Utopia/POS from PHY
- 8-bit POS from ASI
- 8-bit Configuration Bus from ASI
- 32-bit POS to RSP
- Functional Bus to ASI
Routing Switch Processor (RSP)

Functions

- Transmit queuing
- Quality of Service (QoS)
- Class of Service (CoS)
- Packet Modification including segmentation
Routing Switch Processor (RSP)

- Programmable packet modifications
  - Discard Policy, QoS, CoS
  - 16 levels of priority
- Support for Multicast
- Generates required CRC/Checksum
- OC-48c bandwidth
- Support for emerging applications
- High performance architecture – pipelined processing
- Smart processing at very high bandwidths
RSP System Architecture

[Diagram showing the system architecture with various components and connections]

- Input Interface
- Assembly
- Stream Editor
- Output Interface
- Config. Bus Interface
- Queue Manager
- Traffic Mgmt. Engine
- Traffic Shaping Engine
- Transmit Queue

Connections:
- 32-bit POS from FPP
- Context
- Buffer Management
- Transmit Request
- Flow Control
- 32-bit Utopia/POS to backplane
- 8-bit POS to ASI
- 8-bit Configuration Bus from ASI
The Software Landscape

FPL Code
(Functional Programming Language; defines classification)

ASL Scripts
(Agere Scripting Language; defines policing, traffic management, shaping and modification)

Control Code
(interfaces to chipset via Agere RTE and APIs)
The Chip Details

TSMC 0.18um Technology, Max Power Consumption- 6.2 Watts
26.4 Million Transistors, 1.33 Million RAM bits
Bandwidth vs. Payload Length

Payload Plus Chipset operating at 133Mhz
IP over ATM over SONET

ECE 697J - Advanced Topics in Computer Networks
IPv6 Forwarding (ATM)
Conclusions

**Value Add Elements:**
- Classifications
- Statistics Gathering
- Buffer Management
- QoS, CoS Management
- Data Modifications

**Overheads:**
- Linked List and Queue Maintenance
- Parallel Processing
- Pipeline Processing
Thank You
EZchip NP-1

Presented by Hemant Kumar
Ezchip

- Task optimized processors
- 4 types of tasks: parse, search, resolve, and modify
- Pipelined
- Superscalar (multiple instances of each processor)
- Multiple Embedded memory cores
- No caches
Architecture
Applications

- Complex multi-protocol routing
- QoS
- Classification
- Filtering
- Stateful inspection
- Traffic policing
- Traffic grooming/shaping
- Multicast/stream management
- Address translation
The IQ2000 Family Delivers High Performance Network Processing

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<tr>
<th>Exceptional Processing Capability</th>
<th>Scaleable Architecture</th>
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<tr>
<td>■ 4 High Performance CPUs</td>
<td>■ Modular Architecture provides for scaleable growth</td>
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<td>■ Supports high-speed Interfaces up to OC-48</td>
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<th>Flexibility/Programmability</th>
<th>Co-Processor</th>
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<td>■ A totally open, programmable solution, for providing next generation services</td>
<td>■ Embedded function specific Co-processors for QoS, Data Movement, Classification, Lookup, and other functions</td>
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<th>Headroom</th>
<th>Open Interconnect</th>
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<td>■ More Headroom than any NPU vendor</td>
<td>■ Open Interconnect via Partner Devices (DS-0 to OC-48) and Fabrics</td>
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<th>Control Plane Processor</th>
<th>Robust Software Development</th>
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<td>■ Match the Standard Processor features/price to meet your requirements</td>
<td>■ Comprehensive Hardware/Software Developers Workbench</td>
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Architecture

The diagram illustrates the architecture of the IQ2000 system. It features multiple components including:

- Packet Inputs
- Classification Engines
- Order Management
- Input Streaming Bus
- Output Streaming Bus
- Host Interface
- CPU A, CPU B, CPU C, CPU D
- Queue Management
- QoS Engines
- SRAM Interface
- RDRAM

The system also includes a Lookup Bus, SRAM Bus, and an optional SRAM connection. The architecture is designed to manage and process data efficiently, with provisions for packet input and output.
Solutions
Lexra NetVortex

Presented by Ramaswamy Ramaswamy
Lexra
NetVortex PowerPlant (NVP)

ECE 697J, Fall
2002
Features

OC-192, OC-768 processing (10 Gbps to 40 Gbps)
16 LX8380 packet processors (420MHz)
128kB on-chip SRAM
0.13um process
12W typical power dissipation
LX8380 Packet Processing Device

MIPS ISA based
Special instructions for packet processing
    Bit field manipulation
    Check sum computation
Hardware multi-threading support (4 threads)
    Fine grained HMT
16 kB I-cache, D-cache
Crossbar switch allows access of shared resources
LX4580 Processor