A Methodology and Simulator for the Study of Network Processors

ECE 697J

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Introduction

- Why do we want to simulate a system?
- What should we simulate in an NP?

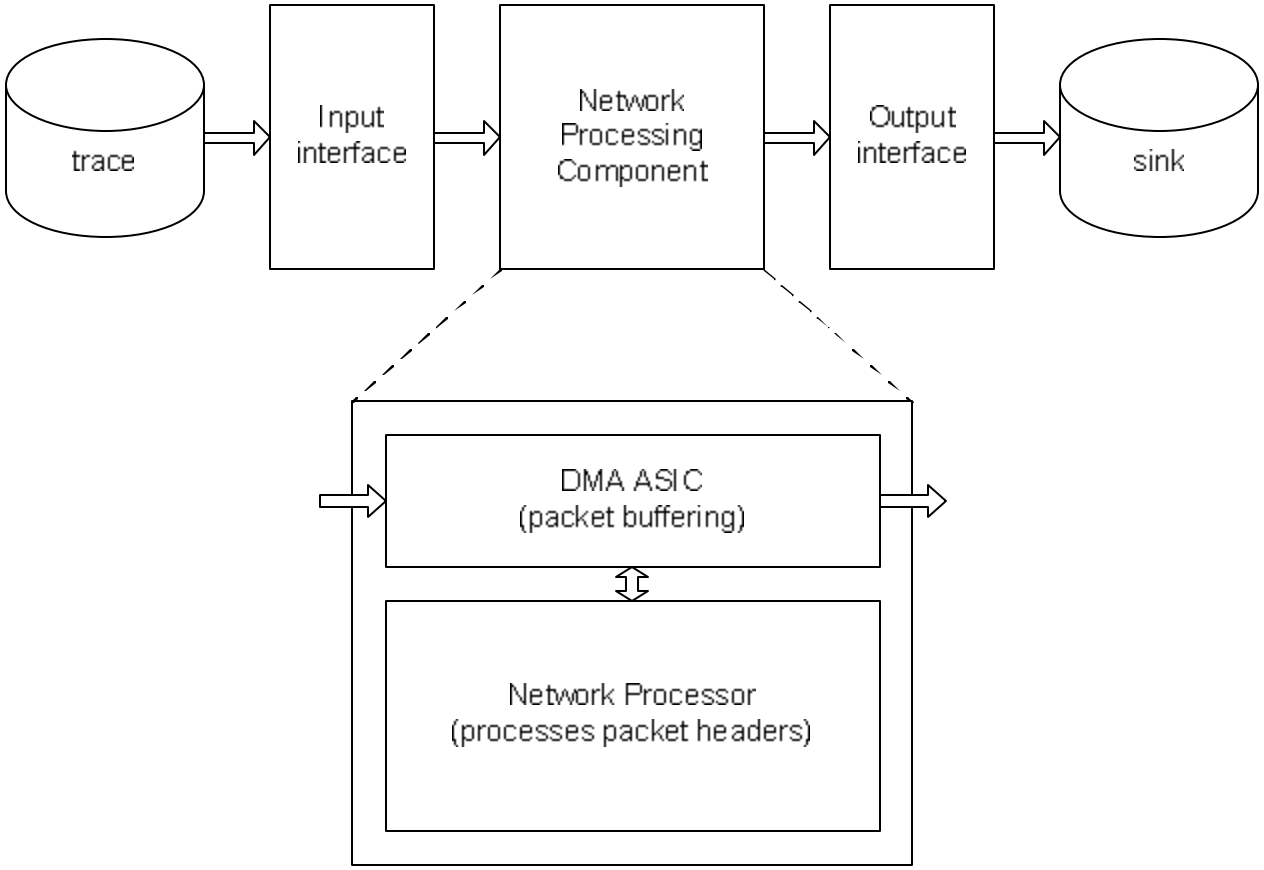
Simulation

- Cheaper than building hardware
- Get understanding of
  - Behavior
  - Performance
  - Timing
- Explore configurations that are not feasible today
  - Next generations CMOS
  - Scalability

NP Simulation

- What to simulate?
  - Depends.
- Examples:
  - Processors
  - Network traffic
  - Memory subsystem
  - Switching fabric
- Combination of all: full system simulator
  - Paper calls it “holistic”
- Other approaches: only components
  - E.g., CommBench is “mircorarchitect’s approach”

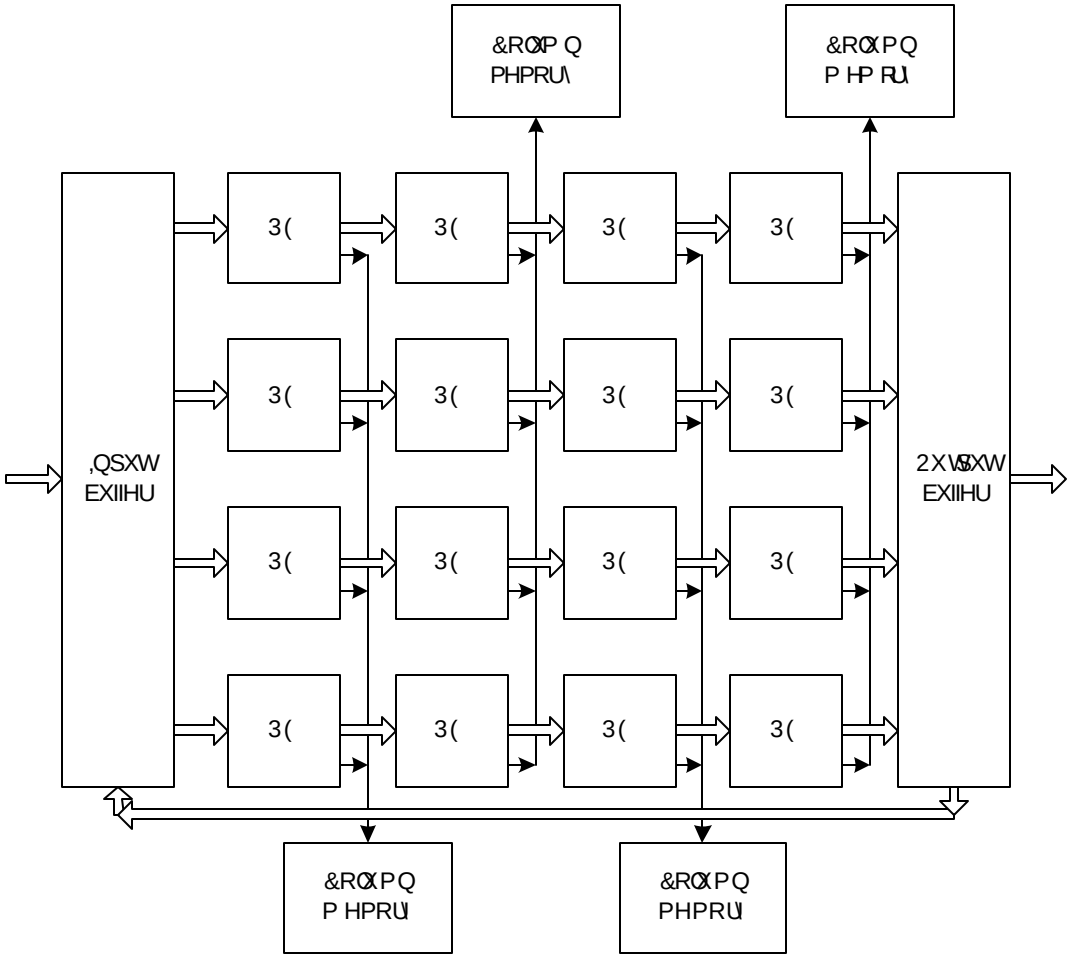
Component Network Simulator



Traces

- Network traffic that is fed to simulator
- Real traces:
  - Collected on real networks
  - Usually hard to obtain
- Synthetic traces:
  - Generated by network model
  - Can be scaled nicely
  - Do not contain packet payload
  - Usually based on traffic self-similarity

Cisco Toaster



Cisco Toaster

- 16 VLIW processors
  - ISA “optimized for network processing”: lookups, bit level ops, …
- Each column executes same code
  - Phase-shifted to avoid memory conflicts
- Memory system
  - 12kB instruction memory
  - 64 byte data cache
  - On-chip memory for “context”
  - Column-memory: 16kB on-chip, 256MB off-chip

Simulator Implementation

- C++ classes representing different Toaster components:
  - Cores, columns, buffers, memories
- Processors:
  - Count cycles and simulates stalls
- Memories:
  - Detailed modeling of memory transaction
- Paper claims “real-time simulator”

DiffServ Application

- Several classes of flows
  - WRR scheduler
- Main issues:
  - Constraint cycle budget (why?)
  - Deterministic behavior
- Make sure serviceable item can be found quickly

Results

- 100000 packets of 21 flows
- Measured delay and jitter
- Ideal memory system:
  - Delay: 2-18 ms
  - Jitter: 5-10 ms
- Real memory system:
  - Delay: 3-28ms
  - Jitter: 6-19ms
- Input rate definition is unclear:
  - How can 21 flows have 500+Mbps on four OC12 ports?

Summary

- Simulators are useful
  - Allows to experiment with architectures and applications
- Difficult to find balance between details and architecture-independence
- Simulations need to be described in detail to be meaningful

Next Class

- Design Space Exploration
  - Evaluation architectures analytically – not with simulations.