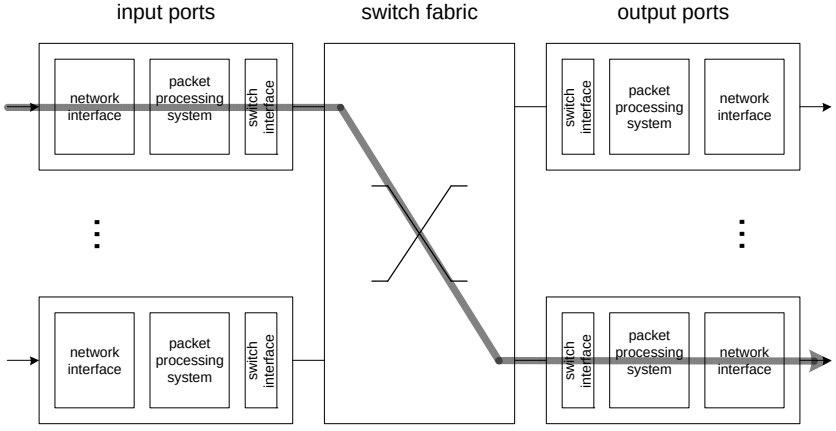
# ECE 671 – Lectures 22

Specialized hardware and
Runtime support

# Packet processing in network systems

- Protocol operations implemented on input port



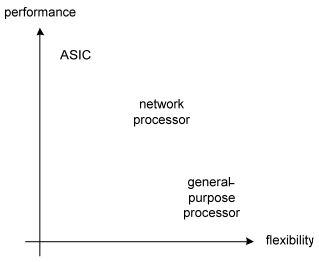
# Packet processor

- How to implement packet processing?



# Packet processor

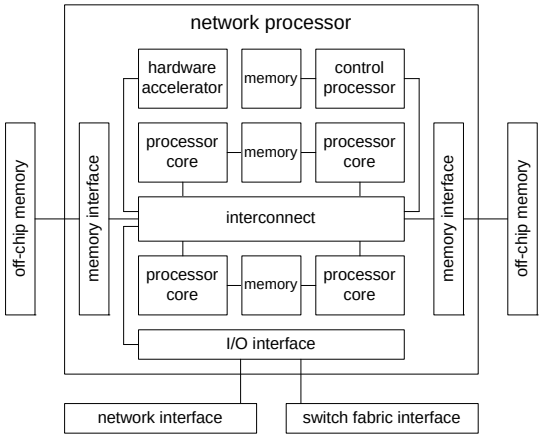
- Tradeoffs between hardware and software
  - Custom hardware: ASIC
  - Software: workstation processor or network processor




- How can processor be optimized for networking?

# Network processor

- System architecture:

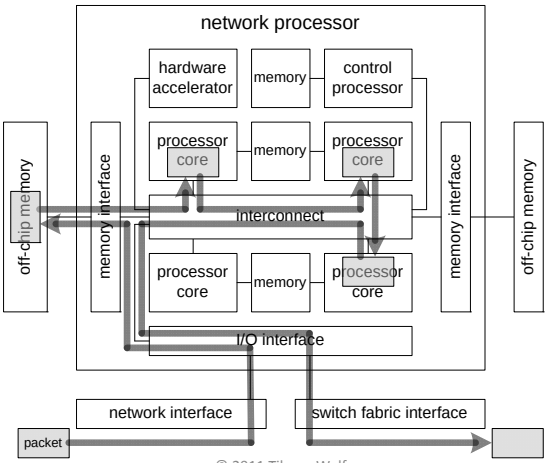







# Network processor

- Operation:



# Example network processors

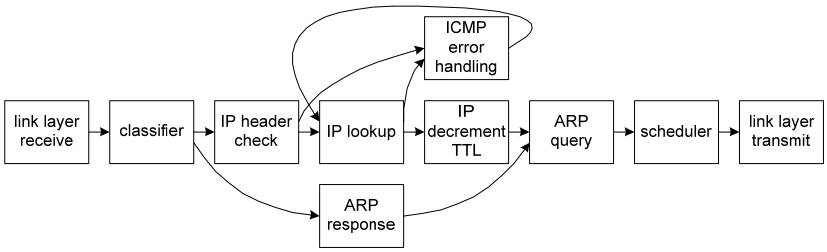
| | Intel IXP2855 | Cisco QuantumFlow | Cavium CN5860 |
|---|---|---|---|
| **Maximum throughput** | 10Gbps | 20Gbps | 20Gbps |
| **Data path processors** | 16 32-bit RISC processors, 8 threads per processor, up to 1.5GHz | 40 32-bit RISC processors, 4 threads per processor, up to 1.2GHz | 16 64-bit RISC processors, up to 800MHz |
| **On-chip memory** | 32kB instruction and 32kB data memory per processor | 16kB cache per processor, 256kB shared cache | 32kB instruction cache and 8kB data cache per processor, 2MB shared cache |
| **Control processor** | 32-bit XScale RISC core, 32kB instruction cache, 32kB data cache, up to 750MHz | Off-chip | Off-chip |
| **External memory interfaces** | 3 DRAM interfaces, 4 SRAM interfaces | DRAM, SRAM, and TCAM interfaces | DRAM and TCAM interfaces |
| **Hardware accelerators** | Cryptographic co-processor | Classification, traffic policing, etc. | Cryptographic co-processor, TCP acceleration, regular expression matching, etc. |
| **Maximum power dissipation** | 32W | 80W | 40W |





# Processing workload

- What does packet processing look like?
  - Many components
  - Processing differs based on packet

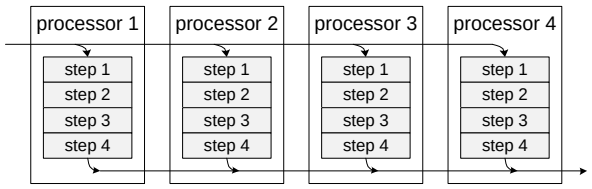



- How to spread workload over processor cores?

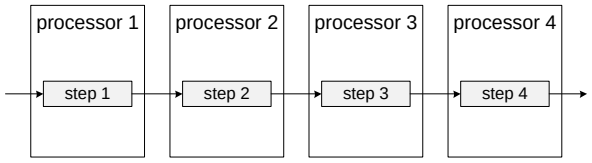
# Processing models

- Splitting workload across cores:

Run-to-completion




Pipelining

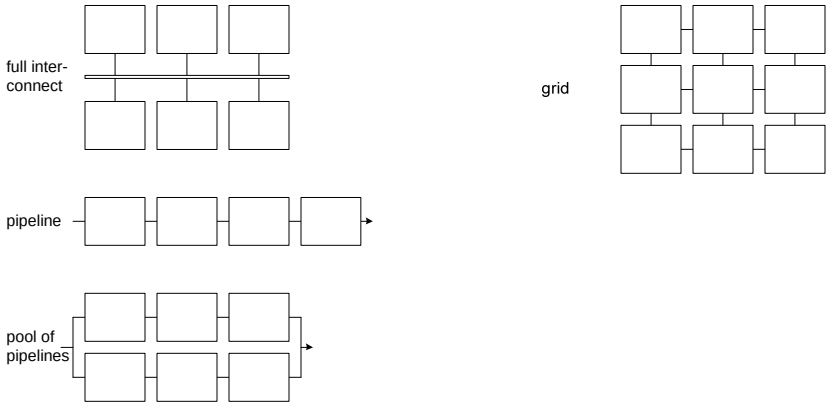







# Network processor topologies

- Different logical or physical arrangements of cores



# Hardware accelerators

- Custom logic components for network functions
  - Lookup and classification (e.g., TCAM)
  - Pattern matching
  - Cryptographic co-processor
  - Compression and decompression
  - XML processing
- Tradeoff between performance gain and space
  - Only highly utilized accelerator is worthwhile



# A look back…