ECE 671 – Lectures 22

Specialized hardware and Runtime support

Packet processing in network systems

• Protocol operations implemented on input port
Packet processor

• How to implement packet processing?

Packet processor

• Tradeoffs between hardware and software
  – Custom hardware: ASIC
  – Software: workstation processor or network processor

• How can processor be optimized for networking?
Network processor

• System architecture:

Network processor

• Operation:
### Example network processors

<table>
<thead>
<tr>
<th></th>
<th>Intel IXP2855</th>
<th>Cisco QuantumFlow</th>
<th>Cavium CN5860</th>
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</thead>
<tbody>
<tr>
<td><strong>Maximum throughput</strong></td>
<td>10Gbps</td>
<td>20Gbps</td>
<td>20Gbps</td>
</tr>
<tr>
<td><strong>Data path processors</strong></td>
<td>16 32-bit RISC processors, 8 threads per processor, up to 1.5GHz</td>
<td>40 32-bit RISC processors, 4 threads per processor, up to 1.2GHz</td>
<td>16 64-bit RISC processors, up to 800MHz</td>
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<tr>
<td><strong>On-chip memory</strong></td>
<td>32kB instruction and 32kB data memory per processor</td>
<td>16kB cache per processor, 256kB shared cache</td>
<td>32kB instruction cache and 8kB data cache per processor, 2MB shared cache</td>
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<tr>
<td><strong>Control processor</strong></td>
<td>32-bit XScale RISC core, 32kB instruction cache, 32kB data cache, up to 750MHz</td>
<td>Off-chip</td>
<td>Off-chip</td>
</tr>
<tr>
<td><strong>External memory interfaces</strong></td>
<td>3 DRAM interfaces, 4 SRAM interfaces</td>
<td>DRAM, SRAM, and TCAM interfaces</td>
<td>DRAM and TCAM interfaces</td>
</tr>
<tr>
<td><strong>Hardware accelerators</strong></td>
<td>Cryptographic co-processor</td>
<td>Classification, traffic policing, etc.</td>
<td>Cryptographic co-processor, TCP acceleration, regular expression matching, etc.</td>
</tr>
<tr>
<td><strong>Maximum power dissipation</strong></td>
<td>32W</td>
<td>80W</td>
<td>40W</td>
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</table>

### Processing workload

- **What does packet processing look like?**
  - Many components
  - Processing differs based on packet

- **How to spread workload over processor cores?**
Processing models

• Splitting workload across cores:
  - Run-to-completion
  - Pipelining

Network processor topologies

• Different logical or physical arrangements of cores
  - Full inter-connect
  - Grid
  - Pipeline
  - Pool of pipelines
Hardware accelerators

- Custom logic components for network functions
  - Lookup and classification (e.g., TCAM)
  - Pattern matching
  - Cryptographic co-processor
  - Compression and decompression
  - XML processing
- Tradeoff between performance gain and space
  - Only highly utilized accelerator is worthwhile

A look back...