

ECE 558/658 VLSI Design Flow

Lecture 2
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TA web-site

- http://vsp2.ecs.umass.edu/vspg/658/TA_Tools/
- TA information
- How to use Cygwin to run X applications on remote UNIX machine.
- Useful links for
 - Models and Tools
 - Design rules
 - Hand calculation parameters
 - Examples!!!!
- Etc.

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Full custom design vs. standard cell design

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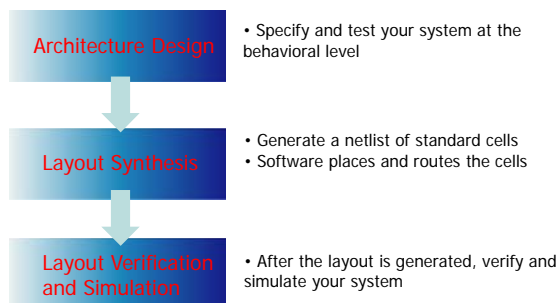
Design Methodology

- **Full Custom:** The designer creates layout masks by hand.
 - **Standard Cell:** The designer uses high level programming language (eg. Verilog) to describe the system and lets the computer make the masks.
- | | |
|---------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------|
| <ul style="list-style-type: none"> • Long design cycle • Potentially fastest and most power efficient designs | <ul style="list-style-type: none"> • Shorter design cycle • Less efficient designs |
|---------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------|

http://vsp2.ecs.umass.edu/vspg/658/TA_Tools/design_flow.html

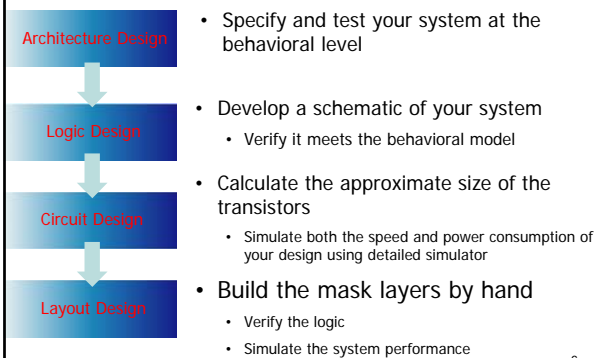
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Standard Cell Design



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Full Custom



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Architecture Design

```

    graph TD
      A[Architecture Design] --> B[Logic Design]
      B --> C[Circuit Design]
      C --> D[Layout Design]
  
```

- Goal: Create a high-level (Behavioral) representation of your system
 - Tools: Verilog, VHDL, System C
 - Synthesizable (PLD's and/or ASIC)
 - Non-synthesizable
 - More in future lectures

<Full custom flow>

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Logic Design and Verification

```

    graph TD
      A[Architecture Design] --> B[Logic Design]
      B --> C[Circuit Design]
      C --> D[Layout Design]
  
```

- Translate system level description into transistors
 - Many logic styles
 - Schematic representation
- Logic verification
 - Simplistic models - to verify functionality
 - Fast - can run many cases
- Use Verilog or IRSIM
 - [schm2vlog.pl](#) : convert schematic netlist to verilog netlist
 - [schm2sim.pl](#) : convert schematic netlist to IRSIM netlist

<Full custom flow>

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Circuit Design

```

    graph TD
      A[Architecture Design] --> B[Logic Design]
      B --> C[Circuit Design]
      C --> D[Layout Design]
  
```

- Calculate transistor sizes
- Performance evaluation
 - Complex models - to evaluate timing and power
 - Slow - run only selected cases
- Use HSPICE

<Full custom flow>

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Layout

```

    graph TD
      A[Architecture Design] --> B[Logic Design]
      B --> C[Circuit Design]
      C --> D[Layout Design]
  
```

- Translate schematic to layout
 - Need to know the [design rules](#)
 - Layout representation may not be similar to schematic
- Logic verification
 - Compare netlists (Layout vs. Schematic, LVS)
 - Simulators (IRSIM)
- Performance evaluation
 - Use HSPICE

<Full custom flow>

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Client – server computing

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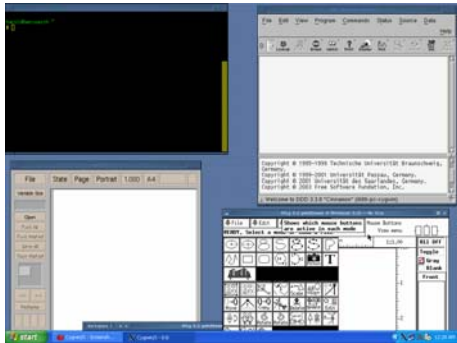
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Client – server computing

- Network transparency: the machine where application programs run need not be the user's local machine.
- Examples
 - Microsoft Windows Remote Desktop
 - Virtual Network Computing
 - X11

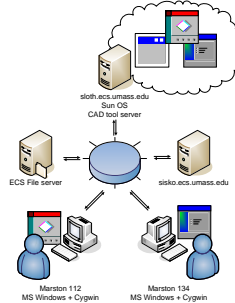
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What is X-Windows?



<http://x.cygwin.com/screenshots/> Visit [Wikipedia](http://en.wikipedia.org/wiki/X_Window_System) to learn about X windows system.¹³

How to run X application on remote UNIX machine?



- All CAD tools are installed in sloth.ecs.umass.edu.
- Students can access CAD tools by using MS Windows machine and Cygwin.

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Full custom example (2 input nor gate)

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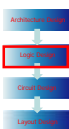
ssh to sloth.ecs.umass.edu

1. ssh username@sloth.ecs.umass.edu
 - http://vsp2.ecs.umass.edu/vspg/658/TA_Tools/cygwin/in/cygwin.html
2. tcsh
3. emacs&
4. cd vlsix
5. ls
 - Directory structure
 - http://vsp2.ecs.umass.edu/vspg/658/TA_Tools/other/tools.html

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Logic Design and Verification

- http://vsp2.ecs.umass.edu/vspg/658/TA_Tools/cadence/Schematic.html
- http://vsp2.ecs.umass.edu/vspg/658/TA_Tools/irsim/irsim.html
- http://vsp2.ecs.umass.edu/vspg/658/TA_Tools/cadence/verilog2.html



1. 2 input nor gate truth table
2. Truth table into a schematic (icms)
3. Logic verification
 - Use Verilog or IRSIM
 - [schm2vlog.pl](#) : convert schematic netlist to verilog netlist
 - [schm2sim.pl](#) : convert schematic netlist to IRSIM netlist.

a	b	c
0	0	1
0	1	0
1	0	0
1	1	0

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Circuit Design

- http://vsp2.ecs.umass.edu/vspg/658/TA_Tools/cadence/Schematic.html
- http://vsp2.ecs.umass.edu/vspg/658/TA_Tools/hspice/hspice.html



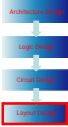
1. Calculate and change transistor sizes (icms)
 - RCN chapter 6 "static CMOS design"
2. Performance evaluation (HSPICE)
 - [schm2sim.pl](#) : convert schematic netlist to IRSIM netlist.
 - **CAUTION: do not overwrite your nor2x1irsim simulation directory during extraction.**

a	b	c
0	0	1
0	1	0
1	0	0
1	1	0

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Layout

http://vsp2.ecs.umass.edu/vspg/658/TA_Tools/cadence/Vertuoso.html
http://vsp2.ecs.umass.edu/vspg/658/TA_Tools/cadence/LVS.html
http://vsp2.ecs.umass.edu/vspg/658/TA_Tools/irsim/irsim.html
http://vsp2.ecs.umass.edu/vspg/658/TA_Tools/hspice/hspice.html



- Translate schematic to layout (layoutPlus)
 - **Design rules**: RCN Chapter 1
- Logic verification (LVS, IRSIM)
 - Layout vs. Schematic (LVS)
 - Simulators (IRSIM)
- Performance evaluation with parasitic capacitance and resistance (HSPICE)
 - **CAUTION: do not overwrite your nor2x1schm simulation directory during extraction.**

a	b	c
0	0	1
0	1	0
1	0	0
1	1	0

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Thank you

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