Russell Tessier

Professor and Associate Dean

Department of Electrical and Computer Engineering
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Research Interests

My research interests are in the areas of field-programmable architectures, VLSI, and high-performance and parallel computer architecture. I am particularly interested in the integration of these fields to support embedded systems.

Academic Positions

University of Massachusetts ..... Amherst, MA

Associate Dean	College of Engineering	1/17 - present
Professor	Electrical and Computer Engineering	9/12 - present
Associate Professor	Electrical and Computer Engineering	9/04 - 8/12
Assistant Professor	Electrical and Computer Engineering	1/99 - 9/04

Education

Massachusetts Institute of Technology ..... Cambridge, MA

Ph.D.	Electrical Engineering and Computer Science	1999
S.M.	Electrical Engineering and Computer Science	1992

Rensselaer Polytechnic Institute ..... Troy, NY

B.S.	Computer and Systems Engineering	1989

Current Research

University of Massachusetts ..... Amherst, MA

1/99 – present

I am currently the head of the UMass Reconfigurable Computing Group. This research effort involves six students. Current research topics include: reconfigurable architectures, FPGA security, and FPGA-based applications, such as radar processing and network function virtualization.

Other Research Experience

Université de Rennes ..... Lannion, France

6/13

Visiting Researcher – I assisted Prof. Olivier Sentieys in designing partially-reconfigurable FPGA architectures.

Université de Bretagne Sud ..... Lorient, France

6/11 – 7/11
5/08 – 6/08
6/07 – 7/07

Visiting Researcher – I assisted Prof. Guy Gogniat in developing new security protocols for FPGA-based embedded systems.

University of Toronto ..... Toronto, ON, Canada

1/05 – 12/05

Visiting Professor – I assisted Prof. Jonathan Rose in creating new FPGA architectures and CAD algorithms during a one-year sabbatical appointment.

CASA Engineering Research Center - UMass ..... Amherst, MA

10/03 – 12/06 Project Leader – I supervised the development and implementation of an FPGA-based digital acquisition system which is an integral part of a weather sensing system. To date, five weather radar systems which include the data acquisition system have been deployed in Oklahoma and Massachusetts. The systems are currently being used in weather prediction and tornado detection.

Massachusetts Institute of Technology ..... Cambridge, MA

12/93 – 10/98 Fast Floorplanning and Routing Algorithms – My doctoral thesis examined algorithmic techniques to reduce place and route time for large field programmable gate arrays (FPGAs). To support this work, I implemented an FPGA layout system called *Frontier* that rapidly evaluates place and route tradeoffs for hierarchical RTL designs. Advisor: Steven Ward.

11/92 – 12/93 Virtual Wires Logic Emulation – I designed and implemented the hardware for an FPGA-based logic emulation system. This scalable system uses an inter-FPGA communication protocol based on static scheduling to overcome limited device pin resources. The hardware and software for this project were later commercialized by Virtual Machine Works.

1/90 – 10/92 NuMesh Parallel Processing – I was a member of the NuMesh group, which worked to design, implement, and explore statically-scheduled multiprocessor routing. My specific contributions to this research included the specification of a hardware communication protocol and the design and implementation of a Sparc-based processing element, high-speed frame buffer, and host computer interface card.

Rensselaer Polytechnic Institute ..... Troy, NY

9/88 – 5/89 Image Processing – I designed an analog signal acquisition board for an ultrasound imaging system.

Teaching Experience

University of Massachusetts ..... Amherst, MA

1/99 – Present Course instructor for *Hardware Organization and Design*, *Data Structures*, *Introduction to Programming for ECE*, *Introduction to Electrical and Computer Engineering*, *Computer Systems Laboratory II*, *Reconfigurable Computing*, *Senior Design Project*, *Graduate Design Project*, *Foundations of Computer Engineering*, and *Parallel Computer Architecture*.

University of Toronto ..... Toronto, ON

9/05 – 12/05 Course instructor for *Reconfigurable Computing*.

Massachusetts Institute of Technology ..... Cambridge, MA

5/93 – 12/97 Junior faculty instructor for *Computation Structures*

9/89 – 5/92 Teaching assistant for *Parallel Processing*, *Microcomputer Project Laboratory*, *Dynamic System Control*, and *Computation Structures*

Industry Experience

Mentor Graphics (formerly Ikos Systems) ..... Waltham, MA

11/08 – 1/09 *Systems Design Consultant*. Involved in the design, implementation, and evaluation of FPGA-based
5/96 - 9/01 logic emulation systems. Hardware design and FPGA evaluation were important aspects of the job.

Altera Corporation ..... Toronto, ON

1/05 - 9/05 *Software Engineer*. Developed power-aware computer-aided design algorithms for FPGA embedded memory mapping and logic block placement.

Prosensing, Inc. ..... Amherst, MA

9/00 - 1/04 *Hardware Design Consultant.* Assisted in the development and debug of digital data acquisition systems.

Altera Corporation ..... San Jose, CA

10/01 - 4/02 *Consultant.* Expert witness in a civil lawsuit.

Virtual Machine Works ..... Cambridge, MA

1/94 - 5/96 *Founder and Principal Engineer.* One of three founders of a logic emulation company based on research performed at MIT. I aided in the design and development of FPGA-based emulation hardware. The company was acquired by Ikos Systems in May 1996.

BBN Corporation ..... Cambridge, MA

6/92 - 1/94 *Hardware Engineer.* Designed a multiprocessing node for a satellite land station. I performed all component selection, schematic entry, and verification for the design.

Data General Corporation ..... Westboro, MA

5/89 - 8/89 *Software Engineer.* Assisted in the development of a debugging tool for a RISC-based, fault-tolerant computer system.

Patents

Russell Tessier, Vaughn Betz, Thiagaraja Golpalsamy, and David Neto, "Power-Aware RAM Processing." U.S. patent 9330733, May 3, 2016.

Russell Tessier, Vaughn Betz, Thiagaraja Golpalsamy, and David Neto, "Power-Aware RAM Processing." U.S. patent 7877555, January 25, 2011.

Anant Agarwal, Jonathan Babb, and Russell Tessier, "Virtual Interconnection for Reconfigurable Logic Systems." U.S. patent 5761484, June 2, 1998.

Anant Agarwal, Jonathan Babb, and Russell Tessier, "Virtual Interconnection for Reconfigurable Logic Systems." U.S. patent 5596742, January 21, 1997.

Service

Co-Editor, book: Highlights of the First Twenty Years of the IEEE Symposium on FCCMs, 2013
Co-Editor, special issue: EURASIP Journal of Embedded Systems, 2006
Co-Editor, special issue: Journal of VLSI Signal Processing, January 2004
Advisor, Eta Kappa Nu, University of Massachusetts, Amherst, 2003 - 2004, 2006 - 2008
Co-General Chair, FCCM'2010
Co-Program Chair, FCCM'2009
Program Committee, FCCM'2007 - 2018
Finance Chair, FPGA'2005
General Chair, FPGA'2004
Program Chair, FPGA'2003
Publicity Chair, FPGA'2001, FPGA'2002
Program Committee, FPGA'2000 - 2005, FPGA'2007 - 2018
Program Committee, FPL'2006 - 2007, FPL'2009 - 2018
Co-Program Chair, FPT'2011
Program Committee, FPT'2002 - 2017
Program Committee, HPEC'2012 - 2014, HPEC'2016 - 2018
Program Committee, ANCS'2012
Program Committee, ARC'2004 - 2008
Special Sessions Chair, ICCD'2011
Program Committee, SIPS'2012
Panelist for the National Science Foundation, 2002, 2005, 2009, 2010, 2014, 2016, 2017
Chair, IEEE Springfield Chapter, 2000 - 2003
Reviewer for various IEEE and ACM journals and conferences

Awards

Most Significant Paper, 20th Anniversary, IEEE International Symposium on FCCMs, 2013
Best Paper Award, IEEE Conference on Communications and Network Security, 2013
Best Paper Award, ACM Great Lakes Symposium on VLSI, 2012
Best Paper Award, ACM Workshop on Virtualized Infrastructure Systems and Architectures, 2010

Best Poster Award, IEEE International Symposium on VLSI, 2014
Keynote address, Conference on Reconfigurable Communication-Centric SoCs, 2007
Chancellor's Leadership Fellow, University of Massachusetts, 2015 - 2016
UMass Distinguished Teaching Award, nominee, 2010 - 2011
Early Tenure and Promotion, University of Massachusetts, 2004
UMass College of Engineering Outstanding Senior Faculty Award, 2017 - 2018
UMass College of Engineering Outstanding Junior Faculty Award, 2002 - 2003
UMass College of Engineering Outstanding Teaching Award, 2002 - 2003
Lilly Teaching Fellow, 2002 - 2003
IEEE Student Chapter Outstanding Faculty Award, 2001

Funded Proposals

Security for Multi-Tenant FPGAs (PI, co-PI D. Holcomb)
Funding source: Intel Corporation 11/1/17-10/31/18
Total amount: $90,000, My share: $50,000

SecureDust – The Physical Limits of Information Security (co-PI, PI D. Holcomb)
Funding source: National Science Foundation / Semiconductor Research Corporation 9/1/16-8/31/19
Total amount: $462,212, My share: $150,000

Hardware Security for Embedded Computing Systems (co-PI, PI T. Wolf)
Funding source: National Science Foundation 8/1/16-7/31/19
Total amount: $512,523, My share: $230,000

Network Function Virtualization Using Dynamic Reconfiguration (PI, co-PI L. Gao)
Funding source: National Science Foundation 10/1/15-9/30/18
Total amount: $499,000, My share: $245,000

New Architectures for Coarse-Grained Reconfigurable Arrays (sole-PI)
Funding source: Xilinx Corporation 9/1/15-12/31/16
Total amount: $40,000, My share: $40,000

New Directions in FPGA Security (PI, co-PI C. Paar)
Funding source: National Science Foundation 10/1/13-9/30/17
Total amount: $432,000, My share: $215,000

Evaluation of Portable Road Weather Information Systems (PI, co-PI S. Gao, D. Hardy)
Funding source: Massachusetts Department of Transportation 10/1/12-6/30/16
Total amount: $395,000, My share: $275,000

Mass Casualty Management System (DIORAMA-II) (co-PI, PI A. Ganz)
Funding source: National Institutes of Health 9/30/12-8/31/16
Total amount: $1,600,000, My share: $200,000

Migration of the DE5 to the NetFPGA and Linux (sole-PI)
Funding source: Altera Corporation 9/1/12-12/31/15
Total amount: $65,000, My share: $65,000

Eliminating the Energy Efficiency Barrier of Reconfigurable Architectures for Diverse Signal Processing (PI, co-PI S. Kundu)
Funding source: National Science Foundation 6/1/12-5/31/16
Total amount: $264,953, My share: $132,500

Securing the Router Infrastructure of the Internet (co-PI, PI T. Wolf)
Funding source: National Science Foundation 9/1/11-8/31/15
Total amount: $500,000, My share: $250,000

Migration of the DE4 to the NetFPGA (sole-PI)
Funding source: Altera Corporation 9/1/10-12/31/12
Total amount: $45,000, My share: $45,000

On-Chip Sensing Strategies for Efficient Scalability in Many-Core Architectures (PI, co-PI W. Burleson)
Funding source: Semiconductor Research Corporation 8/1/10-7/31/13
Total amount: $300,000, My share: $150,000

Automated Counting of Pedestrians and Bicyclists on an Urban Roadside (PI, co-PI D. Ni)
Funding source: Massachusetts Department of Transportation 10/1/09-6/30/12
Total amount: $228,000, My share: $114,000.

Vehicle Infrastructure Integration (VII): Exploring the Application of Disruptive Technology to Assist Older Drivers (co-PI, PI: D. Ni, co-PI: H. Pishro-Nik)
Funding source: New England University Transportation Consortium 9/1/09-12/31/10
Total amount: $100,000, My share: $33,000

Reconfigurable, Next-Generation Network Monitoring (PI, co-PI: T. Wolf)
Funding source: Altera Corporation 9/1/09-12/31/11
Total amount: $25,000, My share: $12,500

Low-Power High Bandwidth Receiver for Ka-Band Interferometry (co-PI, PI: P. Siqueira)
Funding source: NASA 3/1/09-2/28/12
Total amount: $1,088,000, My share: $200,000

Network Virtualization Using Dynamic FPGA Reconfiguration (PI, co-PI: L. Gao)
Funding source: National Science Foundation 9/1/08-8/31/12
Total amount: $350,000, My share: $175,000

CRI: CAD Tool and Compiler Repository for Reconfigurable Computing (sole-PI)
Funding source: National Science Foundation 8/1/07-7/31/11
Total amount: $157,500, My share: $157,500

MNOC: A Network-on-Chip for Configurable Monitors (co-PI, PI: W. Burleson)
Funding source: Semiconductor Research Corporation 4/1/07-1/31/10
Total amount: $300,000, My share: $150,000

X-Band IC Technologies for Low Cost Radars (co-PI, PI: R. Jackson)
Funding source: Raytheon Corporation 4/1/07-1/31/09
Total amount: $400,000, My share: $133,000

FPGA-Based Image Processing Research (co-PI, PI: P. Kelly)
Funding source: Kollmorgen Corporation 1/1/07-1/01/08
Total amount: $77,000, My share: $38,000

Scalable Parallel Processing Using Soft Multiprocessors (sole-PI)
Funding source: Altera Corporation 8/1/06-12/31/07
Total amount: $25,000, My share: $25,000

Power Consumption Comparison for FPGAs and Microprocessors (sole-PI)
Funding source: ST Microelectronics 8/1/04-12/31/06
Total amount: $13,000, My share: $13,000

Power-Aware Logic Synthesis and Tech. Mapping for LUT-based FPGAs (sole-PI)
Funding source: Altera Corporation 1/1/04-12/31/05
Total amount: $35,000, My share: $35,000

CASA Engineering Research Center (Investigator, PI: D. McLaughlin)
Funding source: National Science Foundation 10/1/03-12/31/06
Total amount: $16,000,000, My share: $200,000

Reconfigurable Implementation of Software Radios (sole-PI)
Funding source: M/A-COM Corporation 1/1/03-12/31/03
Total amount: $36,000, My share: $36,000

Architectures and Technology Mapping Issues for Hybrid FPGAs (sole-PI)
Funding Source: Xilinx Corporation 6/01/01-8/31/02
Total amount: $13,200, My share: $13,200

Integration of JBits and VPR (sole-PI)
Funding Source: Xilinx Corporation 6/01/01-8/31/02
Total amount: $10,000, My share: $10,000

ITR/ACS: Adaptive Fault Recovery for Networked Digital Systems (sole-PI)
Funding Source: National Science Foundation 9/01/00-8/31/03
Total amount: $185,000, My share: $185,000

Low-power Adaptive Systems on a Chip (co-PI, PI: W. Burleson)
Funding source: National Science Foundation 7/1/00-6/31/03
Total amount: $300,588, My share: $150,296

Acquisition of Sensing Data on a Reconfigurable Platform (PI, co-PI: D. McLaughlin)
Funding source: Air Force Research Laboratory 12/1/00-6/31/02
Total amount: $69,936, My share: $69,936

Reconfigurable, Time-aware Smartcard Technology (co-PI, PI: S. Desu)
Funding source: Sharp Corporation 12/1/00-11/31/02
Total amount: $200,000, My share: $100,000

Integration of SystemC with a VirtuaLogic Emulation System (sole-PI)
Funding source: Ikos Systems, Inc. 6/1/00-5/31/01
Total amount: $11,771, My share: $11,771

Reconfigurable Computing with Tiled Architectures (sole-PI)
Funding source: UMass Healey Endowment Grant 5/1/99-5/31/00
Total amount: $9,000, My share: $9,000

Ph.D Degree Thesis Advisees

1. Shiting (Justin) Lu, "On Thermal Sensor Calibration and Software Techniques For Many-Core Thermal Management, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, September 2015. (Position: Google)
2. Kekai Hu, "Securing Network Processors with Hardware Monitors", Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, September 2015. (Position: Intel)
3. Deepak Unnikrishnan, "Reconfigurable Technologies for Next Generation Internet and Cluster Computing", Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, September 2013. (Position: Altera)
4. Jia Zhao, "On-Chip Monitoring Infrastructures and Strategies for Multi-Core and Many-Core Systems", Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, May 2012. (Position: Qualcomm)
5. Weifeng Xu, "Software Based Permanent Fault Recovery Techniques Using Inherent Hardware Redundancy", Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, September 2007. (Position: Qualcomm)
6. Murali Kudlugi, "Static Scheduling of Multi Domain Circuits for Functional Verification", Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, May 2005. (Position: Mentor Graphics)
7. Jian Liang, "Development and Verification of a System-on-a-Chip Communication Architecture", Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, May 2004. (Position: Qualcomm)
8. Srini Krishnamoorthy, "Design Mapping Algorithms for Hybrid FPGAs Containing LUTs and PLAs", Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, February 2004. (Position: Advanced Micro Devices)

Masters Degree Thesis Advisees

1. Naveen Kumar Dumpala, "Energy-Efficient Loop Unrolling for Low-Cost FPGAs", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, September 2017. (Position: Intel)
2. Shrikant Vyas, "Variation Aware Placement for Efficient Key Generation using Physically Unclonable Functions in Reconfigurable Systems", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, September 2016. (Position: Altera)

3. Sandesh Virupaksha, "Accelerated Iterative Algorithms with Asynchronous Accumulative Updates on a Hetergeneous Cluster", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, February 2016. (Position: Oracle)

4. Meha Kainth, "Development of Prototypes of a Portable Road Weather Information System", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, September 2015. (Position: Altera)

5. Tedy Thomas, "Hardware Monitors for Secure Processing in Embedded Operating Systems", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, September 2015. (Position: Cavium)

6. Xiaobin Liu, "Energy Efficiency Exploration of Coarse-Grain Reconfigurable Architecture with Emerging Non-Volatile Memory", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, February 2015. (Position: Arecont Vision)

7. Cory Gorman, "Design of an Open-Source SATA Core for Virtex-4 FPGAs", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, September 2013. (Position: IBM)

8. Harikrishnan Chandrikakutty, "Protecting Network Processors with High Performance Logic Based Monitors", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, May 2013. (Position: Juniper Networks)

9. Murtaza Merchant, "Testing and Validation of a Prototype GPGPU Design for FPGAs", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, February 2013. (Position: Marvell Electronics)

10. Gayatri Prabhu, "Automated Detection and Counting of Pedestrians on an Urban Roadside", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, February 2012. (Position: Xilinx Corporation)

11. Akilesh Krishnamurthy, "Design of an FPGA-based Array Formatter for CASA Phase-Tilt Radar System", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, February 2012. (Position: Marvell Electronics)

12. Vishwas Vijayendra, "Design and Testing of a Prototype High Speed Data Acquisition System for NASA", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, August 2011. (Position: Altera Corporation)

13. Benjamin Bovée, "Simulating a Universal Geocast Scheme for Vehicular Ad Hoc Networks", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, May 2011. (Position: BTP Systems)

14. Emmanuel Seguin, "Low Cost FPGA Based Digital Beamforming Architecture for CASA Weather Radar Applications", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, May 2010. (Position: MIT Lincoln Labs)

15. Salma Mirza, "Scalable, Memory-Intensive Scientific Computing on Field Programmable Gate Arrays", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, February 2010. (Position: Netronome)

16. Ramakrishna Vadlamani, "Approaches to Multiprocessor Error Recovery Using an On-Chip Interconnect Subsystem", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, February 2010, (Position: Qualcomm)

17. Deepak Unnikrishnan, "Application-Specific Customization and Scalability of Soft Multiprocessors", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, May 2009. (UMass Ph.D student)

18. Sailaja Madduri, "MNoC: A Network-on-Chip for Monitors", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, September 2008, (Position: Intel)

19. Kevin Andryc, "A Novel Approach to PCI Simulation Using ScriptSim", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, May 2008. (UMass Ph.D student)

20. Jonathan Allen, "Energy Efficient Adaptive Reed-Solomon Decoding System", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, February 2008. (Position: EMC)

21. David Howland, "RTL Dynamic Power Optimization for FPGAs", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, May 2007, (Position: Pratt and Whitney)

22. Kevin Oo Tinmaung, "Power-aware FPGA Logic Synthesis Using Binary Decision Diagrams", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, May 2006, (Position: Guardian Life)

23. Rishi Khasgiwale, "Reconfigurable Data Acquisition System for Weather Radar Applications", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, February 2005. (Position: Mentor Graphics)

24. Lilian Atieno, "Run-Time Dynamically Reconfigurable Reed-Solomon Decoder System", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, February 2005. (Position: Marvell Electronics)

25. Eric Keller, "Programming Model for Network Processing on FPGAs", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, February 2005. (Ph.D, Princeton, Assistant Professor, University of Colorado, Boulder)

26. David Jasinski, "An Energy-Aware Active Smart-Card Architecture", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, September 2003. (Position: Naval Underwater Warfare Center)

27. Ramshankar Ramanarayanan, "Self-Test and Reconfiguration to Support Fault Tolerance in VLIW Processors", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, September 2003. (Position: Advanced Micro Devices)

28. Arun Ramanathan, "Acquisition of Sensing Data on a Reconfigurable Platform", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, February 2003. (Position: Broadcom)

29. Vibhor Garg, "A PCI-X Bus Transactor Model for SOC Verification Using Co-Modeling", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, February 2002. (Position: Cadence Design Systems)

30. Sriram Swaminathan, "An FPGA Based Adaptive Viterbi Decoder", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, September 2001. (Position: Cilantro Technologies)

31. Ramaswamy Ramaswamy, "Integration of SystemC with an Ikos VirtuaLogic Emulator", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, September 2001. (Ph.D, UMass, Position: Cisco Systems)

32. Navin Vemuri, "BDD-based Logic Synthesis for LUT-Based FPGAs", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, May 2001. (Position: Intel)

Book Chapters

B1. Russell Tessier, Tilman Wolf, Kekai Hu[1], and Harikrishnan Chandrikakutty, "Reconfigurable Network Router Security", in Reconfigurable Logic: Architecture, Tools and Applications, Pierre Gaillardon, ed., CRC Press, 2015.

B2. Russell Tessier, "Multi-FPGA Systems: Logic Emulation", in Reconfigurable Computing, Scott Hauck and André DeHon, eds., Morgan Kaufmann, pp. 637-670, 2008.

[1]The names of Prof. Tessier's students are underlined

B3. Russell Tessier and Wayne Burleson, "Reconfigurable Computing and Digital Signal Processing: Past, Present, and Future", in Programmable Digital Signal Processors, Yu Wen Hu, ed., Marcel Dekker, pp. 147-186, 2002.

Journal Publications

J1. Marc Fyrbiak, Sebastian Wallat, Pawel Swierczynski, Max Hoffmann, Sebastian Hoppach, Matthias Wilhelm, Tobias Weidlich, Russell Tessier, and Christof Paar, "HAL - The Missing Piece of the Puzzle for Hardware Reverse Engineering, Trojan Detection and Insertion", *IEEE Transactions on Dependable and Secure Computing*, accepted/to appear.

J2. Marc Fyrbiak, Simon Rokicki, Nicolai Bissantz, Russell Tessier, and Christof Paar, "Hybrid Obfuscation to Protect against Disclosure Attacks on Embedded Microprocessors", *IEEE Transactions on Computers*, vol. 67, no. 3, pages 307-321, March 2018.

J3. Vincent Migliore, Cédric Seguin, Maria Méndez Real, Vianney LaPotre, Arnaud Tisserand, Caroline Fontaine, Guy Gogniat, and Russell Tessier, "Hybrid Obfuscation to Protect against Disclosure Attacks on Embedded Microprocessors", *ACM Transactions on Embedded Computer Systems*, vol. 16, no. 5, pages 138:1-138:17, October 2017.

J4. Kekai Hu, Harikrishnan Chandrikakutty, Zachary Goodman[2], Russell Tessier, and Tilman Wolf, "Dynamic Hardware Monitors for Network Processor Protection", *IEEE Transactions on Computers*, vol. 65, no. 3, pages 860-872, March 2016

J5. Tilman Wolf, Harikrishnan Chandrikakutty, Kekai Hu, Deepak Unnikrishnan, and Russell Tessier, "Securing Network Processors with High-Performance Hardware Monitors", *IEEE Transactions on Dependable and Secure Computing*, vol. 12, no. 6, pages 652-664, December 2015.

J6. Russell Tessier, Kenneth Pocek, and André DeHon, "Reconfigurable Computing Architectures", *Proceedings of the IEEE*, vol. 103, no. 3, pages 332-354, March 2015.

J7. Shiting (Justin) Lu, Russell Tessier, and Wayne Burleson, "Dynamic On-Chip Thermal Sensor Calibration Using Performance Counters", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 33, no. 6, pages 853-866, June 2014.

J8. Deepak Unnikrishnan, Ramakrishna Vadlamani, Yong Liao, Jérémie Crenne, Lixin Gao and Russell Tessier, "Reconfigurable Data Planes for Scalable Network Virtualization", *IEEE Transactions on Computers*, vol. 62, no. 12, pages 2476-2488, December 2013.

J9. Shiting (Justin) Lu, Paul Siqueira, Vishwas Vijayendra, Harikrishnan Chandrikakutty, and Russell Tessier, "Real-Time Differential Signal Phase Estimation for Space-based Systems Using FPGAs", in *IEEE Transactions on Aerospace and Electronic Systems*, vol. 49, no. 2, pages 1192-1209, April 2013.

J10. Jérémie Crenne, Romain Vaslin, Guy Gogniat, Jean-Philippe Diguet, Russell Tessier, and Deepak Unnikrishnan, "Configurable Memory Security in Embedded Systems", in *ACM Transactions on Embedded Computer Systems*, vol. 12, no. 3, pages 1-25, March 2013.

J11. Jia Zhao, Sailaja Madduri, Ramakrishna Vadlamani, Wayne Burleson, and Russell Tessier, "A Dedicated Monitoring Infrastructure For Multicore Processors", in *IEEE Transactions on VLSI Systems*, vol. 19, no. 6, pp. 1011-1022, June 2011.

J12. Tilman Wolf, Russell Tessier, and Gayatri Prabhu, "Securing the Data Path of Next-Generation Router Systems, in Computer Communications", in *Computer Communications*, vol. 31, no. 4, pp. 598-606, April 2011.

J13. Dong Yin, Deepak Unnikrishnan, Yong Liao, Lixin Gao, and Russell Tessier, "Customizing Virtual Networks with Partial FPGA Reconfiguration", in *ACM Computer Communication Review*, vol. 41, no. 1, pp. 125-132, January 2011.

J14. Weifeng Xu and Russell Tessier, "Tetris-XL: A Performance-Driven Spill Technique for Embedded VLIW Processors", in *ACM Transactions on Architecture and Code Optimization*, vol. 6, no. 3, pp. 1-40, September 2009.

[2]Undergraduate researcher

J15. Romain Vaslin, Guy Gogniat, Jean-Philippe Diguet, Edward Wanderley, Russell Tessier and Wayne Burleson, "A Security Approach for Off-Chip Memory in Embedded Microprocessor Systems", in *Journal of Microprocessors and Microsystems*, vol. 33, no. 1, pp. 37-45, February 2009.

J16. Ian Kuon, Russell Tessier, and Jonathan Rose, "FPGA Architecture: Survey and Challenges", in *Foundations and Trends in Electronic Design Automation*, vol. 2, no. 2, pp. 135-253, February 2008.

J17. Russell Tessier, Vaughn Betz, David Neto, Aaron Egier, and Thiagaraja Gopalsamy, "Power Efficient RAM Mapping Algorithms for FPGA Embedded Memory Blocks", in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 26, no. 2, pp. 278-290, February 2007.

J18. Prem Menon, Weifeng Xu, and Russell Tessier, "Design-Specific Path Delay Testing in Lookup Table-based FPGAs", in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 25, no. 5, pp. 867-877, May 2006.

J19. Russell Tessier, David Jasinski, Atul Maheshwari, Aiyappan Natarajan, Weifeng Xu, and Wayne Burleson, "An Energy-Aware Active Smart Card", in *IEEE Transactions on VLSI Systems*, vol. 13, no. 10, pages 1190-1199, October 2005.

J20. Russell Tessier, Sriram Swaminathan, Ramaswamy Ramaswamy, Dennis Goeckel, and Wayne Burleson, "A Reconfigurable, Power-Efficient Adaptive Viterbi Decoder", in *IEEE Transactions on VLSI Systems*, vol. 13, no. 4, pages 484-488, April 2005.

J21. Jian Liang, Andrew Laffely, Sriram Srinivasan, and Russell Tessier, "An Architecture and Compiler for On-Chip Communication", in *IEEE Transactions on VLSI Systems*, vol. 12, no. 7, pages 711-726, July 2004.

J22. Gordon Farquharson, William Junek, Arun Ramanathan, Steven Frasier, Russell Tessier, David McLaughlin, and Mark Sletten, "A Pod-Based Dual-Beam InSAR", in *IEEE Transactions on Geoscience and Remote Sensing*, vol 1, no. 2, pages 62-65, April 2004.

J23. Atul Maheshwari, Wayne Burleson, and Russell Tessier, "Trading Off Transient Fault Tolerance and Power Consumption in Deep Submicron VLSI Circuits", in *IEEE Transactions on VLSI Systems*, vol 12, no. 1, pages 299-311, March 2004.

J24. Prashant Jain, Andrew Laffely, Wayne Burleson, Russell Tessier, and Dennis Goeckel, "Dynamically Parameterized Algorithms and Architectures to Exploit Signal Variations", in *Journal of VLSI Signal Processing*, vol 36, no. 1, pages 27-40, Kluwer Publishers, January 2004.

J25. Srini Krishnamoorthy and Russell Tessier, "Technology Mapping Algorithms for Hybrid FPGAs Containing Look-up Tables and PLAs", in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol 22, no. 5, pp. 545-559, May 2003.

J26. Ian Harris and Russell Tessier, "Testing and Diagnosis of Interconnect Faults in Cluster-Based FPGA Architectures", in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*. vol 21, no. 11, pp. 1137-1143, November 2002.

J27. Murali Kudlugi and Russell Tessier, "Static Scheduling of Multiple Asynchronous Domains for Fast Functional Verification", in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol 21, no. 11, pp. 1253-1268, November 2002.

J28. Russell Tessier and Snigdha Jana, "Incremental Compilation for Parallel Logic Verification Systems", *IEEE Transactions on VLSI Systems*, vol 10, no. 5, pp. 623-636, October 2002.

J29. Navin Vemuri, Priyank Kalla, and Russell Tessier, "BDD-based Logic Synthesis for FPGAs", in *ACM Transactions on Design Automation of Electronic Systems*, vol. 7, no. 4, pp. 501-525, October 2002.

J30. Russell Tessier, "Fast Placement Approaches for FPGAs", in *ACM Transactions on Design Automation of Electronic Systems*, vol 7, no. 2, pp. 284-305, April 2002.

J31. Russell Tessier and Wayne Burleson, "Reconfigurable Computing and Digital Signal Processing: A Survey," in *Journal of VLSI Signal Processing*, pp. 7-27, May/June 2001.

J32. Jonathan Babb, Russell Tessier, Matthew Dahl, Silvina Hanono, David Hoki, and Anant Agarwal, "Logic Emulation with Virtual Wires," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol 16., no. 6, pp. 609-626, June 1997.

Conference Publications - $< 40\%$ accept rate

C1. George Provelengios, Arman Pouraghily, Russell Tessier and Tilman Wolf, "A Hardware Monitor to Protect Linux System Calls", in *Proceedings: IEEE International Symposium on VLSI*, Hong Kong, China, July 2018. (accept rate: 30%)

C2. Chethan Ramesh, Shivukumar B. Patil, George Provelengios, Siva Nishok Dhanuskodi, Daniel Holcomb, and Russell Tessier, "FPGA Side Channel Attacks without Physical Access", in *Proceedings: IEEE International Symposium on Field-Programmable Custom Computing Machines*, Boulder, CO, May 2018. (accept rate: 21%)

C3. Shivukumar B. Patil, Tianqi Liu, and Russell Tessier, "A Bandwidth-Optimized Routing Algorithm for Hybrid FPGA Networks-on-Chip", in *Proceedings: IEEE International Symposium on Field-Programmable Custom Computing Machines*, Boulder, CO, May 2018. (accept rate: 15%)

C4. Xuzhi Zhang, Xiaozhe Shao, George Provelengios, Naveen Kumar Dumpala, Lixin Gao, and Russell Tessier, "Scalable Network Function Virtualization for Heterogeneous Middleboxes", in *Proceedings: IEEE International Symposium on Field-Programmable Custom Computing Machines*, Napa, CA, pp. 219-226, May 2017. (accept rate: 24%)

C5. Naveen Kumar Dumpala, Shivukumar B. Patil, and Russell Tessier, "Energy Efficient Loop Unrolling for Low-Cost FPGAs", in *Proceedings: IEEE International Symposium on Field-Programmable Custom Computing Machines*, Napa, CA, pp. 117-120, May 2017. (accept rate: 23%)

C6. Tianqi Liu, Naveen Kumar Dumpala, and Russell Tessier, "Hybrid Hard NoCs for Efficient FPGA Communication", in *Proceedings: International Conference on Field-Programmable Technology*, Xi'an, China, pp. 157-164, December 2016. (accept rate: 23%)

C7. Christophe Huriaux, Olivier Sentieys, and Russell Tessier, "Effects of I/O Routing through Column Interfaces in Embedded FPGA Fabrics", in *Proceedings: International Conference on Field-Programmable Logic and Applications*, Lausanne, Switzerland, pp. 1-9, September 2016. (accept rate: 21%)

C8. Tedy Thomas, Arman Pouraghily, Kekai Hu, Russell Tessier, and Tilman Wolf, "Multi-Task Support for Security-Enabled Embedded Processors", in *Proceedings: IEEE International Conference on Application-specific Systems, Architectures and Processors*, Toronto, ON, pp. 136-143, July 2015. (accept rate: 25%)

C9. Shiting (Justin) Lu, Russell Tessier, and Wayne Burleson, "Reinforcement Learning For Thermal-Aware Many-Core Task Allocation", in *Proceedings: ACM Great Lakes Symposium on VLSI*, Pittsburgh, PA, pp. 379-384, May 2015. (accept rate: 28%)

C10. Pawel Swierczynski, Marc Fyrbiak, Christof Paar, Christophe Huriaux, and Russell Tessier, "Protecting against Cryptographic Trojans in FPGAs", in *Proceedings: IEEE International Symposium on Field-Programmable Custom Computing Machines*, Vancouver, British Columbia, Canada, pp. 151-154, May 2015. (accept rate: 39%)

C11. Meha Kainth, Lekshmi Krishnan, Chaitra Narayana, Sandesh Virupaksha, and Russell Tessier, "Hardware-Assisted Code Obfuscation for FPGA Soft Microprocessors", in *Proceedings: IEEE/ACM Design Automation and Test in Europe Conference*, Grenoble, France, pp. 127-132, March 2015. (accept rate: 22%)

C12. Christophe Huriaux, Olivier Sentieys and Russell Tessier, "FPGA Architecture Support for Heterogeneous, Relocatable Partial Bitstreams", in *Proceedings: International Conference on Field-Programmable Logic and Applications*, Munich, Germany, pp. 1-6, September 2014. (accept rate: 22%)

C13. Kekai Hu, Tilman Wolf, Thiago Teixeira, and Russell Tessier, "System-Level Security for Network Processors with Hardware Monitors", in *Proceedings: IEEE/ACM Design Automation Conference*, San Francisco, CA, pp. 1-6, June 2014. (accept rate: 22%)

C14. Kevin Andryc, Murtaza Merchant, and Russell Tessier, "FlexGrip: A Soft GPGPU for FPGAs", in *Proceedings: International Conference on Field-Programmable Technology*, Kyoto, Japan, pp. 230-237, December 2013. (accept rate: 21%)

C15. Deepak Unnikrishnan, Sandesh Gubbi Virupaksha, Lekshmi Krishnan, Lixin Gao and Russell Tessier, "Accelerating Iterative Algorithms with Asynchronous Accumulative Updates on FPGAs", in *Proceedings: International Conference on Field-Programmable Technology*, Kyoto, Japan, pp. 66-73, December 2013. (accept rate: 21%)

C16. Kekai Hu, Harikrishnan Chandrikakutty, Russell Tessier, and Tilman Wolf, "Scalable Hardware Monitors to Protect Network Processors from Data Plane Attacks", in *Proceedings: IEEE International Conference on Communications and Network Security*, Washington, DC, pp. 314-322, October 2013. (accept rate: 28%), **Best Paper Award**

C17. Harikrishnan Chandrikakutty, Deepak Unnikrishnan, Russell Tessier, and Tilman Wolf, "High-Performance Hardware Monitors to Protect Network Processors from Data Plane Attacks", in *Proceedings: IEEE/ACM Design Automation Conference*, Austin, TX, pp. 1-6, June 2013. (accept rate: 24%)

C18. Daniel Gomez-Prado, Maciej Ciesielski, and Russell Tessier, "FPGA Latency Optimization Using System-level Transformations and DFG Restructuring", in *Proceedings: IEEE/ACM Design Automation and Test in Europe Conference*, Grenoble, France, pp. 1553-1558, March 2013. (accept rate: 25%)

C19. Jia Zhao, Shiting (Justin) Lu, Wayne Burleson, and Russell Tessier, "Run-time Probabilistic Detection of Miscalibrated Thermal Sensors in Many-core Systems", in *Proceedings: IEEE/ACM Design Automation and Test in Europe Conference*, Grenoble, France, pp. 1395-1398, March 2013. (accept rate: 36%)

C20. Shiting (Justin) Lu, Russell Tessier, and Wayne Burleson, "Collaborative Calibration of On-Chip Thermal Sensors Using Performance Counters", in *Proceedings: IEEE/ACM International Conference on Computer-Aided Design*, San Jose, CA, pp. 15-22, November 2012. (accept rate: 24%)

C21. Y. Sinan Hanay, Wei Li, Russell Tessier, and Tilman Wolf, "Saving Energy and Improving TCP Throughput with Rate Adaptation in Ethernet", in *Proceedings: IEEE Conference on Communications*, Ottawa, Ontario, pp. 1249-1254, June 2012. (accept rate: 37%)

C22. Jia Zhao, Russell Tessier, and Wayne Burleson "Distributed Sensor Data Processing for Many-cores," in *Proceedings: ACM Great Lakes Symposium on VLSI*, Salt Lake City, Utah, pp. 159-164, May 2012. (accept rate: 17%), **Best Paper Award**

C23. Deepak Unnikrishnan, Justin Lu, Lixin Gao, and Russell Tessier, "ReClick - A Modular Dataplane Design Framework for FPGA-Based Network Virtualization", in *Proceedings: ACM/IEEE Symposium on Architectures for Networking and Communications Systems*, Brooklyn, NY, pp. 145-155, October 2011. (accept rate: 32%)

C24. Dong Yin, Deepak Unnikrishnan, Yong Liao, Lixin Gao, and Russell Tessier, "Customizing Virtual Networks with Partial FPGA Reconfiguration", in *Proceedings: ACM SIGCOMM Workshop on Virtualized Infrastructure Systems and Architectures*, New Delhi, India, pp. 57-64, August 2010. (accept rate: 30%), **Best Paper Award**

C25. Jia Zhao, Basab Datta, Wayne Burleson, and Russell Tessier, "Thermal-aware Voltage Droop Compensation for Multi-core Architectures", in *Proceedings: ACM Great Lakes Symposium on VLSI*, Providence, RI, pp. 335-340, May 2010. (accept rate: 30%)

C26. Ramakrishna Vadlamani, Jia Zhao, Wayne Burleson, and Russell Tessier, "Multicore Soft Error Rate Stabilization Using Adaptive Dual Modular Redundancy", in *Proceedings: IEEE/ACM Design Automation and Test in Europe Conference*, Dresden, Germany, pp. 27-32, March 2010. (accept rate: 30%)

C27. Deepak Unnikrishnan, Ramakrishna Vadlamani, Yong Liao, Abhishek Dwaraki, Jeremie Crenne, Lixin Gao, and Russell Tessier, "Scalable Network Virtualization Using FPGAs", in *Proceedings: ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, Monterey, CA, pp. 219-228, February 2010. (accept rate: 25%)

C28. Tilman Wolf and Russell Tessier, "Design of a Secure Router System for Next-Generation Networks", in *Proceedings: IEEE International Conference on Network and System Security*, Gold Coast, Australia, pp. 52-59, October 2009. (accept rate: 26%)

C29. Kevin Andryc, Russell Tessier, and Patrick Kelly, "An Interactive Approach to Timing-Accurate PCI-X Simulation", in *Proceedings: IEEE/IFIP International Symposium on Rapid Systems Prototyping*, Paris, France, pp. 181-187, June 2009. (accept rate: 35%)

C30. Sailaja Madduri, Ramakrishna Vadlamani, Wayne Burleson and Russell Tessier "A Monitor Interconnect and Support Subsystem for Multicore Processors", in *Proceedings: IEEE/ACM Design Automation and Test in Europe Conference*, Nice, France, pp. 761-766, April 2009. (accept rate: 23%)

C31. Deepak Unnikrishnan, Jia Zhao, and Russell Tessier, "Application-Specific Customization and Scalability of Soft Multiprocessors", in *Proceedings: IEEE International Symposium on Field-Programmable Custom Computing Machines*, Napa, California, pp. 123-130, April 2009. (accept rate: 30%)

C32. Romain Vaslin, Guy Gogniat, Jean-Philippe Diguet, Russell Tessier, Deepak Unnikrishnan, and Kris Gaj, "Memory Security Management for Reconfigurable Embedded Systems", in *Proceedings: International Conference on Field-Programmable Technology*, Taipai, Taiwan, pp. 153-160, December 2008. (accept rate: 23%)

C33. Weifeng Xu and Russell Tessier, "Tetris: A New Register Pressure Control Technique for VLIW Processors", in *Proceedings: ACM/SIGPLAN Conference on Languages, Compilers, and Tools for Embedded Systems*, San Diego, CA, pp. 113-122, June 2007. (accept rate: 28%)

C34. Kevin Oo Tinmaung, David Howland, and Russell Tessier, "Power-aware FPGA Logic Synthesis Using Binary Decision Diagrams", *Proceedings: ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, Monterey, CA, pp. 148-155, February 2007. (accept rate: 24%)

C35. Russell Tessier, Vaughn Betz, David Neto, and Thiagaraja Gopalsamy, "Power-aware RAM Mapping for FPGA Embedded Memory Blocks", in *Proceedings: ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, Monterey, California, pp. 189-198, February 2006. (accept rate: 22%)

C36. Lilian Atieno, Jonathan Allen, Dennis Goeckel, and Russell Tessier "An Adaptive Reed-Solomon Errors-and-Erasures Decoder", in *Proceedings: ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, Monterey, California, pp. 150-158, February 2006. (accept rate: 22%)

C37. Jian Liang, Russell Tessier, and Dennis Goeckel, "A Dynamically-Reconfigurable, Power-Efficient Turbo Decoder", in *Proceedings: IEEE International Symposium on Field-Programmable Custom Computing Machines*, Napa, CA, pp. 91-100, April 2004. (accept rate: 27%)

C38. Weifeng Xu, Ramshankar Ramanarayanan, and Russell Tessier, "Adaptive Fault Tolerance for Networked Reconfigurable Systems", in *Proceedings: IEEE International Symposium on Field-Programmable Custom Computing Machines*, Napa, CA, pp. 143-152, April 2003. (accept rate: 39%)

C39. Jian Liang, Russell Tessier, and Oskar Mencer, "Floating Point Unit Generation and Evaluation for FPGAs", in *Proceedings: IEEE International Symposium on Field-Programmable Custom Computing Machines*, Napa, CA, pp. 185-194, April 2003. (accept rate: 39%)

C40. Aiyappan Natarajan, David Jasinski, Wayne Burleson, and Russell Tessier, "A Hybrid Adiabatic Content Addressable Memory for Ultra-Low Power Applications", in *Proceedings: IEEE/ACM Great Lakes Symposium on VLSI*, Washington, D.C., pp. 72-75, April 2003. (accept rate: 26%)

C41. Sriram Swaminathan, Russell Tessier, Dennis Goeckel, and Wayne Burleson, "A Dynamically Reconfigurable Adaptive Viterbi Decoder", in *Proceedings: ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, Monterey, California, pp. 227-236, February 2002. (accept rate: 35%)

C42. Murali Kudlugi, Charles Selvidge, and Russell Tessier, "Static Scheduling of Multi-Domain Memories for Functional Verification", in *Proceedings: International Conference on Computer Aided Design*, pp. 2-9, San Jose, California, November 2001. (accept rate: 29%)

C43. Ian Harris, Prem Menon, and Russell Tessier, "BIST-Based Delay Path Testing in FPGA Architectures", in *Proceedings: International Test Conference*, Baltimore, Maryland, pp. 364-369, October 2001. (accept rate: 39%)

C44. Murali Kudlugi, Charles Selvidge, and Russell Tessier, "Static Scheduling of Multiple Asynchronous Domains for Functional Verification", in *Proceedings: 38th Design Automation Conference*, Las Vegas, Nevada, pp. 647-652, June 2001. (accept rate: 32%)

C45. Mandeep Singh, Santhosh Thampuran, Prashant Jain, Russell Tessier and Csaba Andras Moritz, "Short Range Wireless Connectivity for Next Generation Architectures" in *Proceedings: International Conference on Parallel and Distributed Processing Techniques and Applications*, Las Vegas, Nevada, June 2001. (accept rate: 26%)

C46. Ian Harris and Russell Tessier, "Diagnosis of Interconnect Faults in Cluster-Based FPGA Architectures," in *Proceedings: International Conference on Computer Aided Design*, San Jose, California, pp. 49-54, November 2000. (accept rate: 30%)

C47. Jian Liang, Sriram Swaminathan, and Russell Tessier, "aSOC: A Scalable, Single-Chip Communications Architecture," in *Proceedings: IEEE International Conference on Parallel Architectures and Compilation Techniques*, Philadelphia, Pennsylvania, pp. 37-46, October 2000. (accept rate: 26%)

C48. Ian Harris and Russell Tessier, "Interconnect Testing in Cluster-Based FPGA Architectures," in *Proceedings: 37th Design Automation Conference*, Los Angeles, California, pp. 472-476, June 2000. (accept rate: 30%)

C49. Vijay Lakamraju and Russell Tessier, "Tolerating Operational Faults in Cluster-based FPGAs," in *Proceedings: ACM/SIGDA International Symposium on Field-Programmable Gate Arrays*, Monterey, California, pp. 187-194, February 2000. (accept rate: 35%)

C50. Matthew Dahl, Jonathan Babb, Russell Tessier, Silvina Hanono, David Hoki, and Anant Agarwal, "Emulation of a SPARC Microprocessor with the MIT Virtual Wires Emulation System," in *Proceedings: IEEE Workshop on FPGAs for Custom Computing Machines,* Napa, California, pp. 14-22, April 1994.

C51. Russell Tessier, Jonathan Babb, Matthew Dahl, Silvina Hanono, and Anant Agarwal, "The Virtual Wires Emulation System: A Gate-Efficient ASIC Prototyping Environment," in *Proceedings: 2nd ACM/SIGDA International Workshop on Field Programmable Gate Arrays,* Berkeley, California, February 1994.

C52. Jonathan Babb, Russell Tessier, and Anant Agarwal, "Virtual Wires: Overcoming Pin Limitations in FPGA-based Logic Emulators," in *Proceedings: IEEE Workshop on FPGAs for Custom Computing Machines,* Napa, California, pp. 142-151, April 1993.

Conference Publications - $\geq$ 40% accept rate

C53. Arman Pouraghily, Tilman Wolf, and Russell Tessier, "Hardware Support for Embedded Operating System Security", in *Proceedings: IEEE International Conference on Application-specific Systems, Architectures and Processors*, Seattle, WA, pp. 61-66, July 2017. (accept rate: 51%)

C54. Shrikant Vyas, Naveen Kumar Dumpala, Russell Tessier, and Daniel Holcomb, "Improving the Efficiency of PUF-Based Key Generation in FPGAs Using Variation-Aware Placement", in *Proceedings: 26th International Conference on Field Programmable Logic and Applications*, Lausanne, Switzerland, pp. 1-4, September 2016. (accept rate: 42%)

C55. Kevin Andryc, Tedy Thomas, and Russell Tessier, "Soft GPGPUs for Embedded FPGAs: An Architectural Evaluation", in *Proceedings: Second Workshop on Overlay Architectures for FPGAs*, Monterey, CA, pp. 1-6, February 2016.

C56. Xiaobin Liu, Tedy Thomas, Alan Boguslawski[3], and Russell Tessier, "Adaptive MRAM-Based CGRAs", in *Proceedings: 25th International Conference on Field Programmable Logic and Applications*, London, England, pages 1-4, September 2015. (accept rate: 41%)

C57. Jia Zhao, Shiting (Justin) Lu, Wayne Burleson, and Russell Tessier, "A Broadcast-Enabled Sensing System for Embedded Multi-core Processors", in *Proceedings: IEEE International Symposium on VLSI*, Tampa, FL, pp. 190-195, July 2014. (accept rate: 46%)

[3]Undergraduate researcher

C58. Cory Gorman, Paul Siqueira, and Russell Tessier, "An Open-Source SATA Core for Virtex-4 FPGAs", in *Proceedings: International Conference on Field-Programmable Technology*, Kyoto, Japan, pp. 454-457, December 2013.

C59. Jeŕemie Crenne, Patrice Cotret, Guy Gogniat, Russell Tessier, and Jean-Philippe Diguet, "Efficient Key-Dependent Message Authentication in Reconfigurable Hardware", in *Proceedings: International Conference on Field-Programmable Technology*, New Delhi, India, pp. 1-6, December 2011. (accept rate: 52%)

C60. Emmanuel Seguin, Russell Tessier, Eric Knapp, and Robert W. Jackson, "A Dynamically-Reconfigurable Phased Array Radar Processing System", in *Proceedings: 21st International Conference on Field Programmable Logic and Applications*, Chania, Greece, pp. 258-263, September 2011. (accept rate: 48%)

C61. Ben Bovée, Mohammad Nekoui, Hossein Pishro-Nik and Russell Tessier, "Evaluation of the Universal Geocast Scheme For VANETs" in *Proceedings: IEEE Vehicular Technology Conference*, San Francisco, CA, September 2011. (accept rate: 50%)

C62. Vishwas Vijayendra, Paul Siqueira, Harikrishnan Chandrikakutty, Akilesh Krishnamurthy, and R. Tessier, "Real-Time Estimates of Differential Signal Phase for Spaceborne Systems Using FPGAs", in *Proceedings: NASA/ESA Conference on Adaptive Hardware and Systems*, San Diego, CA, pp. 121-128, June 2011. (accept rate: 48%)

C63. David Howland and Russell Tessier, "RTL Dynamic Power Optimization for FPGAs", in *Proceedings: IEEE Midwest Symposium on Circuits and Systems*, Nashville, TN, pp. 714-717, August 2008. (accept rate: 69%)

C64. Romain Vaslin, Guy Gogniat, Jean-Philippe Diguet, Eduardo Wanderley, Russell Tessier, and Wayne Burleson, "Low Latency Solution for Confidentiality and Integrity Checking in Embedded Systems with Off-Chip Memory", in *Proceedings: International Conference on Reconfigurable Communication-centric SoCs*, Montpellier, France, pp. 146-153, June 2007.

C65. Romain Vaslin, Guy Gogniat, Jean-Philippe Diguet, Wayne Burleson, and Russell Tessier, "High-Efficiency Protection Solution for Off-Chip Memory in Embedded Systems", in *Proceedings: International Conference on Engineering of Reconfigurable Systems and Algorithms*, Las Vegas, NV, pp. 117-123, June 2007.

C66. Rishi Khasgiwale, Luko Krnan, Atchuthan Perinkulam, and Russell Tessier "Reconfigurable Data Acquisition System for Weather Radar Applications", in *Proceedings: IEEE Midwest Symposium on Circuits and Systems*, Cincinnati, OH, pp. 822-825, August 2005.

C67. Dragana Perkovic, Stephen Frasier, Russell Tessier, Mark Sletten, and Jakov Toporkov, "An Airborne Pod-based Dual Beam Interferometer" in *Proceedings: IEEE Aerospace Conference*, Big Sky, MT, pp. 1193-1201, March 2005.

C68. Andrew Laffely, Jian Liang, Wayne Burleson, and Russell Tessier, "Adaptive System on a Chip: A Backbone for Power-Aware Signal Processing Cores", in *Proceedings: IEEE Conference on Signal Processing*, Barcelona, Spain, pp. 105-108, September 2003.

C69. Ramaswamy Ramaswamy and Russell Tessier, "The Integration of SystemC and Hardware-assisted Verification", in *Proceedings: 12th International Conference on Field-Programmable Logic and Applications*, Montpelier, France, pp. 1007-1016, September 2002. (accept rate: 48%)

C70. Atul Maheshwari, Russell Tessier, and Wayne Burleson, "Trading Off Reliability and Power Consumption in Ultra-Low Power Systems", in *Proceedings: International Symposium on Quality Electronic Design*, San Jose, California, pp. 361-366, March 2002. (accept rate: 60%)

C71. Andrew Laffely, Jian Liang, Prashant Jian, Ning Weng, Wayne Burleson, and Russell Tessier, "Adaptive Systems on a Chip (aSoC) for Low-Power Signal Processing", in *Proceedings: Asilomar Conference on Signals, Systems, and Computers*, Monterey, California, pp. 1217-1222, November 2001.

C72. Murali Kudlugi and Russell Tessier, "Multi-domain Communication for FPGA-based Logic Emulation", in *Proceedings of the 10th International Workshop on Logic and Synthesis*, Lake Tahoe, Nevada, June 2001.

C73. Wayne Burleson, Russell Tessier, Dennis Goeckel, Sriram Swaminathan, and Prashant Jain, "Dynamically Parameterized Algorithms and Architectures to Exploit Signal Variations for Improved Performance and Reduced Power" in *Proceedings: International Conference on Acoustics, Speech, and Signal Processing*, vol. 2, pp. 901-904, Salt Lake City, Utah, May 2001. (accept rate: 51%)

C74. Srini Krishnamoorthy, Sriram Swaminathan, and Russell Tessier, "Area-Optimized Technology Mapping for Hybrid FPGAs," in *Proceedings: 10th International Conference on Field Programmable Logic and Applications*, Villach, Austria, pp. 181-190, August 2000.

C75. Russell Tessier and Heather Giza[4], "Balancing Logic Utilization and Area Efficiency in FPGAs," in *Proceedings: 10th International Conference on Field Programmable Logic and Applications*, Villach, Austria, pp. 535-544, August 2000.

C76. Russell Tessier, "Frontier: A Fast Placement System for FPGAs," in *Proceedings: Tenth IFIP International Conference on VLSI*, Lisbon, Portugal, pp. 125-136, December 1999.

C77. Russell Tessier, "Incremental Compilation for Logic Emulation," in *Proceedings: IEEE International Workshop on Rapid System Prototyping*, Clearwater, Florida, pp. 236-241, June 1999.

C78. Russell Tessier, "Negotiated A* Routing for FPGAs," in *Proceedings: 5th Canadian Workshop on Field-Programmable Devices*, Montreal, Quebec, pp. 14-19, June 1998.

C79. Steven Ward, Karim Abdalla, Rajeev Dujari, Michael Fetterman, Frank Honore, Ricardo Jenez, Phillipe Laffont, Ken Mackenzie, Chris Metcalf, Milan Minsky, John Nguyen, John Pezaris, Gill Pratt, and Russell Tessier. "The NuMesh: A Modular, Scalable Communications Substrate", in *Proceedings: International Conference on Supercomputing*, pp. 123-132, July 1993.

Unrefereed/ Invited Publications

C80. Kenneth Pocek, Russell Tessier, and André DeHon, "Birth and Adolescence of Reconfigurable Computing: A Survey of the First 20 Years of Field-Programmable Custom Computing Machines", in *Highlights of the First Twenty Years of the IEEE International Symposium on Field-Programmable Custom Computing Machines*, Seattle, WA, pp. 3-19, May 2013.

C81. Eric Knapp, Jorge Salazar, Rafael Medina, Akilesh Krishnamurthy and Russell Tessier, "Phase-Tilt Radar Antenna Array", in *Proceedings: European Microwave Week Conference*, Manchester, UK, 4 pages, October 2011.

C82. Krzysztof Orzel, Vijay Venkatesh, Robert Palumbo, Rafael Medina, Akilesh Krishnamurthy, Jorge Salazar, Eric Knapp, David McLaughlin, Russell Tessier and Steven Frasier, "Mobile X-Band Dual Polarization Phased Array Radar: System Requirements and Development", in *Proceedings: AMS Conference on Radar Meteorology*, Pittsburgh, PA, 4 pages, September 2011.

C83. Michael Todd, Wayne Burleson, and Russell Tessier, "The Design and Assessment of a Secure Passive RFID Sensor System", in *Proceedings: IEEE New Circuits and Systems Conference*, Bordeaux, France, pp. 494-497, June 2011.

C84. Salma Mirza, J. Blair Perot, and Russell Tessier, "Reconfigurable Sparse Matrix-Vector Multiplication on FPGAs", in *Proceedings: International Conference on Engineering of Reconfigurable Systems and Algorithms*, Las Vegas, NV, 6 pages, July 2010.

C85. Romain Vaslin, Guy Gogniat, Jean-Pierre Diguet, Edward Wanderly, Russell Tessier, and Wayne Burleson, "Low Latency Solution for Confidentiality and Integrity Checking in Embedded Systems with Off-Chip Memory", in *Proceedings: International Conference on Reconfigurable Communication-centric SoCs*, Montpelier, France, 4 pages, June 2007.

C86. Romain Vaslin, Guy Gogniat, Jean-Pierre Diguet, Wayne Burleson, and Russell Tessier, "High-Efficiency Protection Solution for Off-Chip Memory in Embedded Systems", in *Proceedings: International Conference on Engineering of Reconfigurable Systems and Algorithms*, Las Vegas, NV, 6 pages, June 2007.

C87. Francesc Junyent, et al., "Salient Features of Radar Nodes of the First Generation NetRad System", in *Proceedings: International Geoscience and Remote Sensing Symposium*, Seoul, Korea, 3 pages, July 2005.

[4]Undergraduate researcher

C88. William Junek, Arun Ramanathan, Gordon Farquharson, Steven Frasier, Russell Tessier, David McLaughlin, Mark Sletten, and Jakov Toporkov, "First Observations with the UMass Dual-Beam InSAR", in *Proceedings: International Geoscience and Remote Sensing Symposium*, Toulouse, France, 3 pages, July 2003.

C89. Ramshankar Ramanarayanan, Russell Tessier, and Ian G. Harris, "Self-Test Recompilation to Support Fault Tolerance in VLIW Processors", in *Proceedings: International Test Synthesis Workshop*, Santa Barbara, CA, 2 pages, March 2002.

C90. Arun Ramanathan, Russell Tessier, David McLaughlin, James Carswell, and Steven Frasier, "Acquisition of Sensing Data on a Reconfigurable Platform", in *Proceedings: International Geoscience and Remote Sensing Symposium*, Sydney, Australia, 2 pages, July 2001.

Invited Talks

T1. "Scalable Network Function Virtualization for Heterogeneous Middleboxes", *Yale University*, New Haven, CT, October 2017.

T2. "Scalable Network Function Virtualization for Heterogeneous Middleboxes", *Ruhr University*, Bochum, Germany, September 2017.

T3. "Hard Hybrid and Time-Division Multiplexed NoCs for FPGAs", *Xilinx Corporation*, San Jose, CA, February 2017.

T4. "Hardware-Assisted Code Obfuscation for FPGA Soft Microprocessors", *Ecole Polytechnique de Lausanne (EPFL)*, Lausanne, Switzerland, March 2015.

T5. "Network Security Using Reconfigurable Hardware Monitoring", *Winter School on Design Technologies for Heterogeneous Embedded Systems*, Ottawa, ON, January 2014.

T6. "On-chip Monitoring Infrastructures and Strategies for Many-core Systems", *Advanced Micro Devices*, Boxborough, MA, September 2013.

T7. "Scalable Network Virtualization Using FPGAs", *University of Wisconsin*, Madison, WI, November 2012.

T8. "Scalable Network Virtualization Using FPGAs", *Microsoft Research*, Redmond, WA, August 2012.

T9. "Logic Emulation", *Nanjing Forestry University*, Nanjing, China, May 2012.

T10. "Scalable Network Virtualization Using FPGAs", *University of Toronto*, Toronto, ON, June 2011.

T11. "Hardware Core for Off-chip Memory Security Management in Embedded Systems", *University of Arkansas*, Fayetteville, AR, November 2010.

T12. "Next-Generation Networking Using FPGAs", Keynote address, *Conference on the Engineering of Reconfigurable Systems and Algorithms*, Las Vegas, NV, July 2010.

T13. "Scalable Soft Multiprocessor Generation from a High-level Language", *University of Rennes*, Lannion, France, December 2009.

T14. "Scalable Soft Multiprocessor Generation from a High-level Language", *LIRMM*, Montpellier, France, July 2009.

T15. "Hardware Core for Off-chip Memory Security Management in Embedded Systems", *University of New Hampshire*, Durham, NH, March 2009.

T16. "Hardware Core for Off-chip Memory Security Management in Embedded Sytems", *Boston University*, Boston, MA, November 2008.

T17. "Reconfigurable Computing: Research and Curriculum", *University of North Carolina, Charlotte*, Charlotte, NC, May 2008.

T18. "Reconfigurable Data Acquisition System for Weather Prediction", *University of Connecticut*, Storrs, CT, February 2008.

T19. "Power-Reduction Techniques for FPGAs: Technologies and Trends", *Worcester Polytechnic Institute*, Worcester, MA, December 2007.

T20. "A Dynamically-Reconfigurable, Power-Efficient Turbo Decoder", *Xilinx Corporation*, Edinburgh, UK, July 2007.

T21. "Power-reduction Techniques for ReCoSoc: Technologies and Trends", Keynote address, *International Conference on Reconfigurable Communication-centric SoCs*, Montpellier, France, June 2007.

T22. "Reconfigurable Data Acquisition System for Weather Prediction", *Imperial College*, London, UK, June 2007.

T23. "A Power-aware BDD Decomposition Algorithm for FPGAs", *University of Toronto*, Toronto, ON, March 2005.

T24. "aSoC: A Single-Chip Communications Architecture", *Altera Corporation*, San Jose, CA, February 2004.

T25. "aSoC: A Single-Chip Communications Architecture", *University of British Columbia*, Vancouver, British Columbia, August 2003.

T26. "Will FPGAs Take Over Systems-on-a-Chip?", *Northeast Workshop on Circuits and Systems panel discussion*, Montreal, Quebec, June 2003.

T27. "aSoC: A Single-Chip Communications Architecture", *Carnegie Mellon University*, Pittsburgh, PA., March 2003.

T28. "Technology Mapping Algorithms for FPGAs with LUTs and PLAs", *Altera Corporation*, Toronto, Ontario, February 2003.

T29. "aSoC: A Single-Chip Communications Architecture", *California Institute of Technology*, Pasadena, CA., January 2003.

T30. "A Dynamically-Reconfigurable Adaptive Viterbi Decoder", *Queens University*, Belfast, No. Ireland, August 2002.

T31. "Static Scheduling of Multiple Asynchronous Clock Domains for Logic Verification" *Tufts University CAD Seminar,* Somerville, MA., November 2001.

T32. "Fast Place and Route Approaches for FPGAs." *Xilinx Corporation,* San Jose, CA, February 1999.

T33. "Fast Place and Route Approaches for FPGAs." *University of California, Berkeley CAD Seminar,* Berkeley, CA., February 1999.

T34. "Cut-based FPGA Floorplanning for Reconfigurable Computing." *University of Toronto FPGA Research Review,* Peterborough, Ontario, June 1997.

Ph.D Committee Memberships

1. Jason Anderson, University of Toronto, Canada, ECE.
2. Paul Beckett, RMIT University, Australia, ECE
3. Brandon Cahoon, University of Massachusetts, Computer Science
4. Danai Chasaki, University of Massachusetts, ECE
5. Scott Chin, University of British Columbia, Canada, ECE
6. Jérémie Crenne, University of South Brittany, France, ECE
7. Basab Datta, University of Massachusetts, ECE
8. Jeongseon Euh, University of Massachusetts, ECE
9. Andres David Garcia Garcia, Ecole Nationale Superieure des Telecommunications, France, ECE
10. Christophe Huriaux, University of Rennes I, France, ECE.
11. Priyank Kalla, University of Massachusetts, ECE.
12. Samamon Khemmarat, University of Massachusetts, ECE.
13. Martin Labrecque, University of Toronto, Canada, ECE.
14. Andrew Laffely, University of Massachusetts, ECE.
15. Vijay Lakamraju, University of Massachusetts, ECE.
16. Guy Lemieux, University of Toronto, Canada, ECE.
17. Cao Liang, Worcester Polytechnic Institute, ECE.
18. Valovan Manohararajah, University of Toronto, Canada, ECE
19. Vincent Migliore, University of South Brittany, France, ECE

20. Sohan Purohit, University of Massachusetts, Lowell, ECE
21. Diego Puschini, University of Montpellier II, France, ECE
22. Rance Rodrigues, University of Massachusetts, ECE.
23. Renaud Santoro, University of Rennes, France, ECE
24. Deshanand Singh, University of Toronto, Canada, ECE.
25. Sharad Singhai, University of Massachusetts, Computer Science
26. Romain Vaslin, University of South Brittany, France, ECE
27. Edward Walters, University of Massachusetts, Computer Science
28. David Whelihan, Carnegie Mellon University, ECE.