# A Dynamically-Reconfigurable Phased Array Radar Processing System

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***Abstract*—Digital beamforming is an important radar processing technique used in many communication and radar sensing applications. This paper presents a low-cost digital beamforming system which takes advantage of four eight-channel analog-to-digital (A-to-D) converter chips and dynamic FPGA reconfiguration. A full digital beamforming algorithm capable of forming up to 24 beams from 64 antenna input signals is described. FPGA reconfiguration is performed in 400 ms allowing for FPGA retasking of the associated radar for weather and aircraft tracking. Beamforming performance of 64.2 GOPs per second for weather tracking and 72.2 GOPs per second for aircraft tracking is reported. The complete low-cost digital beamforming board, including parts and assembly, costs less than $3,000.**

## I. Introduction

As phased array technology has progressed, the use of solid state radar systems has become diversified [1]. A single array may now be used for a variety of purposes including communications, weather sensing, and aircraft tracking. Both the hardware specialization and dynamic reconfigurability offered by contemporary FPGAs offer unique opportunities to customize beamforming to specific application needs. FPGA hardware can be specialized to focus the radar beam in one or more directions and dynamic FPGA reconfiguration can be used to allow the phased array to support multiple sensing tasks. As the required sensing task changes, a new beamforming design is swapped into the FPGA.

In this paper, a new FPGA-based digital beamforming system which costs less than $3,000 for all components, manufacturing, and assembly is presented. A low-cost system board leverages eight-channel analog-to-digital (A-to-D) converters to support the sampling of 32 separate antenna channels at up to 65 MHz. A-to-D outputs are connected to an Altera Cyclone III FPGA via low voltage differential signaling (LVDS). Following digital beamforming in the FPGA, data products are transferred to a PC via a gigabit per second Ethernet link. Dynamic FPGA reconfiguration forms a critical component of this system as it allows for switching between aircraft and weather radar targets in about 400 ms.

## II. Background

### A. Digital Beamforming

The ability to transmit and receive RF energy in a specific direction plays a crucial role in all radar applications. Forming a beam and electronically scanning it over a range

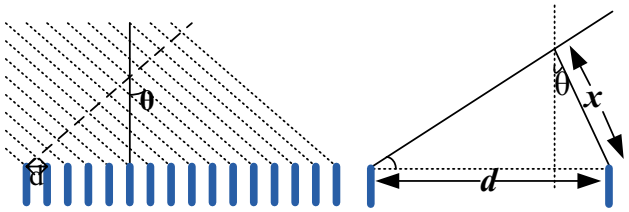


Figure 1. A linear array of antennas with a plane wave with angle of arrival $\theta$. Antennas in the array are spaced at distance **d**

of space can be done using an array of antennas with input/outputs that can be phase shifted with respect to one another. On receive, *phased array* beamforming is performed by taking advantage of the time delay of a wavefront as it reaches different antenna locations in the array. If the wavefront arrives broadside to the array ($\theta$ = 0), the wavefront will reach each element at the same time and produces a signal s(t). However, if the wavefront hits the array at an angle, the signal received at an element will be delayed relative to its neighbor by an amount proportional to the element spacing and the angle of incidence. This effect is illustrated on the left in Fig. 1. The signal at the $m_{th}$ element will be $s_m(t) = s(t - mt_d)$ where $t_d = \frac{X}{c_o} = \frac{dsin(\theta)}{c_o}$ and $c_o$ is the speed of light.

To maximize the signal received from a particular direction, a beamforming system imposes a compensating delay, $\mathbf{mt}_o$, on the received signal at the $\mathbf{m}^{th}$ element and then combines all **M** signals to form signal **C** as described by

$$C = \sum_{m=0}^{M-1} a_m s_m(t + mt_o) \quad (1)$$

where $a_m$ is an amplitude weighting factor that is sometimes used. When the angle $\theta$ is such that $t_d = t_o$, then the delay compensated signals are aligned and they reinforce each other, maximizing **C**. Wavefronts coming from other angles will have different delays that are not equal to $t_o$ and the beamformer will not align them. Gain can be greatly reduced for those signals.

Generally, the $s_m(t)$ signals are sinusoidal functions with frequency $\omega$ and slow (relative to $\omega$) modulations of amplitude and phase. The modulations of amplitude and phase are what carry information about the target. Since $s_m(t)$ is sinusoidal, it is convenient to represent it in terms of a complex signal:

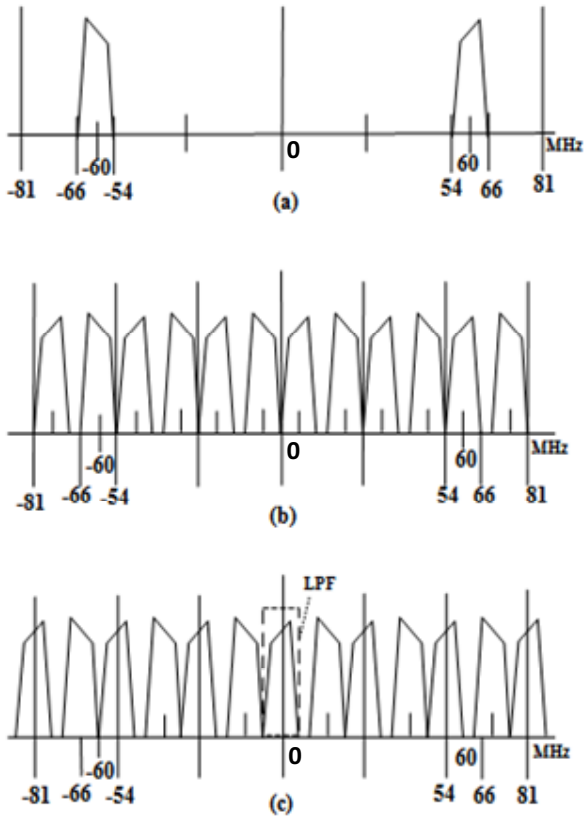


Figure 2. Beamforming preprocessing operations (a) IF spectrum (b) after sampling (c) after detection

$$s_m(t) = Re\left[(I + jQ)e^{j\omega(t-mt_d)}\right] \tag{2}$$

where I and Q are slow functions of time (several MHz) which carry the magnitude and phase information that the receiver is required to detect. When written in the complex signal form, the modified $\mathbf{m}^{th}$ signal becomes,

$$\begin{aligned} &a_m s_m(t + mt_o) = \\ &Re\left[(I + jQ)(a_m e^{j\omega mt_o})e^{j\omega(t-mt_d)}\right] \end{aligned} \tag{3}$$

where the second term on the right hand side is a complex weight which includes the amplitude weighting and delay found in (1). In (3) it can be seen that, when the incidence angle $\theta$ is such that $t_d = t_o$, then the **m** dependent terms in the exponent cancel and all element signals in (1) sum constructively.

In an analog beamformer, the weighting and summation operations occur at high frequency whereas a digital beamformer performs weighting and summing digitally at baseband frequencies. This paper is focused on digital beamforming, which is gaining in popularity for contemporary radar systems.

*1) Beamforming Preprocessing:* Before digital beamforming operations can take place, each received antenna signal is subjected to a series of preprocessing steps including *downconversion*, *sampling*, *demodulation*, and *filtering*. The signal, $s_m(t)$, received by the $\mathbf{m}^{th}$ antenna element is downconverted to an intermediate frequency ($\omega t \rightarrow \omega_{IF} t$) and filtered to remove spurious channels (such as the image channel). In our application, signals are downconverted from near 10 GHz to a 60 MHz intermediate frequency (IF). These signals have an information bandwidth of 12 MHz, as seen in Fig. 2a.

Each downconverted analog signal is subsequently sampled by an analog-to-digital converter (ADC) which effectively replicates copies of the IF spectrum at integer multiples of the sampling frequency. For example, if a signal with the passband shown in Fig. 2a is sampled at 27 MHz ($t_s = 1/f_s = 37$ nS), the frequency response shown in Fig. 2b is generated. The lowest sideband pair, centered at +/- 6 MHz, is the only information that is of interest in the result. In selecting a sampling rate, it is important to ensure that the passband reflections do not overlap because this event would lead to a loss of information. After sampling, all processing takes place digitally (in our case in an FPGA).

Once each signal has been sampled and converted to a digital data sequence, it is demodulated using a digital detector. Demodulation is performed by multiplying the $n^{th}$ member of the sequence by two coefficients, $\cos(2\pi f_d n t_s)$ and $-\sin(2\pi f_d n t_s)$ to produce two new sequences which, after low pass filtering, we define as $I_m(nt_s)$ and $Q_m(nt_s)$ respectively. The demodulation frequency, $f_d$, is the mid frequency of the lowest band in Fig. 2b. For the example with 12 MHz information bandwidth in Fig. 2, $f_d$ is the 6 MHz mentioned earlier.

The demodulation operation shifts the spectrum centered at 6 MHz in Fig. 2b down so that the lowest band is centered around f = 0. This effect is illustrated in Fig. 2c where it is apparent that the baseband spectrum is asymmetric, indicating that the corresponding digital sequence is complex. The $I_m$ and $Q_m$ sequences are the real and imaginary parts of that sequence. For the $m^{th}$ antenna element, the complex sequence corresponds to the phase shifted baseband sequence (see (3)),

$$I_m + jQ_m \equiv [I + jQ]e^{-j\omega mt_d} \tag{4}$$

where the $\omega$ is the original RF frequency. It was not downconverted because it was not multiplied by the variable t.

The FPGA detector/filter can be configured as needed for different baseband requirements.

*2) Digital Beamforming Operations:* Digital beamforming occurs when the delayed baseband sequences represented by (4) are weighted and summed so that:

$$\sum_{m=0}^{M-1} (I_m + jQ_m) W_m = (I + jQ) AF(\theta) \quad (5)$$

where

$$AF(\theta) = \sum_{m=0}^{M-1} e^{-j\omega m t_d} a_m e^{j\Psi_m} \quad (6)$$

$W_m$ is the weighting factor introduced in (3), $W_m$ = $a_m$cos($\Psi_m$) + j$a_m$sin($\Psi_m$), and $\Psi_m$ = m$\omega$t$_o$ (see also, (3)). AF($\theta$) is called the *array factor.* The outputs of the beamformer are two sequences, the real and the imaginary parts of the right side of (5). I and Q are time dependent (functions of nt$_s$) and contain the baseband information, but have no $\theta$ dependance. The array factor depends on $\theta$, but is not time dependent. Although it is complex, its magnitude is the important part.

The magnitude of AF is maximized at the value of $\theta$ where the $\Psi_m$ just compensates for the t$_d$ delays. As stated in Section II.A, waves can be incident on the array from a variety of angles $\theta$, causing sets of signals with delays $mt_d$= $\frac{m(dsin\theta)}{c_o}$. To maximize AF for waves incident at a particular angle, $\theta_o$, the compensating phase shift for the m$^{th}$ antenna should be set to $\Psi_m$ = m$\omega$t$_o$ = $\frac{m\omega(dsin\theta_o)}{c_o}$. This shift causes the m dependent phase terms in (6) to cancel when $\theta$ = $\theta_o$. In the special case where all $a_m$ are chosen equal to a constant, say 1.0, the array factor has a maximum value M when $\theta$ = $\theta_o$. At other incident angles, phase compensation does not occur and the array factor is much smaller and can even show nulls at certain angles.

For many applications, beams corresponding to different $\theta$ values must be formed simultaneously or at different points in time. FPGA beamformers can be configured so that the same set of data {I$_m$, Q$_m$} can be operated on by multiple sets of {W$_m$} to produce multiple beams.

### B. FPGA based Digital Beamforming Systems

Digital beamforming using FPGAs has become a popular technique for many military and commercial radar systems. Generally, these systems have the following characteristics:

1) Multiple boards of ADC and FPGA components are required to sample numerous analog channels and integrate partial beamforming results.
2) The beamforming hardware implemented in the FPGA is generally static throughout the operation of the radar system except for possible beamforming coefficient, $\mathbf{W}_m$, updates.
3) The cost associated with a multi-board beamforming system is often greater than $100,000.

Several recent research projects have used FPGAs to perform beamforming. A multi-component system [2] uses five separate cards and samples up to 20 analog channels with individual ADCs. Five Virtex II devices are subsequently used to form up to four beams. A larger system [3] uses 32 separate ADC boards to sample radar signals at 100 MHz. Sampled data is then transmitted serially to a single Virtex II device via optical fibers. A single beam is formed within the FPGA. A similar system [4] uses six ADCs to implement beamforming for a six-ring annular array ultrasound transceiver. A single beam is formed using a Virtex device. Ma et al. [5], developed a digital beamforming system for 32 analog channels which includes four 8-channel ADC boards, four data interfacing boards, a beamforming board, and a beamforming coefficient generation board. Although effective, all of these systems require numerous discrete boards and components, increasing system cost and complexity.

Several recent digital beamforming systems take advantage of multi-channel ADCs. An 8-channel beamformer [6] interfaces analog signals to two four-channel ADCs. Up to 8 FPGAs are used to perform beamforming. A recent system [7] uses a single 8-channel TI ADS5273 ADC with eight serial outputs in conjunction with a Virtex 5 FPGA to form a single beam. Although these systems provide increased integration, no evidence of dynamic FPGA reconfiguration or integrated support for up to 32 analog channels in a single board is provided.

### C. Dynamic FPGA Reconfiguration

The flexibility of contemporary FPGAs extends beyond their ability to implement specialized logic. These SRAM-based devices can be reconfigured in the field, often while system operation progresses. Dynamic FPGA reconfiguration has been used successfully in a variety of application areas including communications, networking, encryption, and signal processing. Generally, dynamic reconfiguration requires the preparation of multiple FPGA bitstreams that can be swapped into the FPGA as needed prior to system operation. In the case of beamforming, the number of beams, the data rate of the sampled data, and the amount of FPGA power consumption may all be factors in determining the benefit of dynamic FPGA reconfiguration. Previous FPGA-based systems have shown the ability to significantly reduce power consumption by swapping in more power-efficient hardware when less FPGA processing is required. In contrast, in this paper, the ability to support multiple real-time applications is addressed.

## III. Experimental System

### A. Digital Beamforming Hardware Platform

The system architecture consists of analog and digital sections. The analog section directly connects 32 single-ended IF signal lines to the board via SMA connectors. After conversion to differential signaling, the 32 signals are sent to four 8-channel Analog Devices AD9212 A/D chips which digitize the analog signals to 10-bit samples. The analog-to-digital converters operate at up to 65 MSPS. The 32 ADC outputs are interfaced serially to an Altera EP3C120 Cyclone

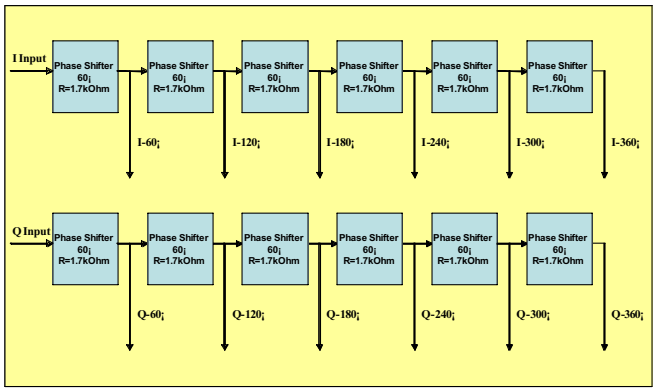


Figure 3. Phase shifts in test circuit

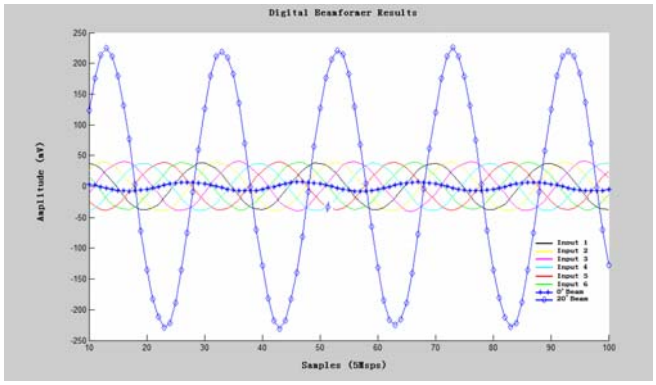


Figure 4. Digital beamforming results for a 150 KHz baseband signal

III device via low voltage differential signaling (LVDS) in the digital section of the board. The FPGA houses all of the digital downconversion and beamforning logic, a NIOS II soft-core processor, a gigabit Ethernet core, a 10/100 Ethernet core, a serial interface, and a JTAG interface.

The 10/100 Mbps Ethernet interface is used as a control interface and a download mechanism for new digital beamforming coefficients. The Gbps Ethernet interface is used to transmit the results of beamforming to an external PC. The FPGA can be programmed via either the JTAG interface or an on-board EPROM.

### B. Target Radar System

The digital beamforming system described in Section III.A has been specifically designed to interface to a modular 64-channel phased array prototype under development at the University of Massachusetts, Amherst as part of the Collaborative and Adaptive Sensing of the Atmosphere (CASA) project.

The system includes a phased array radar panel which can tilt in the vertical direction. A digital receiver which can perform a series of radar processing steps (demodulation, filtering, and beamforming) and a host computer system for network connectivity and data storage is attached to this phase tilt radar. The phase tilt array antenna consists of 64 dual polarized columns each containing 32 microstrip patch antennas. Each antenna transmits at 9.36 GHz (X band). Each column is controlled by a solid state transmit/receive (T/R) module and can be considered a separate element in a linear array. The radar focuses beams in the horizontal (azimuth) dimension by phase adjusting transmitted signals. Beam steering in the vertical (elevation) plane is performed mechanically. The solid state phase tilt radar contains four subpanels of 16 antenna columns. Up to four subpanels can be combined to form 64 total analog transmit/receive columns. These compact arrays measure 1m wide x 0.5m tall and can be mounted on existing infrastructure such as a cell phone tower or a building rooftop.

## IV. Experimental Approach

### A. FPGA-based Digital Beamforming Block

The FPGA-based beamforming blocks used for experimentation are based on a multiply-accumulate structure. Each beamforming block performs four multiply operations and the addition operations shown in (5). Each complex multiplication is implemented using six 9x9 integer multipliers inside the FPGA. Coefficients are streamed out of FPGA block memory as I and Q values become available. Every cycle, an I-Q pair and its respective complex coefficient are loaded into registers and enter the four-stage complex multiplier pipeline. The result is accumulated until a predetermined number of pairs have been processed. A state machine is used to control the operation of the beamforming block.

### B. Experimental Validation

An analog test circuit was implemented and interfaced to the platform to assess the functionality of the 32-channel FPGA-based beamforming platform. In this initial test, only the beamforming function of the platform was tested, and not the detector, filter, and decimator parts of the design. The full design including these components is discussed in Section V. In this initial test, the outputs from a pair of signal generators are phase locked to create I and Q components of a 150 kHz, 150 mV peak-to-peak sinusoid. As shown in Fig. 3, these I and Q signals are then input to a network of analog phase shifters that produce six outputs for I and six outputs for Q with equal amplitude and phase. The sequences that result after sampling correspond to the six pairs of ($I_m$, $Q_m$) that would normally be generated by a digital detector followed by low pass filtering. Thus, 150 kHz is the baseband frequency. The $\{I_m, Q_m\}$ pairs roughly correspond to a plane wave incident on a six element linear antenna array. The delay elements in the test circuit generate an input pattern that roughly corresponds to an incident angle of $20^o$. This angle was chosen because it results in minimal gain for a 6-element array when the signals are combined without phase correction. Equation 7 shows that

Table I
WEATHER AND AIRCRAFT TRACKING SPECIFICATIONS

| Spec. | Weather | Aircraft |
|---|---|---|
| Bandwidth | 3 MHz | 12 MHz |
| Sample Rate | 27 Msps | 27 Msps |
| Throughput | 6 Msps | 27 Msps |
| OPS per Beam | 2676 MOPS | 12042 MOPS |
| # of Beams | 24 | 6 |
| Total OPS | 64.2 GOPS | 72.2 GOPS |

a 20 degree azimuth angle corresponds to an inter-element phase difference $\mathbf{\Psi}$ of about 60 degrees, leading to a nearly even phase spacing for 6 elements across 360 degrees and resulting in near maximum rejection.

$$2\pi * \frac{d}{\lambda} * \sin(\theta) = \Delta\rho \Leftrightarrow 2\pi * \frac{\lambda/2}{\lambda} * \sin(20) = 61.25^\circ \quad (7)$$

The outputs from the signal generators were input directly to the A/D converters to check phase alignment. Phase differences were negligible up to 2 MHz. Two beams were formed using the beamforming blocks described in Section IV.A and compared in Fig. 4 to the six $I_m$/$Q_m$ pair input signals. The digital beamforming (DBF) circuits used to produce these beams consisted of two DBF blocks which performed a total of 16 multiply and accumulate operations. The circuit consumes 8,320 LUTs. Fig. 4 illustrates the six I input signals and the real (in-phase) results of the beamformed signals for $\theta$ angles of $0^o$ and $20^o$. The plots indicate that the beam formed at zero degrees has negative gain, as expected, while the beam formed at 20 degrees has a gain of about 6 times the input signal, also as expected.

A comparison between beamformed data generated by the FPGA and results determined by MATLAB for the same sampled input data collected from the board showed a disparity of about 1%. This difference is due to quantization error resulting from the use of truncation in the hardware beamformer (10-bit multiplications). MATLAB uses 64-bit operations and a more accurate rounding scheme when performing calculations.

## V. FPGA RADAR APPLICATION PERFORMANCE

This section describes the results of implementing beamforming circuits for two distinct radar applications: weather sensing and aircraft tracking. The use of dynamic reconfiguration allows for the near-simultaneous use of beamforming circuits for both of these applications in a multifunction radar.

### *A. Digital Beamforming for Weather Applications*

The tracking of distributed target objects such as storms benefits greatly from multiple beams (>20), but does not require a great deal of bandwidth (about 3 MHz) due to the relatively slow moving nature of weather masses. The beamforming circuit designed for weather tracking uses 64 I/Q pairs derived from 64 phased array antennas. The 64 inputs can be interfaced to the 32 analog inputs on the DBF board using external 2-to-1 analog multiplexing. A per-beam throughput of 6 MSPS is required for weather tracking to meet the bandwidth requirement of 3 MHz with 2x oversampling. Since data is initially sampled at 27 MHz, slightly more than 75% of post-filtered data is discarded to support downsampling. Each weather-tracking beam is formed using the 64 I/Q pairs received from the antennas and 6-bit coefficients. A total of 4 beamforming blocks operating at 96 MHz perform the required multiply-accumulate operations. Each block performs 16 10-bit multiply-accumulates and the results are summed using an adder tree. MAC results of 20 bits are generated and following summation, 16-bit beamformed results are retained.

The second column of Table I summarizes the specification for the weather radar and Table II indicates the amount of resources required for the beamforming implementation. A total of 94,800 logic elements (LEs) are used, of which 24,048 are required for beamforming. A total of 576 embedded multiplier blocks are used for the complex multiplication. The other blocks implemented in the FPGA

Table II
WEATHER AND AIRCRAFT TRACKING DBF RESULTS FOR 64 ANTENNAS

| Application | Weather Tracking 6 MSPS per beam 96 MHz | | Aircraft Tracking 27 MSPS per beam 108 MHz | |
|---|---|---|---|---|
| # of Beams | 1 beam | 24 beams | 1 beam | 6 beams |
| Logic Usage (LEs) | 1,002 | 24,048 | 4,122 | 24,732 |
| DSP Usage | 24 mult | 576 mult | 96 mult | 576 mult |
| Dyn. Power (mW) | 27.13 | 528.65 | 91.67 | 563.40 |

Table III
LOGIC USAGE AND MAX THROUGHPUT FOR FPGA BLOCKS USED FOR WEATHER TRACKING. A TOTAL OF 6 MSPS IS ACHEIVED PER BEAM. EXCEPT FOR DBF CORES, THE VALUES FOR AIRCRAFT TRACKING ARE THE SAME. A TOTAL OF 30 MSPS PER BEAM IS ACHIEVED FOR AIRCRAFT TRACKING.

| Weather Tracking | | |
|---|---|---|
| Module: | Logic Usage (LEs) | Max Throughput |
| Deserializer | 490 | 60 MSPS |
| IQ Demodulator | 5698 | 30 MSPS |
| FIR filter/w Decimation | 52460 | 30 MSPS |
| DBF Cores | 26442 | 6 MSPS per beam |
| Gbit MAC | 1852 | 31.25 MSPS |
| Ethernet MAC | 4097 | 1.5 MSPS |
| NIOS II | 3369 | – |
| Misc | 392 | – |
| Total: | 94800 | – |

include input deserializers, an I/Q digital downconversion core, 128 channel FIR filter, NIOS II microprocessor, Ethernet interface, Gbit Ethernet hardware MAC, and various glue logic and control state machines. The throughput and logic consumption of these blocks are shown in Table III. The results of several beams were forwarded from the platform to an external PC via Gbit Ethernet to verify accurate beamforming operation.

### B. Digital Beamforming for Aircraft Tracking

Single-point target applications, including aircraft tracking, require significantly more bandwidth (about 12 MHz) but do not demand a large number of parallel beams. The requirement of a higher bandwidth necessitates higher per-beam throughout. For example, aircraft tracking requires at 12 MHz bandwidth pulse, which translates to a minimum required beam throughput of 24 MSPS, according to Nyquist requirements. This throughput is achieved by performing only four multiply accumulates per beamforming block (complex multiply-accumulate) and increasing the number of beamforming blocks per beam to 16. An adder tree combines the 16 18-bit multiply-accumulate results to generate 16-bit beamforming results. A total of 6 beamforming circuits operating at 108 MHz are implemented. The requirements of the aircraft tracking application are shown in the third column of Table I.

Table II indicates the amount of resources required for the implementation. The beamforming blocks provide for 27 MSPS bandwidth for each of the 6 beams. A total of 93,029 LEs are used, of which 24,732 are required for beamforming. The other FPGA blocks are the same as listed for weather processing in the previous subsection.

### C. Dynamic FPGA Reconfiguration

As seen in the previous two subsections, the beamforming circuits required for both weather and aircraft tracking differ considerably in structure and required throughput per beam. The following specific reasons preclude the inclusion of *both* circuits in the FPGA at the same time.

- The number of required 9-bit multipliers for a combined circuit (1152) would exceed the available 9-bit multipliers in the FPGA (576).
- The structures of the data paths and complex multiply accumulate blocks for the two designs are significantly different. The overhead required to multiplex circuitry between the two designs would be prohibitive.

As a result, the beamforming hardware needed to support a multifunction radar must require hardware reconfiguration to allow for both radar functions in real-time. Through experimentation, it was determined that a new configuration can be swapped into the FPGA every 400 ms under external system control. A reconfiguration pulse is sent to the board via the 10/100 Mbit Ethernet port to commence reconfiguration. An Altera EP3C120 Cyclone III configuration file contains 16.5 Mbits when uncompressed and 10.7 Mbits when compressed. The proper configuration is externally selected and transferred serially at 100 MHz from the on-board configuration EPROM to the FPGA. This configuration rate supports a radar pulse rate for both applications of about 200 to 1000 pulses/second if the configuration is updated every few hundred pulses.

### D. Overall Digital System Cost

An important aspect of the integrated digital beamforming system is its low cost. In total, the platform, including all components costs about $3,000. This cost includes $1,000 for the PCB manufacture, $600 for assembly, $400 for the FPGA, $200 for the four ADCs, and $700 for miscellaneous components. This cost is in direct contrast to previous multi-board systems [4]-[7] which cost at least $20,000.

## VI. Conclusions

This project has explored the design and implementation of a low-cost digital beamforming platform. This FPGA-based system supports 65 MHz sampling for up to 32 analog channels. The board analog inputs and FPGA beamforming circuits have been tested to verify system operation. Up to 72.2 GOPs per second have been performed for weather tracking beamforming. Dynamic reconfiguration is used to retask the beamforming circuit between weather and aircraft tracking. The low cost of the system facilitates its easy integration into phased array radar systems.

## References


[1] R. Hendrix, "Aerospace system improvements enabled by modern phased array radar," in *Northrup Grumman white paper*, Oct. 2002.

[2] M. Gay and I. Phillips, "Advanced FPGA systems enable real-time adaptive beamforming for phased array radar," in *QinetiQ Corporation*, 2008.

[3] M. Fischman, C. Le, and P. Rosen, "A digital beamforming processor for the joint DoD/NASA space based radar mission," in *Proceedings of the IEEE Radar Conference*, 2004, pp. 9–14.

[4] P. Cao, K. Shung, N. Karkanis, and W. H. Chen, "Design of a real time digital beamformer for a 50 MHz annular array ultrasound transducer," in *Proceedings of the Ultrasonics Symposium*, 2002.

[5] X. F. Ma, W. X. Sheng, and F. Huang, "Development of two-dimensional digital beamforming receiving array system," in *Proceedings of the International Conference on Microwave and Millimeter Wave Technology*, 2008.

[6] *Heterogeneous Processing Platform FPGA Solutions for the IBM BladeCenter*, Annapolis Microsystems, 2009.

[7] C. Fernandez-Prades, P. Closas, and J. Arribas, "Implementation of digital beamforming in GNSS receivers," in *Proceedings of the European Workshop on GNSS Signals and Signal Processing*, 2009.