DE5 NetFPGA Packet Generator Design User Guide

Revision History

Date	Comment	Author
08/30/2014	Initial draft	Kekai Hu

Contents

1. Introduction

DE5 NetFPGA packet generator is an open source port of the NetFPGA packet generator on Altera DE5 board. This tutorial describes the steps to download the DE5 NetFPGA packet generator design from the project website, compile the design using Altera Quartus II software, and to verify the packet generator.

DE5 NetFPGA packet generator v1.0 ported NetFPGA 1G design and has been verified at 1Gbps speed. Next versions would target on 10Gbps packet generation.

2. System Requirements

To successfully install and test Packet Generator on DE5, you must satisfy the following system requirements.

Operating System Requirements

- Microsoft Windows (Verified with Windows XP)

Software Requirements

- Altera Quartus II 13.1 or later and Qsys Builder
- Microsoft Visual Studio 2010
- Jungo Windriver 32bit

Hardware Requirements

- PC with PCIe x8 or x16 slot.
- Altera DE5 board
- SFP+ Transceivers
- 10GbE Duplex Multimode LC/LC Fiber Patch Cable

IP License Requirements

- Altera 10G BASE-R PHY IP Core
- Altera 10G Ethernet MAC

Table 1 provides additional information on obtaining the hardware and software necessary to compile DE5 NetFPGA packet generator.

Table 1: Software and Hardware Requirements

Requirement	Source
Altera Quartus II 13.1 and Qsys Builder	https://www.altera.com/download/software/quartus-ii-se
Microsoft Visual Studio 2010	http://www.microsoft.com/visualstudio/en-us/try
Jungo Windriver	http://www.jungo.com/st/windriver_usb_pci_driver_development_software.html
Altera DE5 board	http://www.terasic.com.tw
Altera 10G Ethernet IP Core	http://www.altera.com/support/ip/interface-protocols/ips-inp-10gbe.html

Note: Altera provides a free time limited Open Core Plus core of 10G MAC Ethernet. This core is available as part of the Altera Quartus II software.

3. Installing DE5 NetFPGA Board in the Host PC

To operate Altera DE5 in PCI Express mode, perform the following two steps:

1. Enable PCI mode by setting the SW0 switch in **OFF** position as shown in Figure 1.

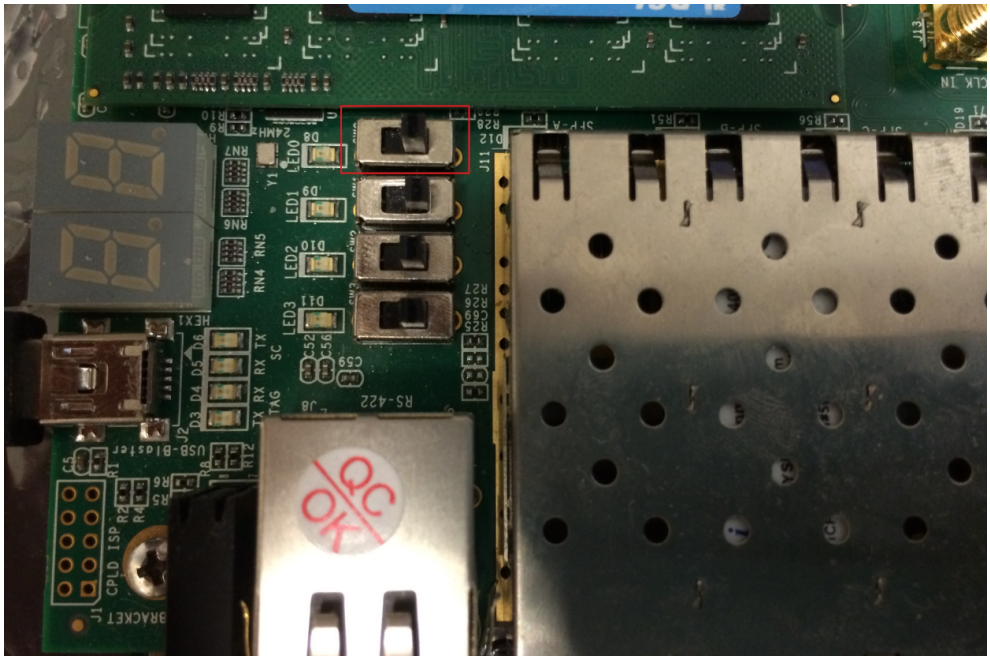


Figure 1: SW0 switch OFF position

2. Make sure the PCI Express Mode SW7 is switched to x8 mode. Table 2 lists the switch controls and description. Figure 2 shows the default configuration of SW7 on the bottom of the FPGA board.

Table 2: SW7 PCIe Control DIP Switch

Board Reference	Signal Name	Description	Default
SW7.1	PCIE_PRSNT2n_x1	On : Enable x1 presence detect Off: Disable x1 presence detect	OFF
SW7.2	PCIE_PRSNT2n_x4	On : Enable x4 presence detect Off: Disable x4 presence detect	OFF
SW7.3	PCIE_PRSNT2n_x8	On : Enable x8 presence detect Off: Disable x8 presence detect	ON

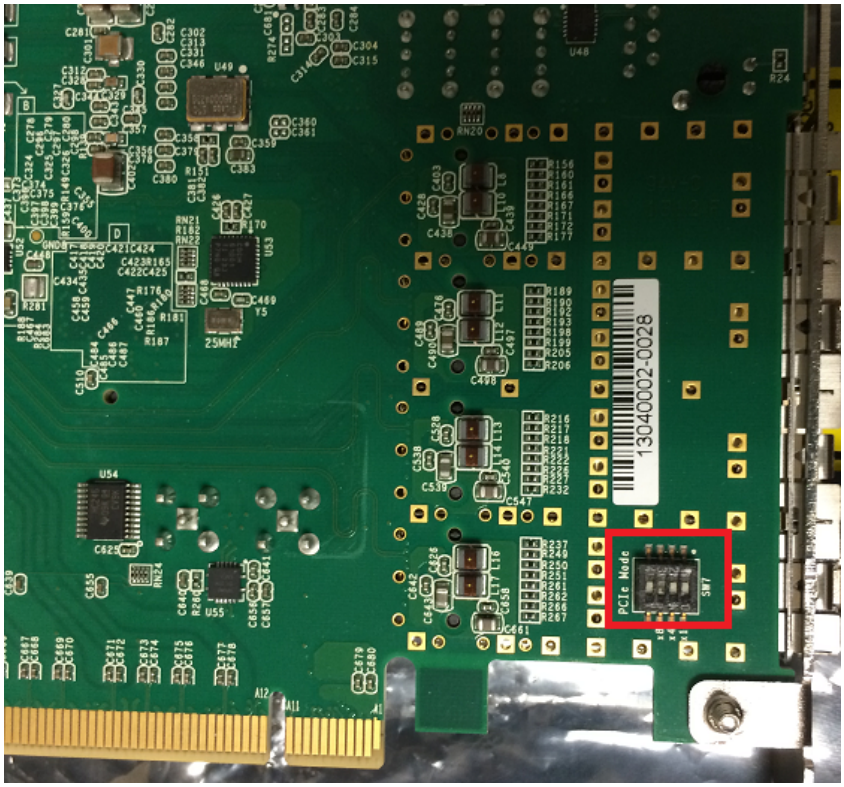


Figure 2: PCI Express Control DIP Switch

The PCI Express mode does not require a standalone power supply. Instead, the Altera DE5 board can be powered up through the x8 or x16 PCI Express edge connector attached to a PC as shown Figure 3.

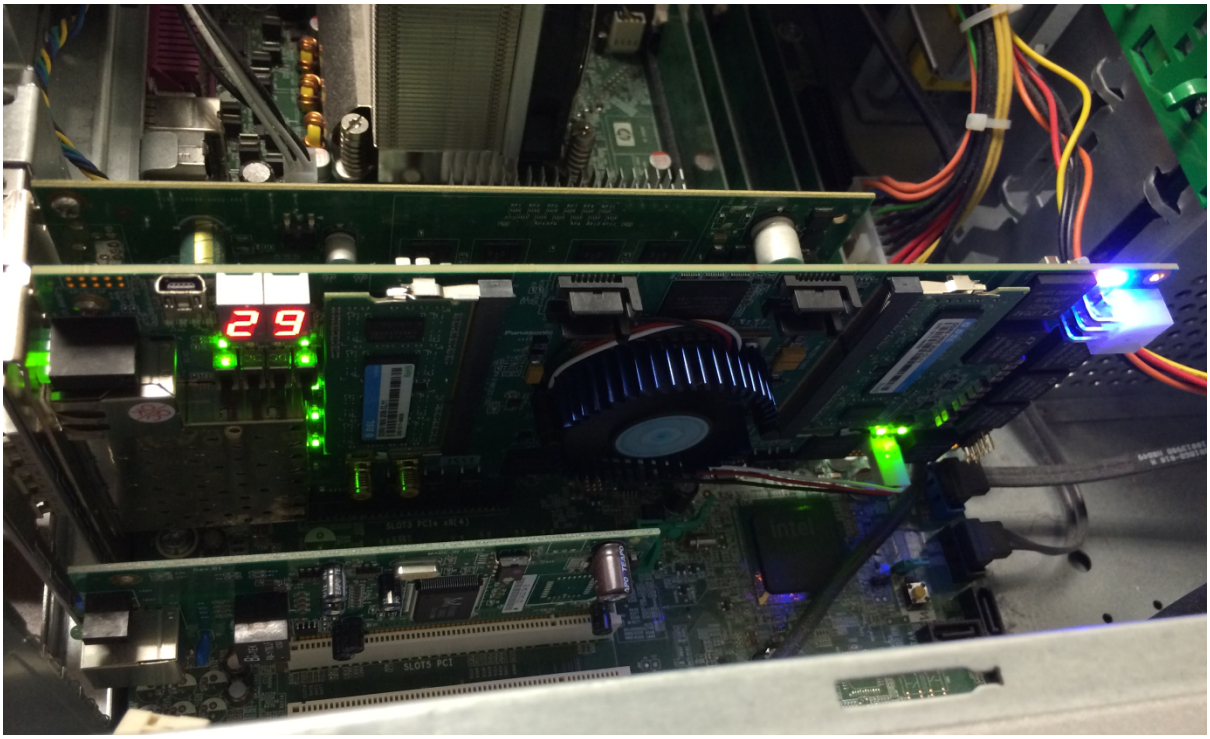


Figure 3: PCI Express Mode

4. Obtaining DE5 NetFPGA Packet Generator

The NetFPGA packet generator [3]. is a simple packet generator and capture tool for education and research purposes from Stanford University. The DE5 NetFPGA packet generator provides a port of the NetFPGA packet generator on the Altera DE5 platform. Download the gateware and software for DE5 NetFPGA packet generator as bundled as two separate packages:

- Download **DE5 NetFPGA Packet Generator project directories package (DE5_Packet_Generator.zip)** provided by University of Massachusetts, Amherst from [1]. A link to the repository is also available from the project website [1].
- Obtain the **DE5 Packet Generator package source code (DE5_Packet_Generator_v1.0.zip),** a modified version of Stanford University's NetFPGA packet generator design by sending an e-mail to Professor Russell Tessier (email:tessier@ecs.umass.edu).

- Unzip DE5_Packet_Generator.zip and DE5_Packet_Generator_v1.0.zip to the same directory. Unzipping DE5_Packet_Generator.zip will create the project directory.

- Unzipping DE5_Packet_Generator_v1.0.zip and copy the source code files in "src" directory to the "src" directory in the DE5_Packet_Generator project package.

5. Directory Contents

The projects folder contains the following subdirectories:

- **src** – The DE5 Packet Generator reference data path verilog source code files are placed here. You need to request these files from Professor Tessier.
- **sw** - It has one subdirectory **pcie_config**. 'pcie_config' contains the Visual Studio software application for configuring the packet generator in PCIe mode.
- **phy_10gbaser** and **phy_10gbaser_sim** – These two folders include all the Altera 10G Base-R Phy source code files for the 10G Ethernet PHY.

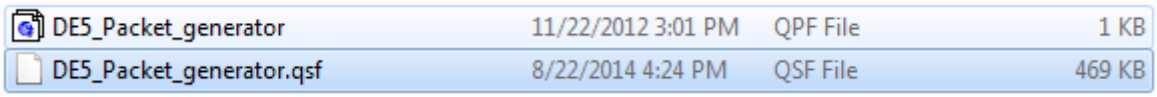
6. Compiling DE5 NetFPGA Packet Generator

Compiling the DE5 NetFPGA packet generator requires two separate packages as described in Section 4:

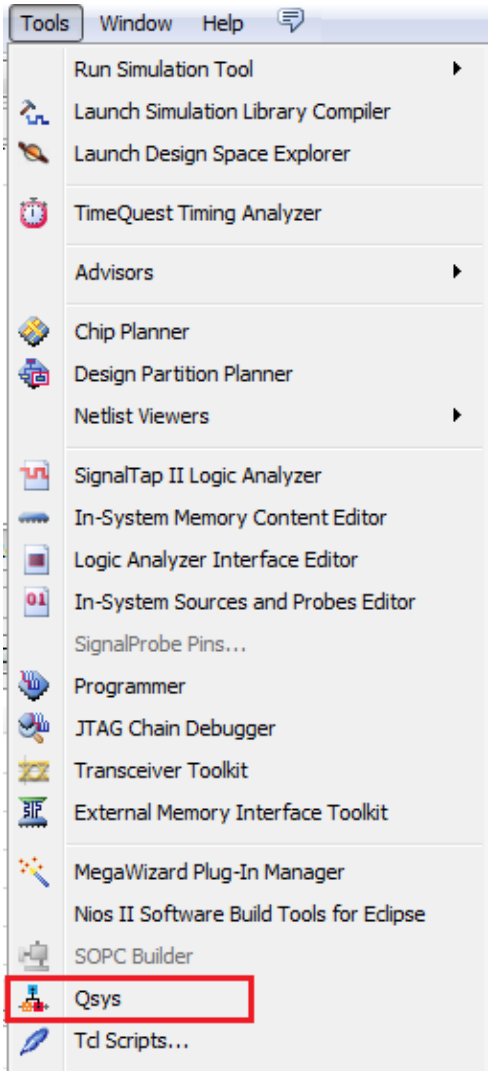
- DE5 NetFPGA directories package (**DE5_Packet_Generator.zip**).
- A modified version of the NetFPGA Packet Generator RTL source files (**DE5_Packet_Generator_v1.0.zip**).

The detailed compilation steps are described below:

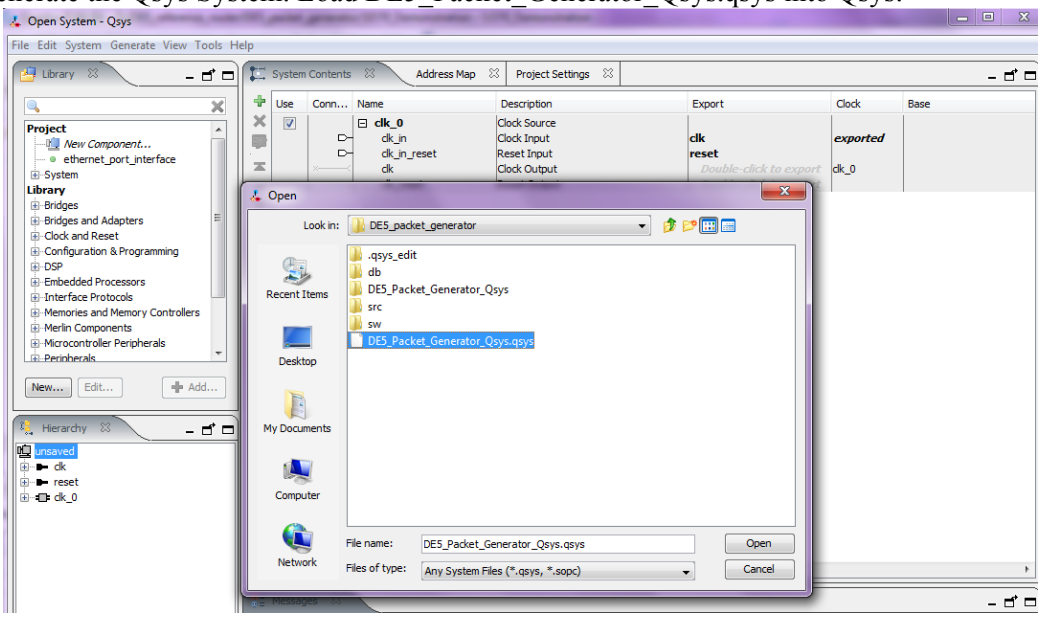
1. Open the DE5_Ethernet project in Quartus II by double clicking **DE5_ Packet_Generator.qpf**



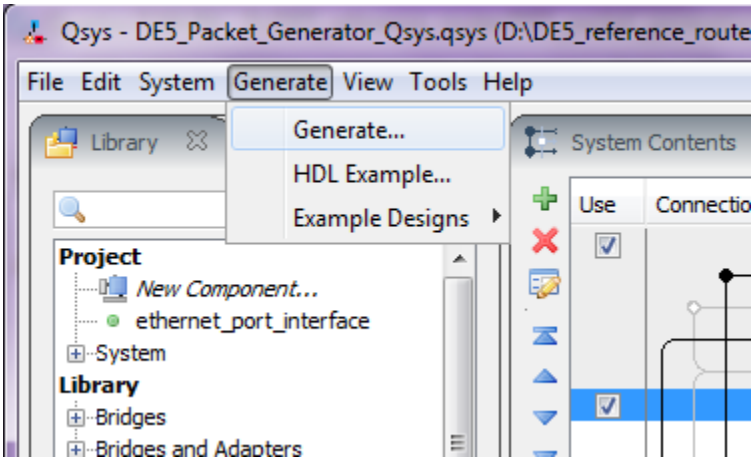
2. Open Qsys builder (Quartus → Tools →qsys)



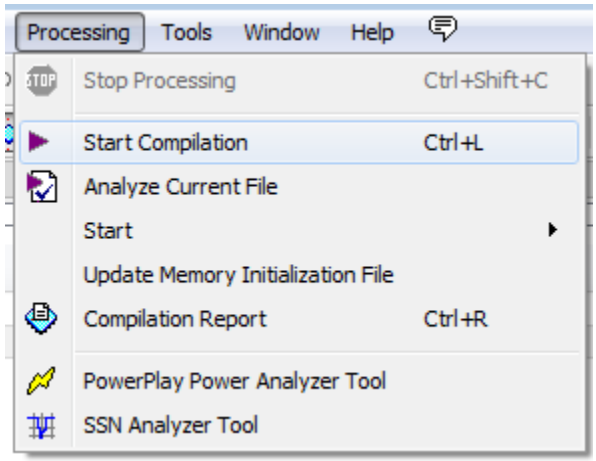
3. Generate the Qsys System. Load DE5_Packet_Generator_Qsys.qsys into Qsys.



4. Generate the design by click Generate → Generate.

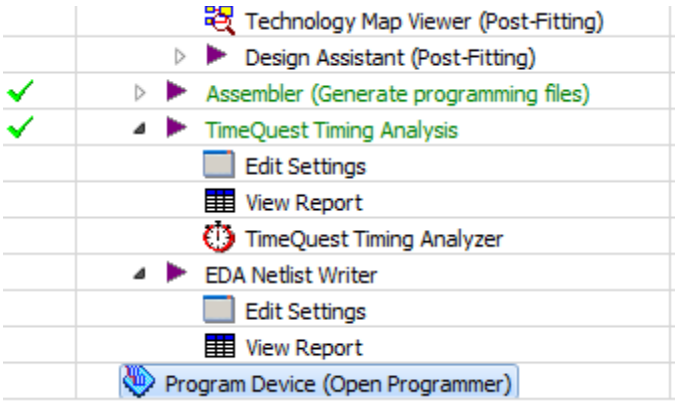


5. Once Qsys system generation is successful, compile the design from Quartus (In Quartus, Processing → Start Compilation).

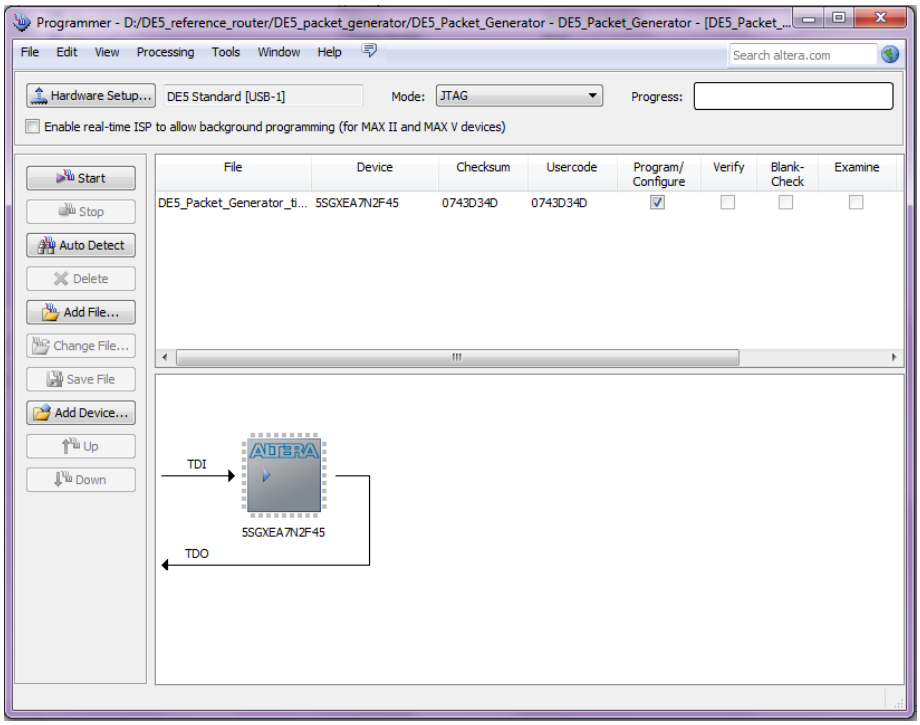


6. Install the DE5 board on the PCIe slot (Section 3). Make sure that the board is also connected to PC via the USB/JTAG cable.

7. Download the bit-file generated after the compilation to the target DE5 board by double clicking the "Program Device" in the Task Window.



8. Click Start in the Programmer window to begin download.



9. Reboot the host PC after downloading the bit-file.

7. Testing the DE5 NetFPGA Packet Generator

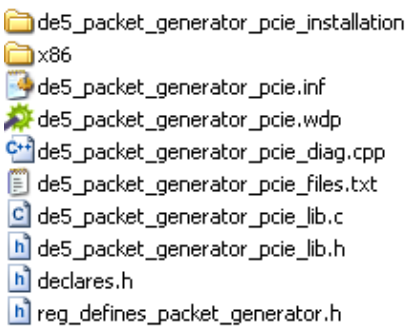
7.1. Configuring the DE5 NetFPGA Packet Generator

The DE5 NetFPGA packet generator can be used only in PCIe mode. After configuring the Altera DE5 board to be used in PCIe mode, the FPGA bit-stream must be downloaded through USB/JTAG cable. Now the packet generator functionality can be tested using the PCIe software.

Setting up PCIe software:

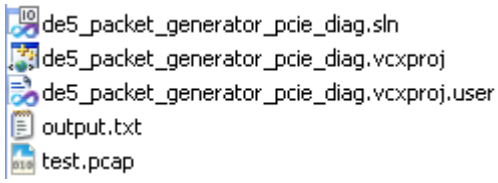
We use Jungo's Win Driver [7]. 32-bit to establish communication between the host PC running Windows XP and the Altera DE-5 board. Jungo's Win Driver exposes two APIs (OnRCSlaveWrite and OnRCSlaveRead) to applications to read and write using the PCI Express bus. We have developed a Visual Studio 2010 based application that uses these APIs to read and write the packet generator registers on the DE5 board. This application is available in **{project root}\sw\pcie_config** directory. **{project root}** refers to DE5_Packet_Generator project directory.

The file structure of the **pcie_config** folder is shown below:

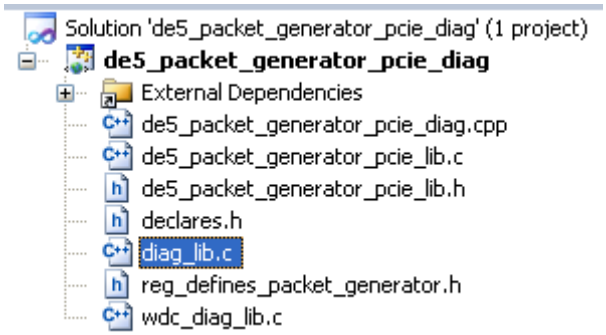


Perform the following steps to setup the PCIe software.

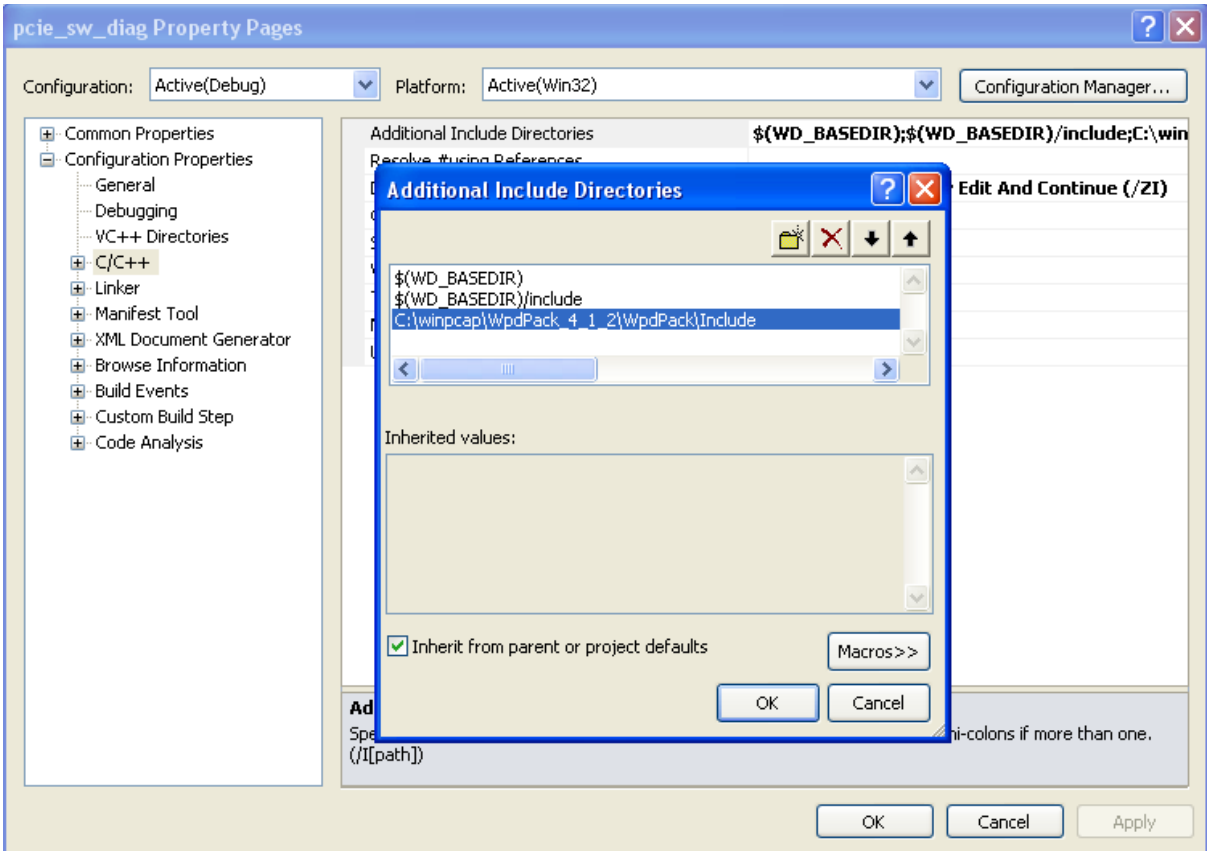
1. Navigate to **{project root}\sw\pcie_config\x86\msdev_2010**
2. Double click on de5_packet_generator_pcie_diag.sln



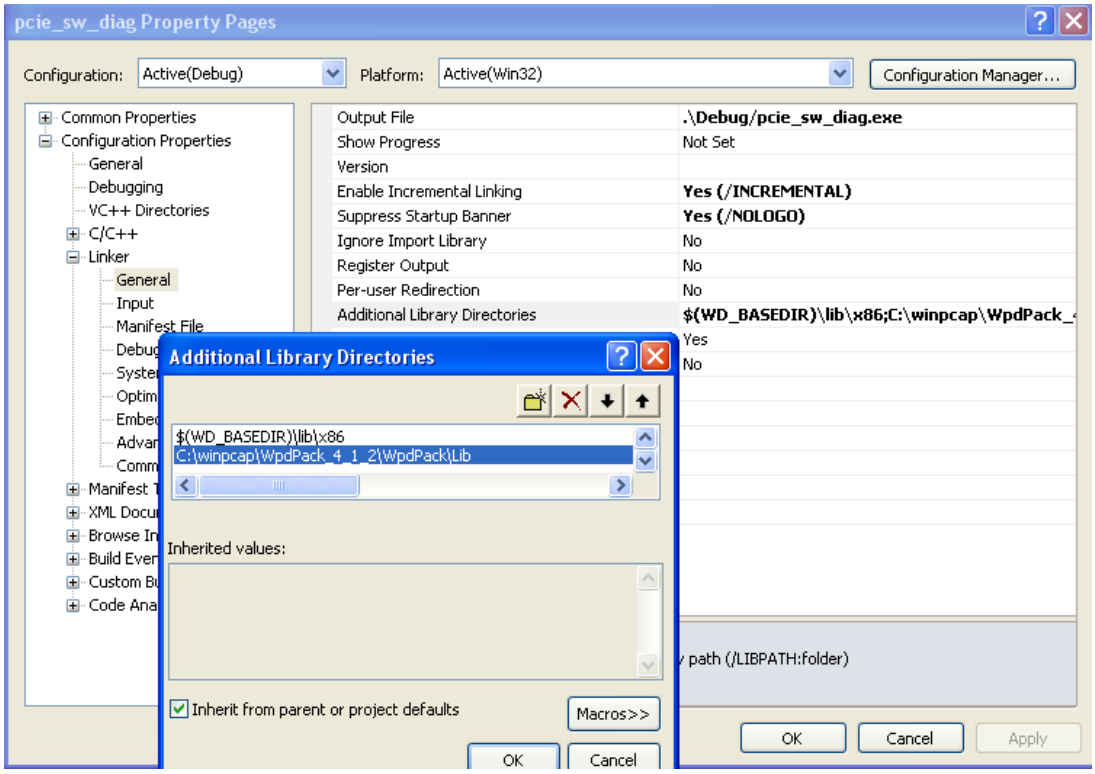
3. The Visual Studio 2010 window pops up with the following file structure.



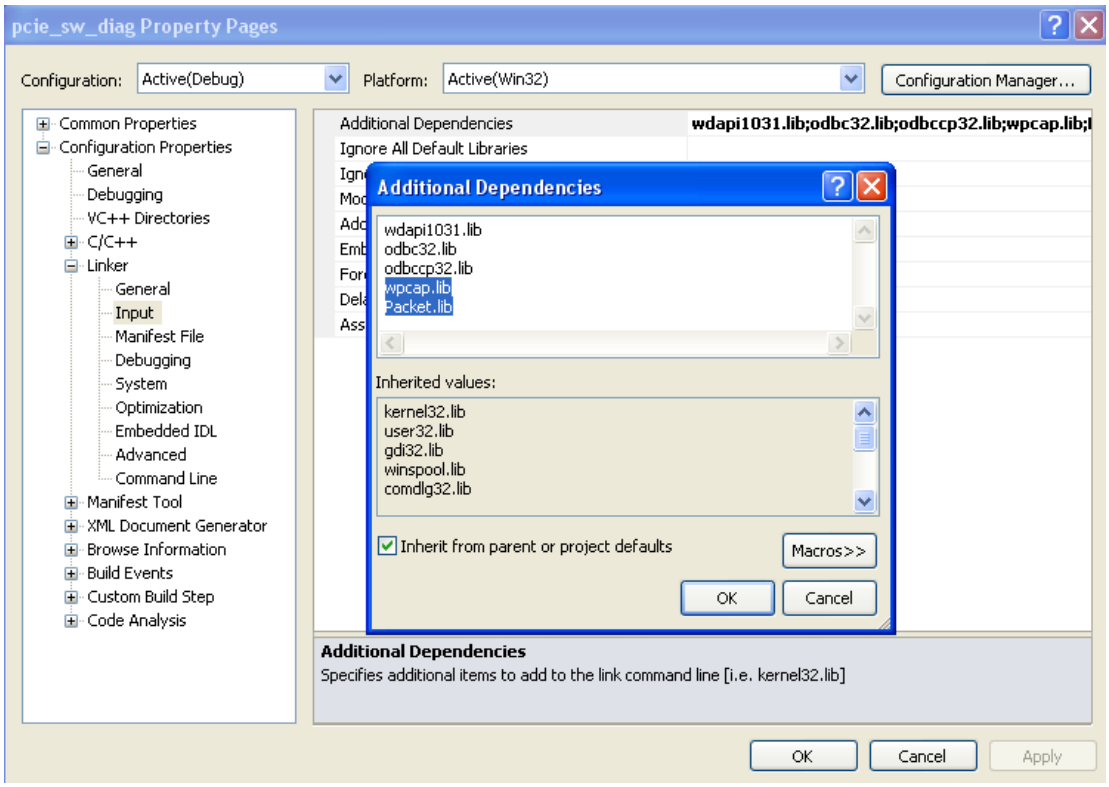
4. Install WinPcap driver [9]. and WinPcap developer's pack [10]. . The developer's pack is installed in the location "C:\WpdPack_4_0_2\WpdPack".
5. Link Visual Studio with the WinPcap libraries as mentioned below.
6. In Visual Studio, under the Configuration Properties → C/C++ → General tab, add the WinPcap include path to Additional Include Directories.



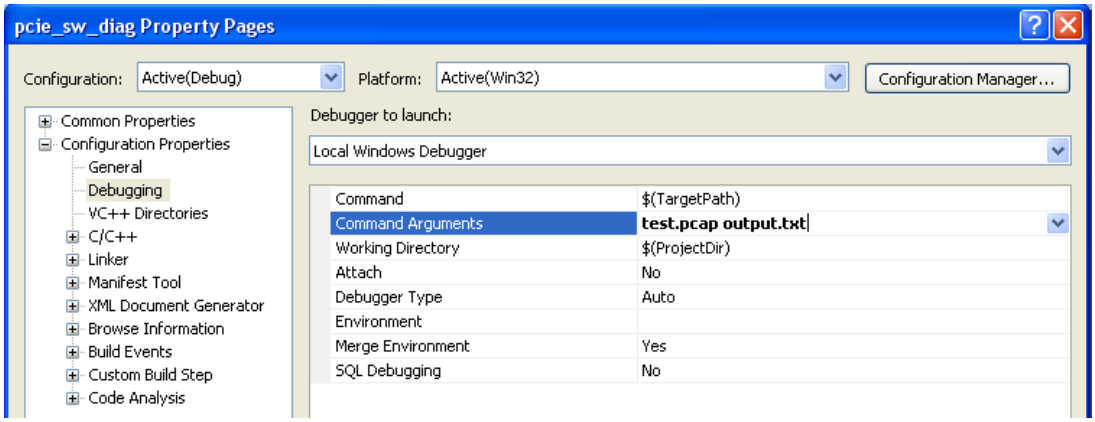
7. Under the Configuration Properties → Linker → General tab, add the WinPcap library path to Additional Library Directories.



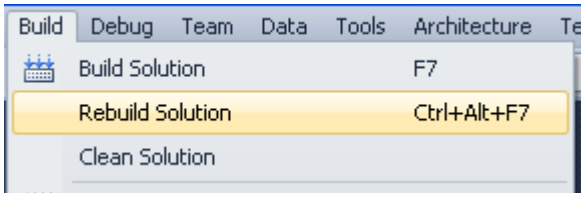
8. Under the Configuration Properties → Linker → Input tab, add the two main WinPcap libraries (wpcap.lib & Packet.lib) to Additional Dependencies.



9. Under the Configuration Properties → Debugging tab, add the files (test.pcap and output.txt) required for running the test.



10. Rebuild the design: In Visual Studio, click Build → Rebuild Solution.



The DE5 NetFPGA packet generator can be tested once the packet generator bit-file has been downloaded into the FPGA by sending sample packets and collecting the packets back in a loopback formation. The user can load a custom PCAP file into the DE5 NetFPGA packet generator (test.pcap) and subsequently transmit the packets in the PCAP file at user defined rates through DE5 NetFPGA ports.

7.2. Test Setup – Packet Generator

1. Install the DE5 board in the PCIe slot and connect the Ethernet cable in loopback formation as shown in Figure 4.
2. Download the bit-file on the DE5 board through the JTAG cable and restart the PC
3. Setup the PCIe software in Visual Studio.
4. Configure the required input parameters (rate, iterations, MAC queue) in the **{project root}\sw\pcie_config\declares.h** file.
5. Rebuild the design

7.3. Running the Test

A pcap file is provided {pcie_config/x86/msdev_2010/test.pcap} for testing. The packet generator is configured in loopback according to Figure 4. The experimental setup is shown in Figure 5.

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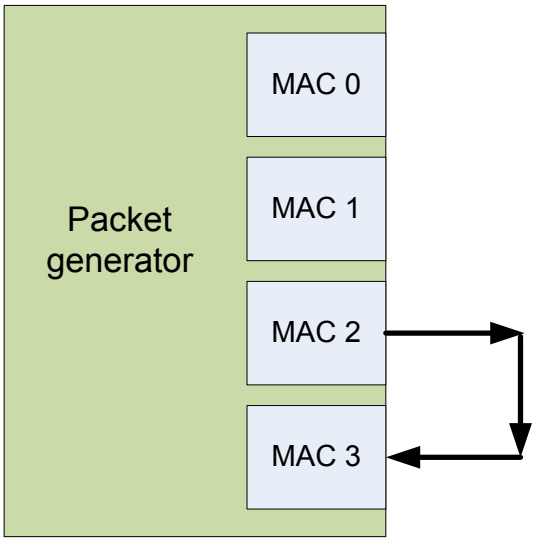

Figure 4: Packet Generator Test Setup

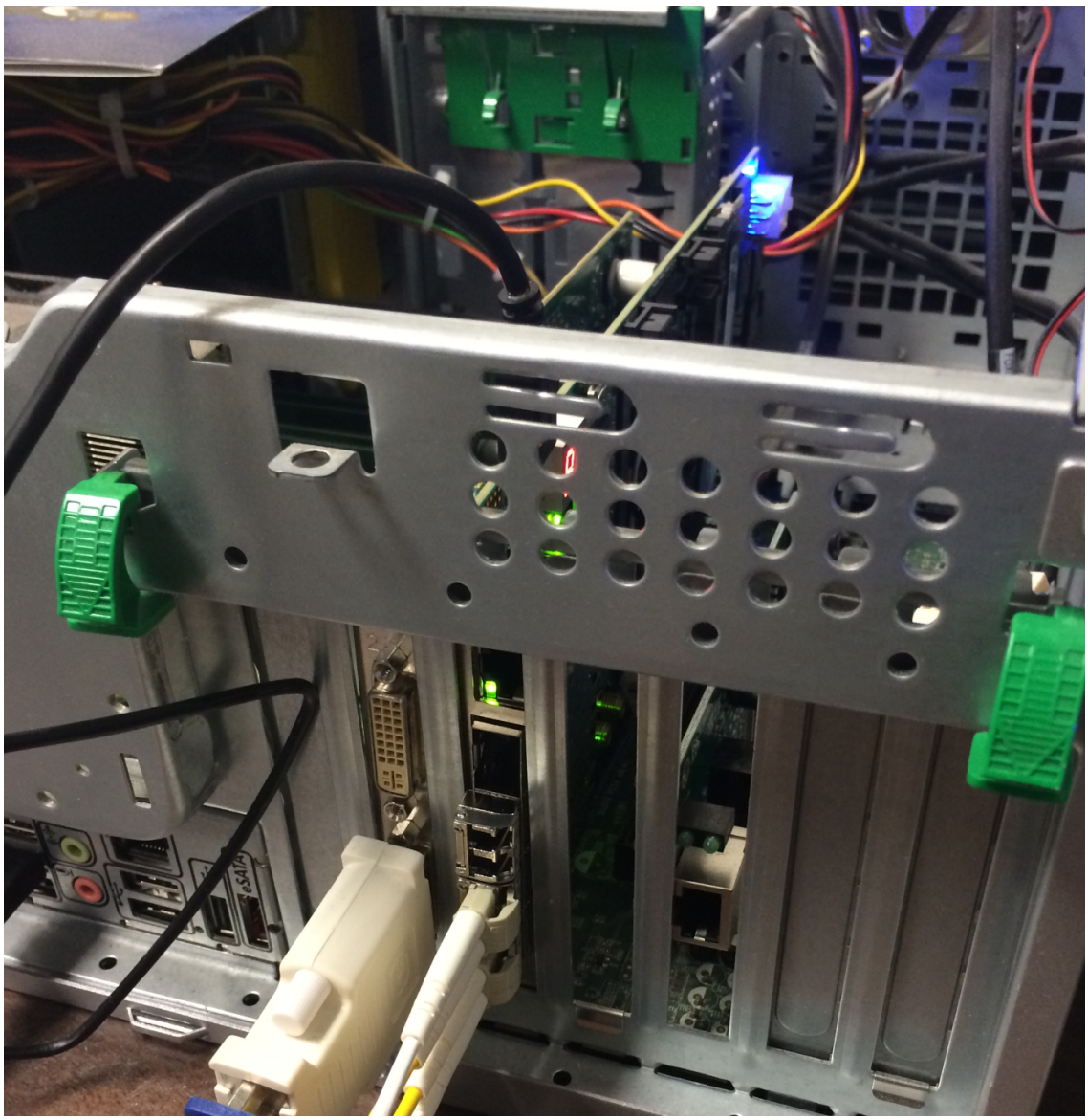

Figure 5: Packet Generator Experimental Setup

Run the packet generator by clicking on Start Debugging in Visual Studio as shown in Figure 6. This command sends packets through the specific Ethernet interface queue **(MAC_ENABLE)** at a user defined rate **(RATE_MAC)** with a user defined delay **(DELAY_MAC)** for a specific number of iterations **(ITER_MAC)**. All the parameters (**MAC_ENABLE, etc**) are defined in the declares.h file.

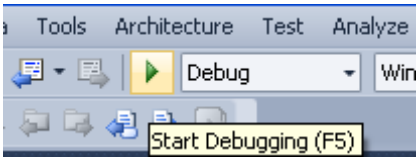

Figure 6: Start Debugging

Example:

To test packet transmission with 32 packets at line rate (1Gbps) through queue 2, use the following input parameters:

define RATE_MAC0 = 0;
define RATE_MAC1 = 0;
define RATE_MAC2 = 1000000;
define RATE_MAC3 = 0;
define ITER_MAC0 = 0;
define ITER_MAC1 = 0;
define ITER_MAC2 = 32;
define ITER_MAC3 = 0;
define MAC_ENABLE = 2;

When the topology as shown in Figure 4 is used, the forwarded packets are captured at queue 3 of the DE5 NetFPGA packet generator. The packet capture statistics is observed in **pcie_config/x86/msdev_2010/output.txt** as shown in Figure 7.

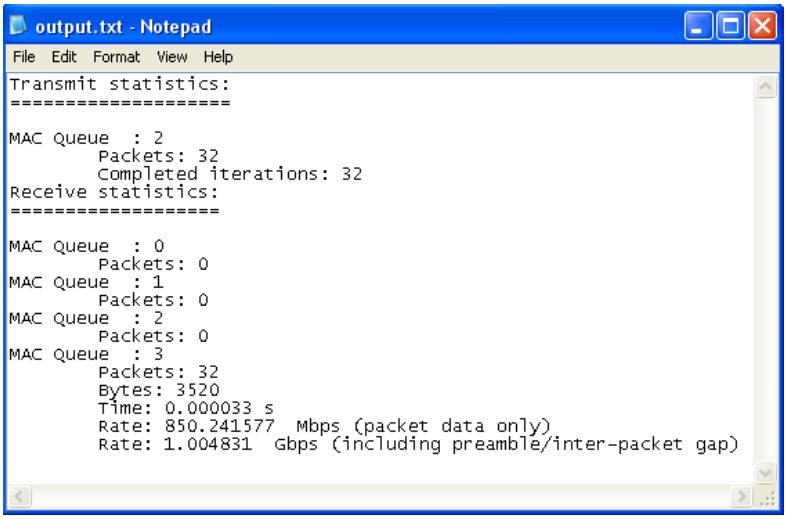

Figure 7: Sample packet capture at line rate (1Gbps)

8. Reference router-Packet generator test setup

The test setup for testing the DE5 NetFPGA reference router-packet generator system is illustrated in Figure 8.

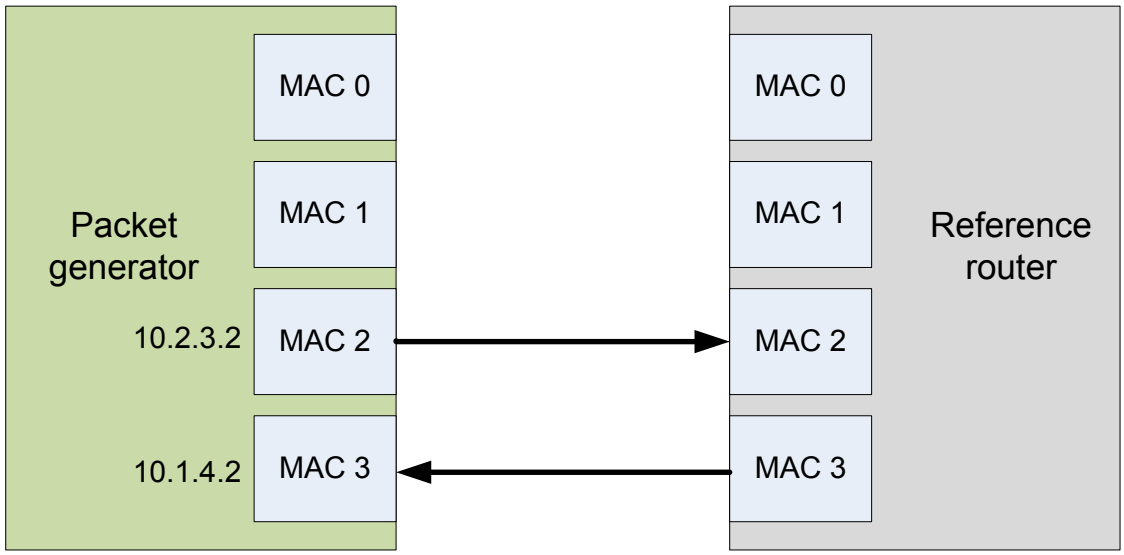

Figure 8: DE5 NetFPGA Reference router-Packet generator setup

The steps for testing the above test topology are explained below.

1. Connect Reference router and Packet generator as per Figure 8
2. Setup the reference router as per DE5 reference router user guide
3. Setup the packet generator
4. Run the PCIe software
5. Observe the output from the **output.txt** file

9. References

[1]. DE5 NetFPGA Project Web, http://www.ecs.umass.edu/ece/tessier/rcg/netfpga-de5/index.html

[2]. NetFPGA Project, http://netfpga.org/

[3]. NetFPGA packet generator http://netfpga.org/foswiki/bin/view/NetFPGA/OneGig/Projects/PacketGenerator

[4]. Altera 10G Ethernet MAC, http://www.altera.com/literature/ug/10Gbps_MAC.pdf.

[5]. Altera PCI Express, http://www.altera.com/literature/ug/ug_pci_express.pdf

[6]. Altera PCI Express Wiki, http://www.alterawiki.com/wiki/PCI_Express_in_Qsys_Example_Designs

[7]. Jungo USB Driver, http://www.jungo.com/st/windriver_windows.html

[8]. Terasic Technologies, http://www.terasic.com.tw/en/

[9]. WinPcap for Windows, http://www.winpcap.org/install/default.htm

[10]. WinPcap Developer Resources, http://www.winpcap.org/devel.htm

[11]. Altera Quartus II 13.1 and Qsys Builder, https://www.altera.com/download/software/quartus-ii-se

[12]. Microsoft Visual Studio 2010, http://www.microsoft.com/visualstudio/en-us/try