Reconfigurable Data Acquisition System for Weather Radar Applications

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Abstract— **Tornado, hazardous weather and flood detection radars demand high-throughput, high-speed data acquisition and processing. Weather-processing systems need to be capable of implementing powerful signal processing algorithms on the raw data collected by the radars. Following processing, data is distributed to the end-user in real-time for timely and accurate detection of imminent weather disasters. Since physical accessibility to such systems is often limited, remote-user based control and reconfiguration of processing capabilities are also essential. A real-time data acquisition, processing and distribution system for weather radar applications that meets these needs is described in this paper. This FPGA-based system has been successfully integrated with a radar optimized for tornado detection and deployed in the field.**

I. Introduction

Data acquisition systems are an integral part of radar applications [1]. A weather radar transmits radio frequency signals and acquires meteorological information based on the echo of such signals from particles in the atmosphere. Data acquisition systems must digitize such backscatter, and perform various processing tasks to cast the raw data into an intelligible and meaningful format. As a result, radar data acquisition systems must meet a series of requirements. Due to the volume of raw data produced by such a radar [1], it cannot be efficiently stored; real time processing is a must. Such operation is especially important for applications such as atmospheric sensing, which is often used for the prediction of tornados and other extreme weather events. The processed data must be made available to the end-user in real time. Since straightforward physical access to such systems may not be feasible, remote dynamic reconfiguration of system computing resources is needed to meet the varying requirements of the user. Additionally, these processes often require numerous control signals and parameters, which necessitates the efficient, reliable implementation of numerous standard communication interfaces.

We present a reconfigurable data acquisition system for weather radar applications. This system uses two Altera Stratix EP1S40 field programmable gate arrays (FPGAs) as its main processing components. System control and interfacing is managed by an on-board ARM microcontroller. The combined use of these components allows for high-speed data processing and dynamic reconfiguration. Radar data is sampled via two analog to digital (A/D) converters. Numerous interfaces including Gigabit Ethernet, IDE, USB, and serial ports provide standard communication ports to the user. A distinguishing feature of our system is its capability for remote FPGA reconfiguration in the field. Upon command of the user, new FPGA configurations can be remotely downloaded to the system via an Ethernet interface. The fine-grained parallelism of the FPGAs allows for real-time radar processing of weather data streams. Processing algorithms may be changed in response to changing weather conditions via remote reconfiguration.

Our architecture meets the requirements of an atmospheric monitoring radar application - the Distributed Collaborative Adaptive Sensing (DCAS) radars [1], being developed at the Engineering Research Center (ERC) for Collaborative Adaptive Sensing of the Atmosphere (CASA) at the University of Massachusetts, Amherst. This radar system is being created to perform timely prediction and detection of tornados, hazardous weather conditions and floods. A complete data acquisition architecture has been implemented using standard off-the-shelf components.

II. Motivation

The DCAS application presents some unique challenges in data acquisition. Previous generations of data collection systems for weather radar applications could be categorized into two groups: those used for high performance research applications, and those intended for large operational weather radars such as NEXRAD [2]. Members of the first family are characterized by high data rates, and a relatively large amount of flexibility for the radar system designer. However, they lack ease of use which leads to high system development costs, and also lack sophisticated reliability features. Systems intended for operational radars are typically bandwidth limited, employ rigid processing schemes, and are highly integrated to allow for simplified inclusion in a weather radar application. In general, this comes at the cost of flexibility and bandwidth. CASA seeks to revolutionize the weather sensing paradigm through DCAS, improving the coverage of the lowest portion of the atmosphere through coordinate scanning of low-power, short range, networked radars [3]. This necessitates the task

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of bringing the benefits of both operational and research data acquisition systems together into one integrated solution.

The system has been designed to use a state-of-the-art intermediate frequency (IF) digitizing receiver. The first generation DCAS radars [1] will employ transmitters whose frequency can drift as a function of temperature, humidity, duty cycle, aging, etc. This necessitates a data acquisition system capable of receiving inputs over a wide frequency range. In addition, future systems will employ frequency agile transmitters with wide bandwidth transmit waveforms, which further emphasizes the need for high bandwidth. Wide dynamic range is also required. As the DCAS radars will be sampling the lowest 3 km of the atmosphere, they will be plagued by echos from non-meteorological targets such as buildings and airplanes. Effective cancellation of these targets depends on a high dynamic range digitizer. As radar systems become increasingly capable of agile and adaptive operation, the requirements on data processing grow accordingly. In addition to traditional algorithms such as software radio, more complex decision based algorithms are becoming candidates for real-time hardware implementation. High resolution data is essential for monitoring micro-scale phenomena such as tornados. As a result, interfaces to enable dissemination of this high rate data are needed.

Reconfigurability is of utmost importance to such a system. "Static" reconfiguration is essential to adapt to changes and updates in the radar hardware. In particular, one salient feature of this data acquisition system is that it enables one to build heterogeneous sensor networks with identical interfaces to the exterior world. Another driving goal is to allow "dynamic" reconfiguration of the system. Many algorithms which one may like to run will be constrained by the computational resources available. The ability to reconfigure the processing hardware to adapt to changing user data needs is present in this design. Processing can also be scene adaptive to employ algorithms appropriate for any given meteorological condition. This type of scene-aware processing also advances the low power goal of CASA; processing hardware can be reconfigured to a low power surveillance mode when the weather conditions are of no interest.

III. Data Acquisition System Architecture

A. Hardware Architecture

Figure 1 gives the data acquisition system architecture. For clarity, only major components are shown. Two Altera Stratix EP1S40 FPGAs [4] form the main processing modules of this architecture. These parts each contain 41,250 logic elements, abundant internal memory (over 3 Mbits), and dedicated multiplier circuitry. These FPGAs are controlled and supervised by an Atmel AT91RM9200 microcontroller [5].

The data acquisition system receives the radar echo via a dual channel, high performance IF sampling receiver. As shown in Figure 1, the A/D channels each contain an Analog Devices AD6645 converter [6], which supports 14 bit, 105 MSPS sampling with a -3 dB input bandwidth of 5 to 270 MHz. Two parallel channels are included to simultaneously

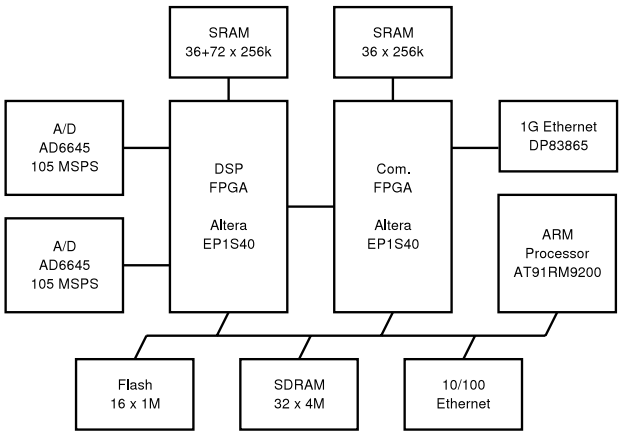

Fig. 1. Block Diagram of Data Acquisition System

sample both the horizontally and vertically polarized (H and V) components of the backscattered signal. Sampling is synchronous to a phase reference provided by the radar system. PLLs resident on the FPGA allow the sampling clock to be generated from any given frequency reference (up to 500 MHz); alternately, one may provide the sampling clock directly through a low phase noise clocking path to the digitizers. This configuration allows us to have a maximum range resolution of 3 meters. Several features have been incorporated to ensure a high degree of noise immunity, both from the digital sections of the board and from external sources. These include isolation of the analog and digital ground planes with differential transmitter-receiver pairs at the plane boundaries. The analog sections are powered by a dual-stage power supply which consists of a shared switching regulator, and separate linear regulators for each of the A/Ds. The sensitive analog components are also protected from radiated noise through several board-level shielded enclosures.

The two FPGAs are organized logically in accordance to their functionality. One FPGA is responsible for digital signal processing, while the other manages data distribution. Once digitized, the data is ingested by the DSP FPGA. To facilitate processing, the DSP FPGA is equipped with two SRAM banks. The first of these is a 36 bit x 256k device intended for function lookup. The second is a wider, 72 bit, bus of the same depth which serves as scratch space for memory intensive processing. Both banks can perform interleaved read and write operations at 250 MHz. Processed data is transported from the DSP FPGA to the communications FPGA (Com. FPGA) by means of a 124 bit bus, capable of 250 MHz operation. The Com. FPGA is also fitted with a similar, but smaller complement of SRAM (36 bit x 256k), to be used primarily for data buffering. Further processing may also be performed in this device. A Gigabit Ethernet interface is implemented through the inclusion of a National Semi. DP83865 physical layer device by which data products are transfered to the user.

The Atmel ARM-based AT91RM9200 microcontroller acts as the master control for the system. This microcontroller is a

complete system-on-chip built around the 32-bit ARM920T ARM processor that can operate at a maximum speed of 209 MHz (200 MIPS at 180 MHz). It has a built-in 10/100 Mbps Ethernet media access controller. It also supports a variety of other standard communication interfaces such as a serial interface, a dedicated Universal Asynchronous Serial Transmission (UART) debug channel and a Universal Serial Bus (USB) interface, in addition to a standard JTAG (Joint Test Action Group) port.

In addition to the main system components shown in Figure 1, several other features have been implemented for flexibility and scalability. There are numerous uncommitted digital I/Os, which include buffering and ESD protection, on each FPGA and also the microcontroller. These may be used for synchronization with the radar system or peripheral expansion. The Com. FPGA also has an ATAPI/IDE interface intended to buffer and back up collected data in the event of network outage or congestion. Four additional low speed (200 KSPS), high resolution (16 bit) A/D channels are provided to accept auxiliary meta-data. The FPGAs are programmed through the use of an Altera EPM7128AE PLD. This device sits on the microcontroller bus and allows one to load FPGA configuration files from any location accessible to the microcontroller, including any network location.

B. On-board Software

FPGAs have been shown to be highly effective in performing time varying tasks such as data compression, digital signal processing and communication related operations [7]. The DSP FPGA is configured to perform the specialized software radio functions needed for weather radar processing. A programmable digital oscillator is generated to mix the received echo to baseband. Filtering is performed in two stages: a coarse, multiplier-free CIC (Cascaded Integrator-Comb) followed by a polyphase decimation FIR with fully programmable taps. Transmitter phase is measured, and subtracted from each sample. Correlations may be calculated to extract relevant weather data such as reflectivity and velocity measurements.

The Communications FPGA embeds a Gigabit Ethernet core which performs all Internet Protocol layers from the application layer down to media access control. A transport protocol based on UDP is employed for data transfer. In the event of network unavailability, the IDE interfaces can be used for temporary data backup.

For ease of programming and controlling the microcontroller and hence the entire data acquisition system, a Linux kernel, version 2.4.19, has been ported to the microcontroller. This allows for the efficient leveraging of open-source software and utilities such as secure shell, network time protocol, etc. In our configuration, the root file system of this microcontroller is mounted via network file system (NFS) resident at a remote location. This gives the user great flexibility in controlling microcontroller operation; software upgrades do not require any changes to the firmware resident on the board. An additional function of the microcontroller software is to control the configuration process of the two FPGAs. Upgrade of the FPGA firmware is as simple as replacing the configuration files on the remote NFS server.

IV. RESULTS

The system described has been fabricated and deployed in an operational weather radar system [1]. Certain parameters of the data acquisition subsystem have great impact on the performance of weather observation. Of particular interest is dynamic range; although precipitation displays a dynamic range of 50 to 60 dB variation in backscattered power, unwanted reflections from stationary objects, commonly referred to as "ground clutter", can mask useful weather echos. Such objects can be easily filtered from the useful weather data if they do not saturate the receiver. Traditionally, the data acquisition system has always been the limiting factor in this figure of merit. Figure 2 shows the dynamic range of the fabricated system when implementing a 3.5 MHz (24 meter) wide filter. Note that our front end exhibits a dynamic range of 102 dB. This represents an improvement of 11.97 dB over an industry standard product [8]. Figure 3 shows that the receiver enjoys a signal to noise ratio of 74.5 dB and a spurious free dynamic range (SFDR) of 88 dB.

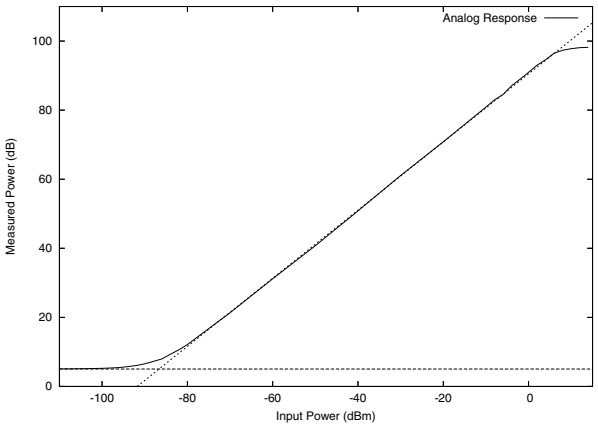

Fig. 2. Analog front end dynamic range calibration plot

The board is currently employed in a high performance digital receiver mode. We first down-convert the radar return to baseband, adjusting for transmitter frequency and phase drift. Filtering to match the receiver bandwidth to that of the transmitted pulse and various meta-data tagging functions are then performed. This high-rate data is then transfered to a host server on which downstream meteorological algorithms can be quickly prototyped and later migrated into the real-time hardware system.

The abundant memory resources enable us to implement a very high performance numerically controlled oscillator (NCO) needed to mix the incoming signal down to baseband. The spurious free dynamic range performance of an NCO is typically limited by the amount of high-speed memory available for lookup of trigonometric functions. We are able

to implement this oscillator with 1.457 nano-Hertz tuning resolution, and a worst-case SFDR better than 120 dB.

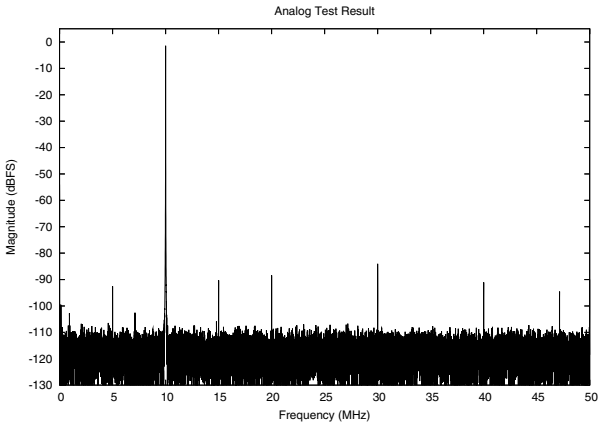

Fig. 3. Analog front end single tone response

The FPGA processing hardware enables us to compute at a rate of 28.0 18x18 GMACS (Giga-multiply accumulates per second). This allows us to compute a pair of FIRs of 8000 taps each with 1 MHz output bandwidth. The large number of taps allows the filter designer great freedom in balancing mismatch loss, out of band rejection, range smearing and sidelobe levels. Future systems employing wider bandwidth pulse compression techniques [9] will be easily accommodated. All processing firmware has been shown to run at speeds of over 220 MHz.

The Gigabit Ethernet interface allows us to transfer data at speeds equivalent to a 33 MHz/32 bit PCI interface, while retaining the autonomy of the board. Testing has confirmed that we can sustain data rates of 88.3 MBytes/s, with peak rates around 10 MBytes/s higher. This allows for the transfer of processed data at 11 MHz bandwidth per channel without limiting the data acquisition duty cycle.

The complete radar system has been tested and calibrated at Colorado State University's CHILL radar facility [10]. Several weather data sets have been collected by this data acquisition system and carefully examined against the well-characterized CHILL weather radar. For example, Figure 4 shows received power in a vertical cross section of a winter snow event. The results from this deployment confirm that the performance goals for this design have been attained.

A. Remote-User based, Dynamic Reconfiguration of the FPGAs

The flash chips (Figure 1) can store different FPGA configuration files each implementing different signal processing algorithms or different parameters (range modes, pulse repetition frequencies etc.). A remote user, via the microcontroller Ethernet interface, can select from these configuration files and load it into the appropriate FPGA, providing us with the option of *dynamic reconfiguration* of the system.

Further, as the file-system of the microcontroller operating system is run on a remote host PC and accessed by the microcontroller via its Ethernet interface, the configuration

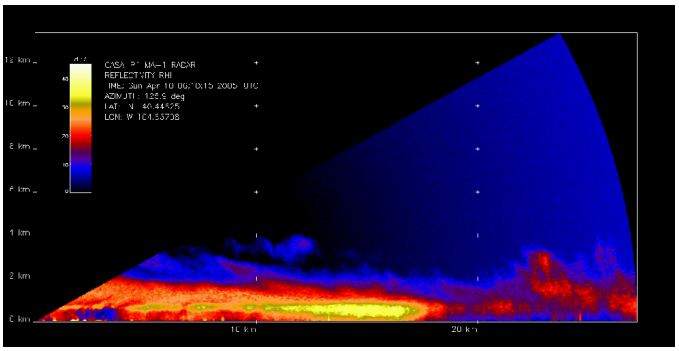

Fig. 4. Radar reflectivity image of winter storm in Colorado

files for the FPGAs too can be stored or generated as and when required on this remote host PC and downloaded into the FPGAs (via the PLD) to reconfigure them. Thus, this configuration scheme has the added benefit of *remote-user based dynamic reconfiguration* of the system.

V. Summary

This research project has developed a single-card reconfigurable data acquisition architecture for DCAS, a hazardous weather prediction radar system. The presence of high-density, high-performance FPGAs as processing elements, a microcontroller acting as the master control, and a variety of contemporary high-speed communication interfaces facilitate real-time acquisition, processing and distribution of radar data. Essential features such as remote-host based control and reconfiguration of the system has been successfully implemented.

The design, layout, manufacturing and testing process of this hardware has been completed and the system has been integrated with the DCAS radars and field-tested as a complete weather monitoring system.

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