Acquisition of Sensing Data on a Reconfigurable Platform

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Abstract:

Recent developments in wireless networking and re-configurable computing are making real-time processing of remotely sensed data and real-time information dissemination feasible. In this paper we describe the development of a single card re-configurable hardware system that allows for both real-time acquisition and processing of radar polarimetric data. The proposed approach was developed after examining the architecture and implementation of several current data acquisition systems. Upon project completion it will be possible to support the acquisition, processing, bulk hard-disk data storage and Ethernet transfer of radar polarimetric data. This work will be particularly useful in supporting real-time operation due to speed improvements gained from reconfigurable devices.

I. Introduction

The development of networked remote sensing instruments [1] has been limited by the lack of digital components that can handle large quantities of data in real-time. These needs can now be met through the development of a small form-factor board built from contemporary, off-the-shelf components such as a StrongARM [4] processor and field-programmable gate arrays. The on-board availability of reconfigurable digital components allows for system flexibility and improved sampling rates.

II. Background

For our system, we envision the collection of data across three spatial dimensions and numerous points in time, leading to significant demands in computation, communication and data storage. The design of the system has been driven by sensor sampling requirements and a desire to interface to off-the-shelf communication protocols. Current specifications indicate a need to support a sampling range of 7.5m requiring 20MHz of sampling bandwidth. To support Nyquist sampling rates with appropriate consideration for sampling error, an analog to digital conversion rate of 80MHz is required. Since higher sampling rates will likely be needed in the future, the architecture has been designed to support more advanced A/D technology as it becomes available.

III. Proposed System

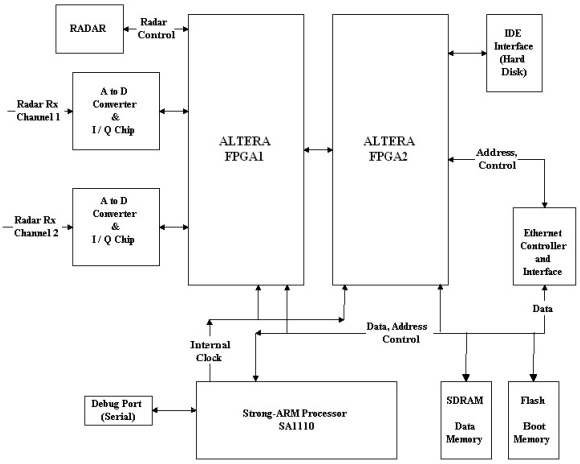

Figure 1: System Architecture

A candidate design concept for our proposed system has been developed and is shown in Figure 1. The electronic subsystem is based on a small form factor (8 inches x 8 inches) single-board computer that acquires and processes radar polarimetric data. The system has two A/D channels each of which can sample data at 80MSPS (10 bit samples). Two dedicated digital tuner chips [7] perform I/Q processing on this data to bandlimit the data to 40MSPS and generate in-phase and quadrature components of the data.

The processing core of this system is a StrongARM (SA1110) Processor [4]. This recently introduced 200MHz processor is ideally suited for real-time embedded applications. Existing software can be used with this architecture that not only supports data processing of information gathered from the surrounding environment, but also supports necessary networking tasks needed for communication with external Internet channels. Flash and SDRAM memory modules act as program and data memory respectively for the StrongARM. The

processing power of the StrongARM is supplemented by two Altera Apex20K200E FPGA's [5]. Programmable logic devices such as these have been shown to be highly effective at time-varying computational tasks such as data compression, pattern matching and communications encoding & decoding [2]. Since the FPGA is closely coupled with the StrongARM, high communication bandwidths can be achieved.

The data acquisition system has been augmented with a host of dedicated data interfaces to allow for fast data transfer. A high-speed IDE interface is used to provide for fast data transfer between the single-board system and a disk array. A dedicated Fast Ethernet interface is provided for high-speed Internet access.

IV. Ongoing Work

The complete architecture and the interface specifications have been defined for the system. Logic implementation for FPGA1 & 2 shown in Figure1 is presently underway. The basic logic blocks that have been implemented in the FPGA's are shown in Figure 2.

FPGA1 controls the radar and its timing and acquires analog radar data through two analog channels. The FPGA1 then performs correlation [3] on the radar data over a set of samples defined by the StrongARM. FPGA1 also implements a FIFO memory to store the processed radar samples.

The StrongARM processor can perform processing on the radar data by reading the data from the FIFO. After processing, it can transfer the data to the IDE or Ethernet interface via FPGA2. The processor can also control FPGA2 to directly transfer the data from the FIFO to the external interfaces. Finally the StrongARM can download data from the Ethernet interface and decode the data to control the radar through FPGA1.

FPGA2 implements the Ethernet controller and the IDE controller. It also implements the FIFO control logic to read data from FPGA1. FPGA2 performs data transfer from the FIFO or the StrongARM processor to the Ethernet interface and the hard disks.

The Ethernet controller used in the system can support fast Ethernet transfer of up to 100Mbps. The IDE interface chosen is the ATA-3 [6] standard, which can support two hard disks, and maximum data transfer rate of up to 16.67MBps.

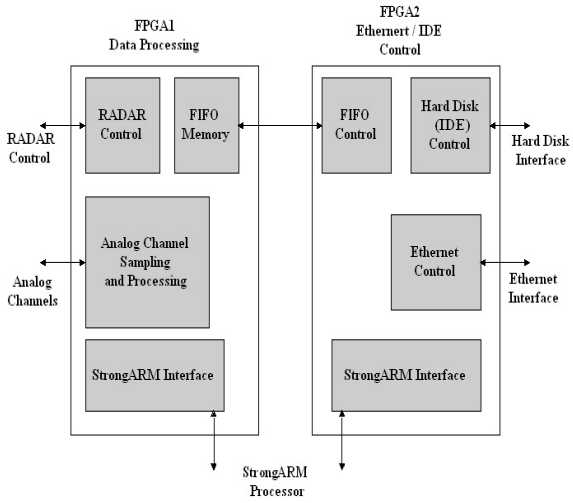

Figure 2 : Internal Blocks - FPGA's 1 & 2

V. Conclusion

In this paper, a new digital receiver/processor for high bandwidth radar applications has been described. This single-board system meets current data sampling rates through the use of two dedicated A/D channels. Advanced processing capabilities in the form of off-the-shelf processors and FPGA's form the core of the system. Processed data can be transferred to either bulk storage (hard disk) or to the Ethernet. Through the development of this system, the goal of networked data acquisition for radar polarimetry will be achieved.

VI. References

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