A Hybrid Adiabatic Content Addressable Memory for Ultra Low-Power Applications

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ABSTRACT

This paper presents a hybrid adiabatic content addressable memory (CAM). The CAM uses an adiabatic switching technique to reduce the energy consumption in the match line while keeping the performance for the read/write operation. The adiabatic CAM is suitable for ultra low-power, low performance applications such as smart cards and portable devices. This CAM uses a clocked power supply for the match line while the rest of the circuit is the same as the basic CAM. A novel smart card application which uses the adiabatic CAM is illustrated. The circuit simulations for a 16x16 and 32x32 CAM were done in Hspice using 0.18 μm Berkeley models and the energy dissipation was compared with a basic CAM. The results show three orders of magnitude in energy savings for the 16x16 CAM and one order of magnitude savings for the 32x32 CAM when operated at 2Mhz. The maximum frequency of operation for which there was considerable energy savings was found to be 200 Mhz with a 20% and 45% energy savings for 16x16 and 32x32 CAM respectively.

Categories and Subject Descriptors

B.3.2 [**Memory Structures**]: Design Styles—*Associative memories*

General Terms

Design, Performance

Keywords

Ultra-low power, Energy recovery, adiabatic switching

1. INTRODUCTION

Content Addressable Memories (CAM) are gaining increased importance due to their parallel pattern matching property. This property makes them useful in applications such as networking where a quick search is needed in routing tables [1], and in caches for fast tag comparisons [4]. The CAM structure is similar to that of the normal RAM but has additional circuitry for its compare operation. The challenge in this design is to reduce the power consumption in the compare circuitry. The compare operations are always active and are a major source of power dissipation. Most of the power that is dissipated is due to switching in the match line. Therefore, one of the most common techniques to reduce the power dissipation is to reduce this switching. Several ways to achieve this reduction include selective precharging of the match line, shutting off power to unwanted blocks and to alternate between active high and active low for the match line [13, 6, 5]. This paper addresses the application of CAM in ultra low-power and low-performance applications such as smart cards and handheld devices.

The energy dissipation in a circuit is due to the charging and discharging of its node capacitance. The charging and discharging paths are different, causing energy to be dissipated in the form of heat. An adiabatic switching technique reduces the energy dissipation in circuits by recycling the charge stored in the capacitance. This recycling is achieved by using an AC power source instead of the traditional DC source. The energy dissipation is reduced by maintaining a very low potential difference across the capacitance.

New and different logic styles have been proposed using adiabatic principles [11, 9]. Latches, shift registers, multipliers and memories have been proposed and implemented [3, 12, 11, 9, 10]. The designs have shown significant power savings when compared to the conventional CMOS circuits.

In this paper, the adiabatic switching principle is applied to a CAM to reduce the energy dissipated in the match line. This reduction is possible by using an AC power source for the compare circuitry, thereby providing the same charging and discharging path for the match line. Since the charging and discharging happens in the same cycle, there is no need to pre-charge the match line. The CAM cell structure is not altered, thereby requiring no area overhead. Also, switching the power supply from AC to DC causes the adiabatic CAM to act as a basic CAM when high performance is needed.

The second section of this paper describes the previous work done to reduce the power dissipation in CAM(s) and also explains the adiabatic switching principle. The third section provides the motivation for the work and illustrates an application for the adiabatic CAM. The function of the adiabatic CAM and the simulation results are presented in the fourth section. The conclusion is presented in the fifth section along with the future work.

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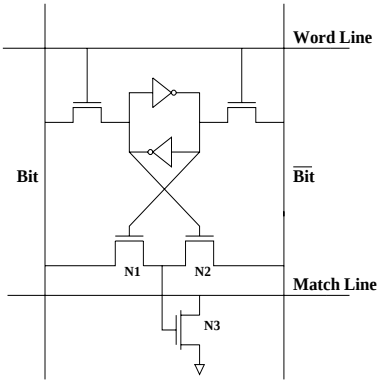

Figure 1: Schematic of a basic CAM Cell

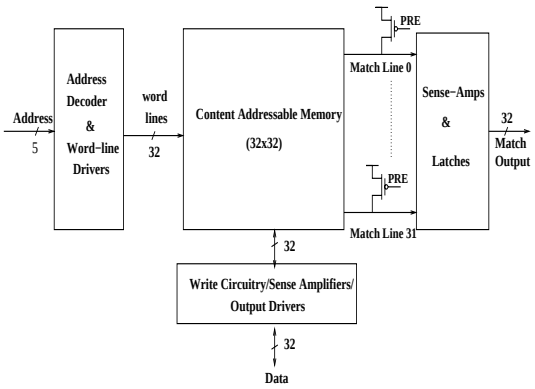

Figure 2: Structure of a 32x32 basic CAM System

2. BACKGROUND

The CAM structure is similar to that of the conventional SRAM cell but has three additional transistors (N1,N2 and N3) for the compare circuitry. Figure 1 [8] shows the schematic of a basic CAM cell and Figure 2 shows the structure of a 32x32 CAM along with the peripheral circuitry. The match lines are precharged before the evaluation phase. However, the bit lines cannot be precharged as it would cause the comparison circuitry to be ON when the match lines are being precharged. Bit-line precharging would provide a path between the match line and ground causing short circuit current to flow. The bit lines are therefore pre-discharged to avoid the path between the match line and ground. The search data is loaded on the bit lines of the cell and compared with the contents of the cell. At any point of time, either N1 or N2 is ON. When a mismatch occurs, transistor N3 is ON and the match line is pulled low. During a match condition, the transistor N3 is OFF and the match line is held high. Power dissipation in a CAM is due to the swing in the bit-lines and the match line. Half of the bit-lines swing due to the search data while the match lines swing for a mismatch. For wide memories, the matchline capacitance is larger than the bit-line capacitance and therefore the power dissipated in the match line is significant. Several techniques are employed to reduce the switching in the match line.

The Toggling CAM proposed in [5] involves alternating the match line output between active high and active low for every access. As only a few words match the search data, most of the match lines are pulled low. Therefore, by alternating between an active high and active low output, the switching in the match line is reduced by fifty percent. The transistor N3 of the basic CAM is connected to a signal AHAL (Active High Active Low) instead of ground. The disadvantage of this technique is that the signal AHAL also switches, causing power dissipation. The maximum power savings is around 50 %.

Power reduction can also be achieved by shutting off the comparison circuitry when it is not in use [6]. This technique is applicable in memories that have multiple banks, where only one bank is accessed and the other banks are switched off. However, inside the bank the parallel comparison has to be done, thereby, requiring the comparison circuitry.

Another method for reducing the power dissipation is to use selective precharging [13]. In this technique, a selected number of bits are taken out of the CAM and if they match with the search data, then only a precharge is done. This reduces the switching in the match line considerably. The key issue here is the number of bits that are taken out of the CAM. The selective precharge technique depends upon the input data. There is a delay associated with the compare circuitry outside the CAM which is used to precharge the match line.

The above approaches are designed to reduce the power in high performance applications. However, for low-performance applications, significant reduction in power can be obtained by using the adiabatic switching principle[12]. The energy dissipation in conventional CMOS circuits is caused by the channel resistance of the transistor. The dissipation through the channel resistance R is then:

$$E_{diss} = P \cdot T = I^2 \cdot R \cdot T = \left(\frac{C_L V_{dd}}{T}\right)^2 \cdot R \cdot T = \left(\frac{RC_L}{T}\right) \cdot C_L V_{dd}^2 \quad (1)$$

From Equation (1) it can be deduced that one way to reduce the energy dissipation is by increasing the switching time to a large value. This approach is adiabatic switching. However, as the switching time decreases, the energy savings is reduced. In adiabatic switching an AC source is used to maintain low voltage drop at circuit nodes at all times thereby dissipating almost zero energy. The AC power supply transitions slowly which helps to reduce the energy dissipation. The adiabatic principle has been applied to memories and considerable energy savings have been achieved [10]. However, most of the previous work has focussed on SRAMs rather than content addressable memories.

3. MOTIVATION

The role of static power dissipation, primarily in the form of leakage power, is increasing as CMOS technologies scale. Therefore, one way to reduce power dissipation is by shutting off the power supply to the circuits that are not needed[7]. However, there must be an active circuit in the system that activates the circuits that are needed and puts the unwanted parts of the system into sleep mode. These circuits must dissipate minimum power. An adiabatic content addressable memory is a good choice for such a circuit. The contents of the memory describe the parts of the system which are to be put into sleep mode or that is to be woken up. The performance of such a memory is not critical and can be

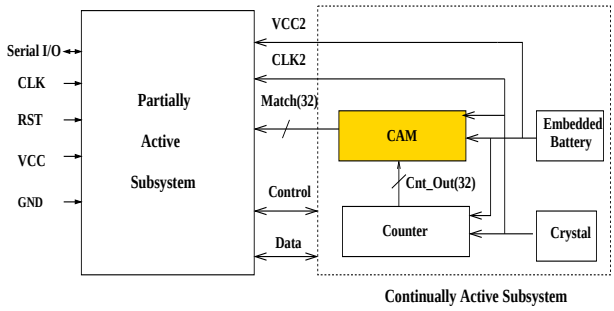

Figure 3: An active smart card system

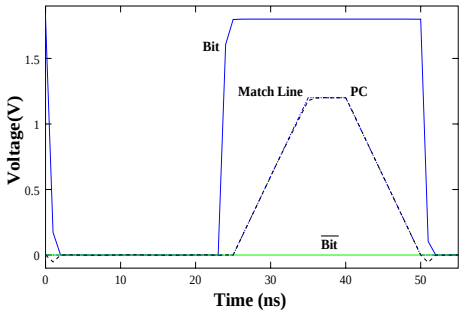

Figure 4: Waveforms for the adiabatic CAM

exploited to tradeoff performance for power.

One application that can make full use of the CAM's quick search capability and small energy dissipation is an "active smart card" that has an embedded battery. To provide for a wider array of applications, such as the readerless update of a cryptographic key, the computational ability of a microcontroller is needed during times when the card is not connected to the card reader, thus necessitating an on-card power supply.

The energy-aware smart card architecture uses a combination of low-power techniques and selective module activation to facilitate longer battery life. The architecture is composed of a Continually Active Subsystem (CAS) and a Partially Active Subsystem (PAS), and is represented as a block diagram in Figure 3. The CAS consists of only a small fraction of the entire circuit and houses only the components that need to be active at all times like the adiabatic CAM and the counter. The PAS will be activated only when required by the CAS or when the card is connected to a reader, and consists of the microcontroller (MCU), a secure interface, and a main interface(not shown in figure). A crystal, providing a clock in the order of 3 MHz, and an embedded battery are also present in the CAS. When the smart card is communicating with a card reader, the embedded battery will be disabled and the reader will power the entire system. The power and clocking also drive the PAS when it is stimulated by the CAS.

The energy consumption of the whole smart card (E_{card}) can be written as a function of the power dissipated by the CAS and the PAS, and the amount of time they are active:

$$E_{card} = P_{CAS} \times T_{CAS} + P_{PAS} \times T_{PAS} \quad (2)$$

where P_{CAS} and P_{PAS} represent the power consumption of the CAS and the PAS, and T_{CAS} and T_{PAS} represent the amount of time each of these two modules are active. The goal of the power-aware architecture is to reduce E_{card} and preserve the finite energy contained in the embedded battery.

P_{CAS} is thus the most critical factor with respect to the lifetime of the battery. In order to minimize the CAS power consumption and extend the overall system life, an ultra low-power adiabatic CAM is implemented. The energy-aware smart card application provides a motivation for the hybrid adiabatic CAM where read/write can occur at a high speed and the associative computing occurs at a very low speed, saving energy while it is away from the reader.

4. ADIABATIC CAM

4.1 Schematic and Working

The structure of the adiabatic CAM cell is same as in Figure 1 except that the transistor N3 is connected to a clocked power supply (PC) instead of ground. The power clock causes adiabatic transitions in the match line thereby saving considerable energy.

The waveform for the adiabatic CAM under the mismatch condition is shown in Figure 4. The bit lines are pre-discharged and the search data is loaded onto the bit lines. The match line is pre-discharged initially. When a mismatch occurs, the transistor N3 is ON and the match line follows PC, thereby maintaining a very low potential drop across the match line capacitance. The swing in the match line is maintained to a value of one threshold voltage less than the full rail, to decrease the charge loss that would arise across the transistor N3. The charging and discharging path are the same for the match line and the charge stored is recovered in the same clock cycle. The match line is therefore held low after the evaluation phase, because the energy is recovered by ramping down the power clock.

When a match condition occurs the transistor N3 is OFF leaving the match line in a low state. This state causes no energy dissipation. For both conditions the energy dissipated is minimal and substantial energy savings are obtained. The output of this CAM is adiabatic and is valid when the power-clock is high. Energy recovery latches in [3] could be used to obtain further energy savings.

4.2 Experimental Set up and Results

The spice simulations for the memory were performed on 0.18μm technology with a Vdd of 1.8V. Interconnects were modeled as a distributed RC network using the Berkeley Predictive Model [2]. Spice simulations were performed for two different CAM sizes - 16x16 and 32x32. The worst case scenario considered in the simulations was the contingency in which none of the data stored in the CAM matches the search data. A trapezoidal power clock was used for the adiabatic CAM. The energy dissipation in the match line was measured for different frequencies for both the adiabatic and basic CAM.

The results obtained were compared with the basic CAM. Figure 5 shows the energy dissipation at different frequencies in the match lines for a 16x16 adiabatic CAM and basic CAM. Figure 6 shows the energy dissipation in the match lines for a 32x32 CAM.

The results show three orders of magnitude in energy sav-

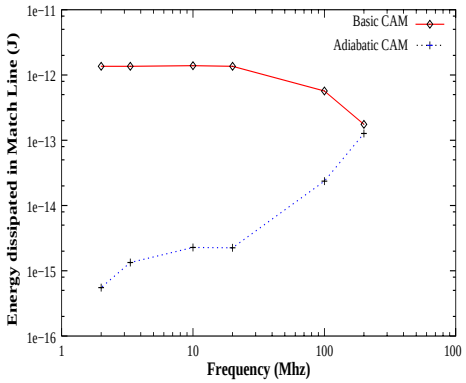

Figure 5: Energy dissipation in match line for 16x16 CAM

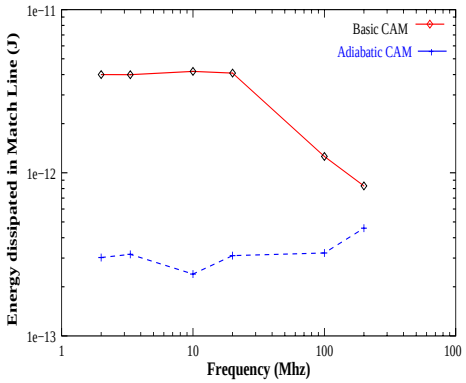

Figure 6: Energy dissipation in match line for 32x32 CAM

ings at a frequency of 2 Mhz for a 16x16 CAM and one order of magnitude for 32x32 CAM when compared to the basic CAM of the same size. However, as the frequency increases, the energy dissipation also increases for the adiabatic CAM. The energy savings for the 16x16 adiabatic CAM is around 20% and 45% for the 32x32 CAM when compared to the basic CAM at an operating frequency of 200 Mhz.

5. CONCLUSION

In this paper, a content addressable memory which uses the adiabatic switching principle to reduce the energy dissipation in the match line was presented. The CAM provides significant energy savings at operating frequencies on the order of few Mhz. It has been shown that this CAM is suitable for an active smart card architecture which has an operating frequency in the order of 3Mhz. Simulation results show three orders of magnitude energy savings for a 16x16 CAM and one order of energy savings for 32x32 CAM operating at 2 Mhz. It is shown that as the size of the CAM increases, the energy savings are reduced due to the increase in match line capacitance. A possible approach to reduce the energy dissipation in wider memories would be to decompose them into smaller memories and then apply the adiabatic techniques to the smaller modules and the interface between the modules. The impact of the leakage current on the adiabatic CAM needs to be investigated for future technologies.

6. ACKNOWLEDGMENTS

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