

Homework # 3

Due: October 26

Multi-FPGA Systems and Coarse-Grained FPGAs

In this assignment you will have an opportunity to provide brief summaries of important topics regarding multi-FPGA systems and coarse-grained FPGAs.

Ex 1: Rent's Rule

Please read pages 416-421 in [2] and Section 4.2 in [1]. Based on the references, summarize, in your own words, the Rent's Rule equation, its parameters and its implications from a system standpoint. Your description should include a discussion of approaches to overcome pin limitations. What types of circuits are most susceptible to Rent limitations? Is this problem likely to get better or worse as devices scale? Include in your discussion values taken from Table 9.5 in [2] and Figure 9 in [1] to support your arguments. Please limit your discussion to one page at most.

Ex 2: Virtual Wires

Please read the remainder of [1] and summarize the basics of the virtual wires approach. How does this emulation system differ from existing systems? This discussion should cover the following areas: new software steps added to support virtual wires, impact on multi-FPGA partitioning, description of phase-based scheduling, and summary of results reported in the paper. Please limit your discussion to one page at most.

Ex 3: Transmogripher-4 versus BEE-2

Please read [3] and look over [5]. In less than a page, contrast the hardware architectures and programming environments of these systems. How are they similar? How do they differ? You may wish to summarize your results in a table.

Ex 4: Matrix

Please read [4]. In less than a page, comment on the architecture and its target application space. Include a brief summary of the paper. What are some of the shortcomings of the architecture?

References

- [1] J. Babb, R. Tessier, and A. Agarwal. Virtual Wires: Overcoming Pin Limitations in FPGA-based Logic Emulators. In *Proceedings, IEEE Workshop on FPGA-based Custom Computing Machines*, Napa, Ca, Apr. 1993.
- [2] H. B. Bakoglu. *Circuits, Interconnections, and Packaging for VLSI*. Addison Wesley, Reading, Ma, 1990.

- [3] C. Chang, J. Wawrzynek, and R. Broderson. BEE2: A high-end reconfigurable computing system. *IEEE Design and Test of Computers*, Apr. 2005.
- [4] E. Mirsky and A. DeHon. Matrix: A Reconfigurable Architecture with Configurable Instruction Distribution and Deployable Resources. In *Proceedings, IEEE Workshop on FPGA-based Custom Computing Machines*, Napa, Ca, Apr. 1996.
- [5] University of Toronto. *The Transmogripher-4 Project*, 2005. <http://www.eecg.toronto.edu/~tm4/>.