

Parameter	Meaning
B	Total bits
N	Number of arrays
W_{eff}	Set of allowable effective data widths of each array
M	Number of pins in each memory block
G	Number of logic blocks
W	Parallel tracks per logic routing channel
F_m	Number of tracks to which each memory block pin can connect
F_c	Number of tracks to which each logic block pin can connect
F_s	Number of choices offered to each incident track by a switch block
V	Vertical tracks between each memory array
R	Logic blocks per memory block in the horizontal dimension

Table 6.1: Architectural parameters for embedded memory resources.

6.1.2 Logic Resources

The logic resources of the FPGA are assumed to consist of five-input lookup tables interconnected using horizontal and vertical channels, similar to the Xilinx 4000 FPGA, the Lucent Technologies ORCA FPGA, and the architecture studied in [37].

Of particular interest is the switch block that is found at the intersection of each horizontal and vertical channel. Figures 6.3(a) and 6.3(b) show two switch blocks used in previous work; in both, each incoming wire is offered three possible connections (denoted by $F_s = 3$ in [37]). Each dotted line represents one of these connections.

Neither of these switch blocks works well with the limited memory/logic interconnect that will be described in the next subsection. As will be shown, an inflexible memory/logic interconnect structure will often make it necessary to route a net to a specific track within a channel. Figure 6.4 illustrates the problem. Consider the implementation of a portion of

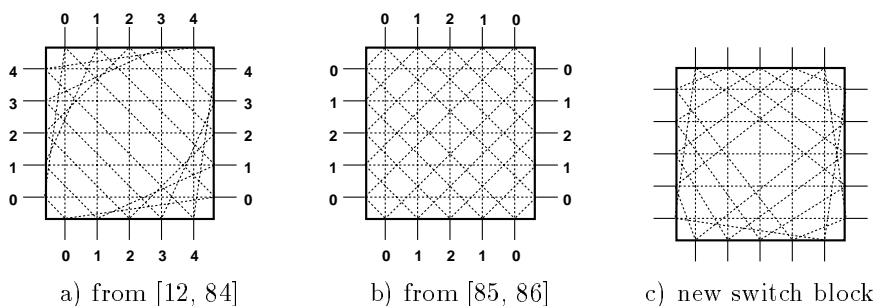


Figure 6.3: Three different switch blocks.

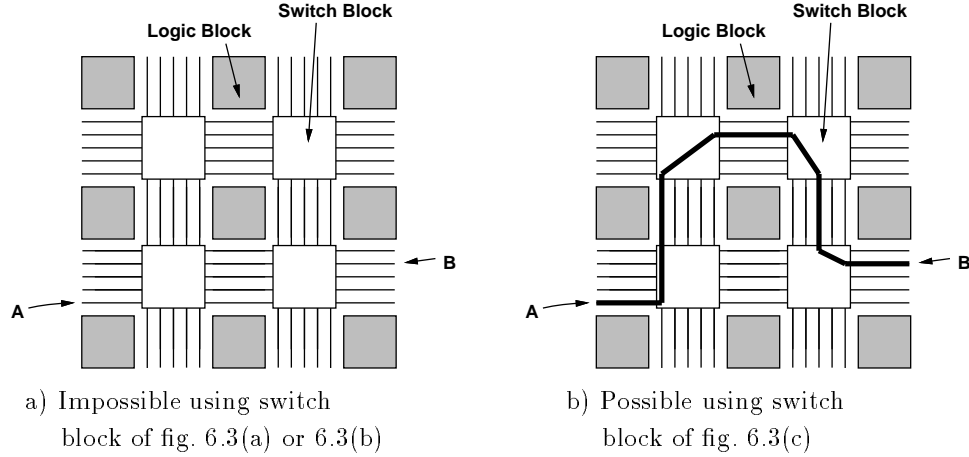


Figure 6.4: Routing a net from A to B .

a net that must connect track A to track B . If either of the switch blocks in Figures 6.3(a) or 6.3(b) is used, the connection is impossible. Each track in Figure 6.3(a) and (b) is labeled; both of these switch blocks are such that a track labeled i can only be connected to another track labeled i . Since track A would have a different label than track B , the connection is impossible, no matter how many switch blocks are traversed along the route. In [87, 88], such a routing structure is termed *disjoint*.

To alleviate this problem, we have used the switch block shown in Figure 6.3(c). This is similar to the switch block in Figure 6.3(b), except the diagonal connections have been “rotated” by one track. A precise description of the switch block can be written by representing it by a graph $M(T, S)$ where each node in T represents a terminal (incident track) of the switch block and each edge in S represents a programmable switch that connects two terminals. T is partitioned into four subsets, each with W terminals (each subset represents the tracks incident to one side of the switch block). Each terminal in T is labeled $t_{m,n}$ where m is the subset number ($0 \leq m \leq 3$) and n is the terminal number within the subset ($0 \leq n \leq W - 1$). Figure 6.5 shows the correspondence between terminal label and physical switch block pin. The set of edges, S , for the non-disjoint switch block is then:

$$S = \bigcup_{i=0}^{W-1} \{ (t_{0,i}, t_{2,i}) , (t_{1,i}, t_{3,i}) , (t_{0,i}, t_{1,(W-i) \bmod W}) , (t_{1,i}, t_{2,(i+1) \bmod W}) , (t_{2,i}, t_{3,(2W-2-i) \bmod W}) , (t_{3,i}, t_{0,(i+1) \bmod W}) \} \quad (6.1)$$

In Section 6.2.3, this switch block will be compared to the others in Figure 6.3.