NoCIC: A Spice-based Interconnect Planning Tool Emphasizing Aggressive On-Chip Interconnect Circuit Methods

V. Venkatraman, A. Laffely, J. Jang, H. Kukkamalla,
Z. Zhu & W. Burleson
Interconnect Circuit Design Group
Department of Electrical and Computer Engineering
University of Massachusetts Amherst
{vvenkatr}@ecs.umass.edu

This work was supported by SRC Tasks 766 & 1075 and a grant from Intel.

ICDG

Outline

- System-on-Chip Design
- Nanometer Design Challenges.
- Network-on-Chip
- Advantages of NoC
- Maximize Interconnect-centric NoC design? An example scenario!
- NoCIC – Network-on-Chip Interconnect Calculator
- High performance circuit techniques.
- Sample results from NoCIC.
- An example scenario cont…

System-on-Chip

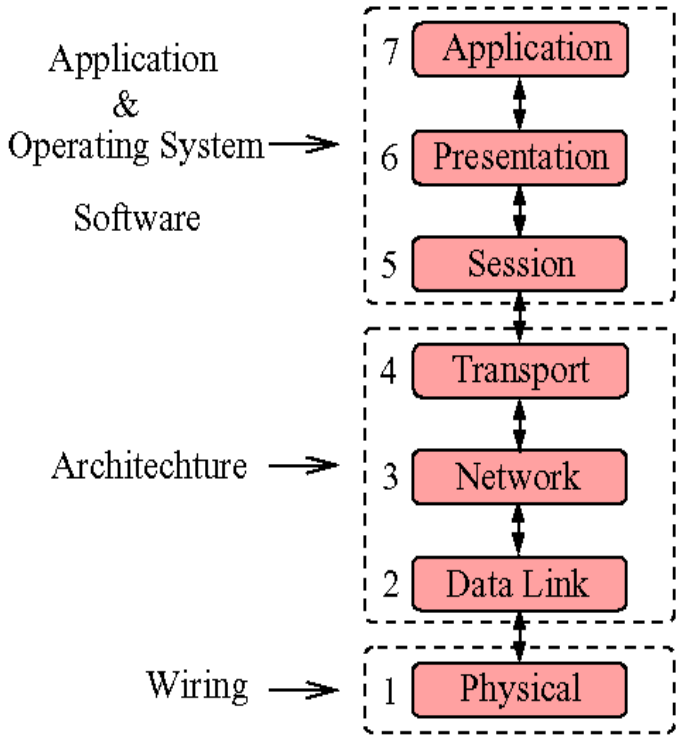
- SoC designs provide integrated solutions to cope with increasing circuit complexity.
- Increase performance by replication or reuse of resources.
- Uses standardized bus systems with the incorporation of pre-designed Intellectual Property (IP) cores.
- Interconnect-centric communication fabric.
- According to ITRS in the next decade, SoCs at 50nm will have 50 billion transistors and operate at 10Ghz.

Nanometer design challenges

- Wires have become potential showstoppers for performance and power.
- Optimistic predictions estimate propagation delays for highly optimized global wires to be between **6 – 10 clock cycles in 50nm.** [Benini 02]
- Wire technology will be a limiting factor for SoC performance
- Global clock distribution extremely difficult with negligible skews leading to Globally Asynchronous Locally Synchronous Systems (GALS).
- Network-on-Chip architecture proposed to cope with interconnect effects.

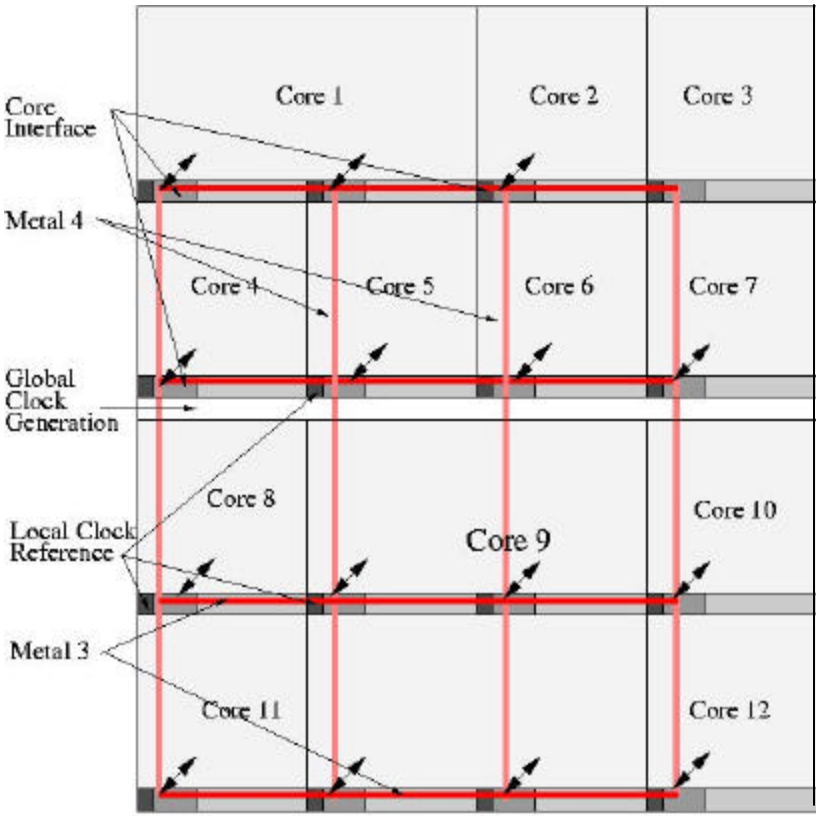
Network-on-Chip

- Layered Design of reconfigurable micronetworks
- Exploits methods and tools used for general network and can achieve better communication in SoCs.
- Micronetworks based on the ISO/OSI model.
- NoC architecture consists of Data link, Network and Transport layers.



Advantages of NoC

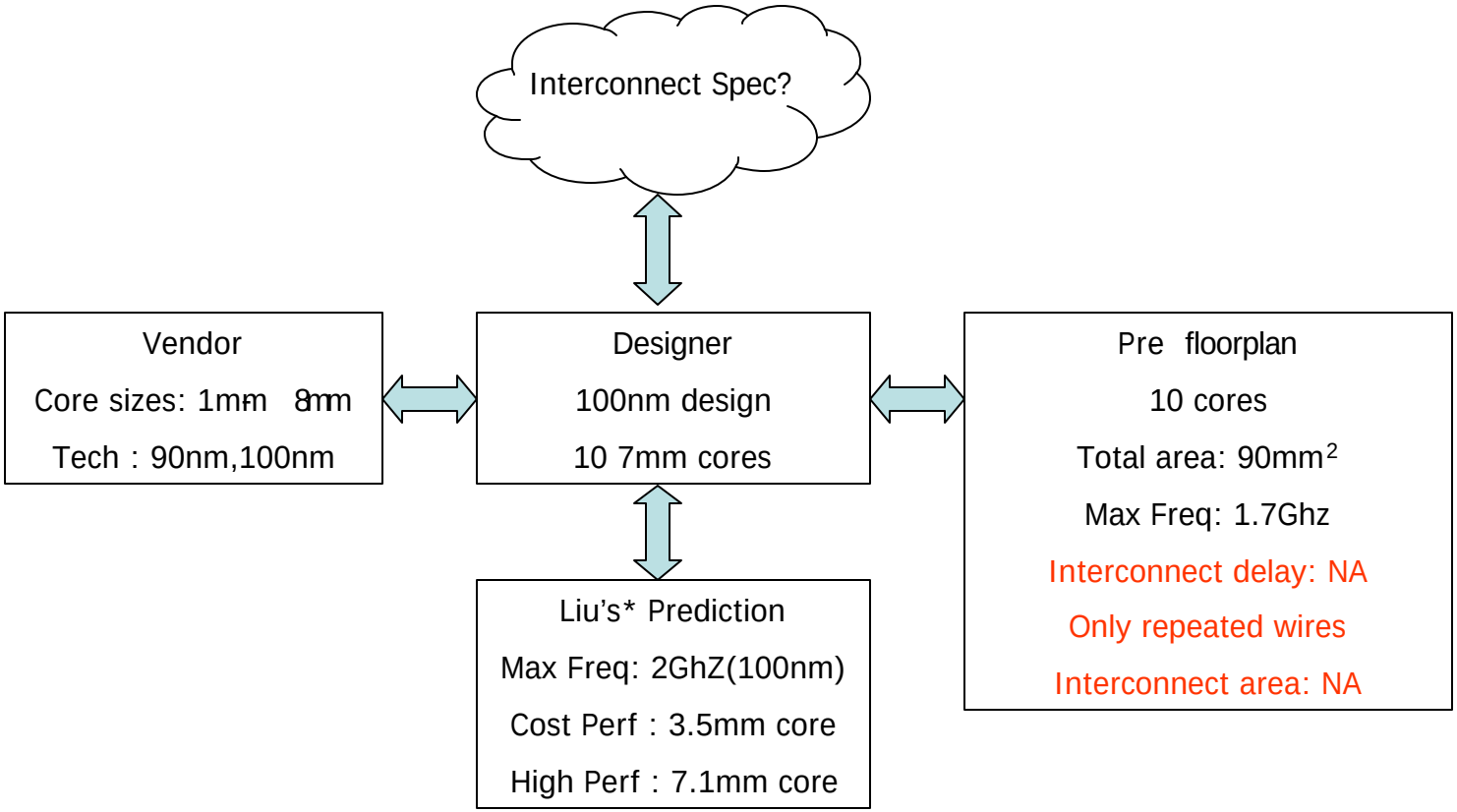
- Tiled architecture with mesh interconnect
- Point to point communication pipeline
- Allows for heterogeneous cores
  - Differing sizes, clock rates, voltages
- Regularity of the architecture eases interconnect design to a point to point communication.
- Allows for reuse of tiles.
- Regular repetition of similar wire segments which are easier to model as DSM interconnects.
- Allows the application of other high performance interconnect techniques including repeaters due to regularity in design.



RECENTLY PROPOSED NOC ARCHITECTURES

[BENINI 02], [KUMAR 02], [DALLY 01]

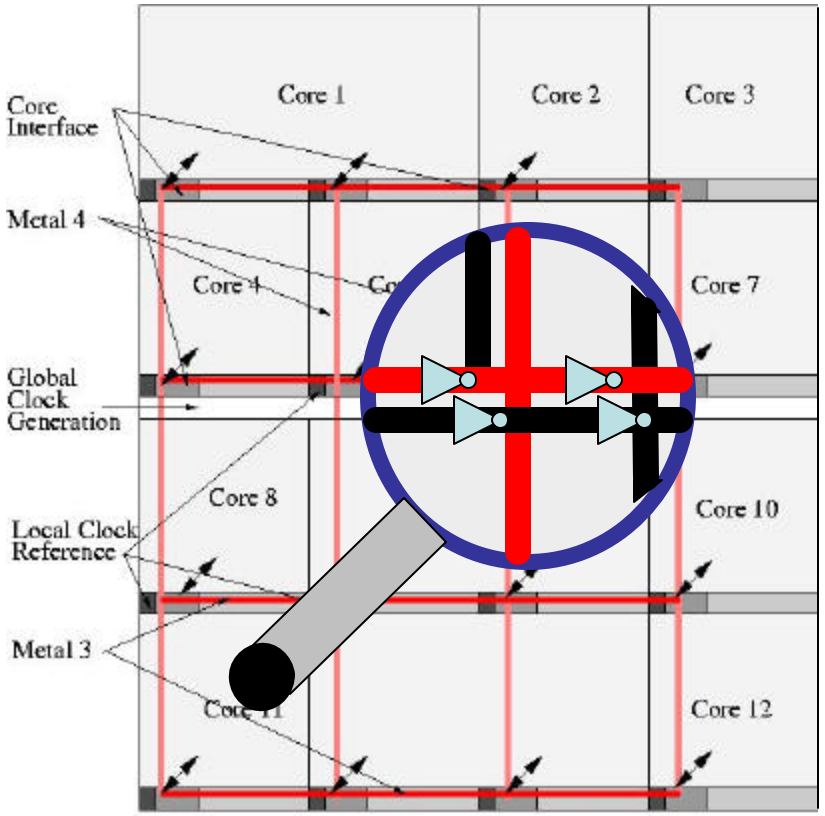
Example Scenario



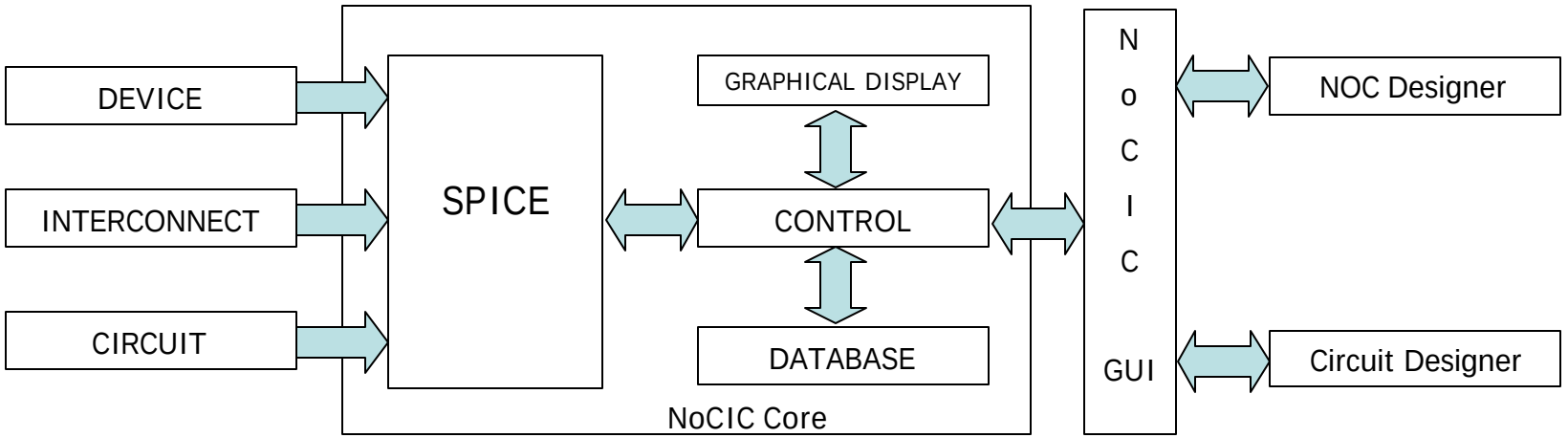
* J. Liu et.al System level interconnect design for network-on-chip interconnect IPs, *in proceedings of the international workshop on System level interconnect prediction, SLIP 2003.*

Questions from system-level designers about interconnects at pre-floorplan stage?

- Dependant parameters
  - Delay?
  - Power?
  - Active area?
  - Signal Integrity?
- Independent parameters
  - Technology scaling?
  - Signaling techniques?
  - Process variation?



NoCIC: Network-on-Chip Interconnect Calculator



- Network-on-Chip Interconnect Calculator, a spice-based tool.
- Accurately evaluate the interconnect design space.
- Choice of alternative signaling options Delay and power for interconnects displayed over a wide range of design space.

Why Spice-based analysis?

- Spice provides a relatively accurate electrical analysis of a circuit.
- These high performance circuit techniques do not have convenient closed form expressions.
- Easier to adapt to changes/advances in device and technology.
- The existing tools do not use Spice based exploration.
- Allows circuit designers see impact on NoC
- When coupled with analytical approach provides an exhaustive analysis of the design space.
- Running Spice takes a lot of design effort and time.
- Depends on the accuracy of device models.
- Does not give a direct relationship between parameters.

Analytical approaches

SUSPENS [Bakoglu 87]

BACPAC [Sylvester 99]

RIPE [Geuskens 97]

GENESYS [Eble 96]

GTX [Caldwell 02]

High Performance Interconnect Circuit techniques

- Repeater Insertion. [Alpert 97], [Adler 98], [Sylvester 99], [Ismail 00]
- Booster Insertion. [Nalmalpu 02]
- Differential current sensing. [Maheshwari 02], [Bashirullah 03]
- Multi-level current signaling. [Dhaou01], [Srinivasan 02]
- Bus-invert coding. [Stan 97]
- Low power bus coding techniques. [Sotiriadis 00]
- Static source-follower driver. [Zhang 00]
- Pseudodifferential interconnect. [Zhang 00]
- Transition Aware Global Signaling. [Kaul 02]
- Near speed-of-light signaling. [Chang 02]

A snapshot of NoCIC

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NoCIC : Network-on-Chip Interconnect Calculator

PARAMETER SELECTION WINDOW

NoC Parameters

Tile Size: 4mm

Bus Size: 8-bit

Supply Voltage: 1.8v

Interconnect Parameters

Signaling Technique: Repeater

Technology: 180nm

Shielding: Unshielded

Analysis

Ouput: Delay

Compare:

- ☐ Repeater
- ☐ Booster
- ☐ Differential Current Sensing
- ☐ Multi-level Current Signaling

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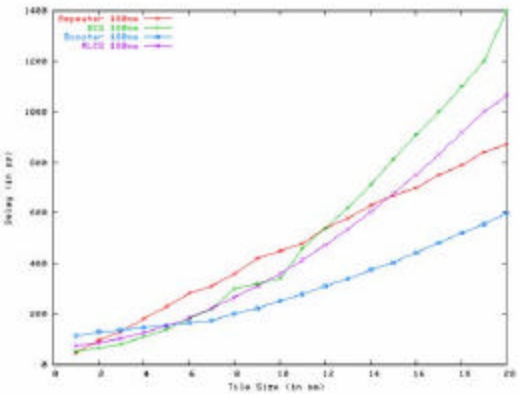
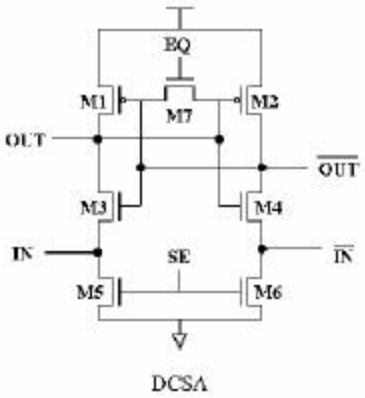
PLOT DISPLAY WINDOW





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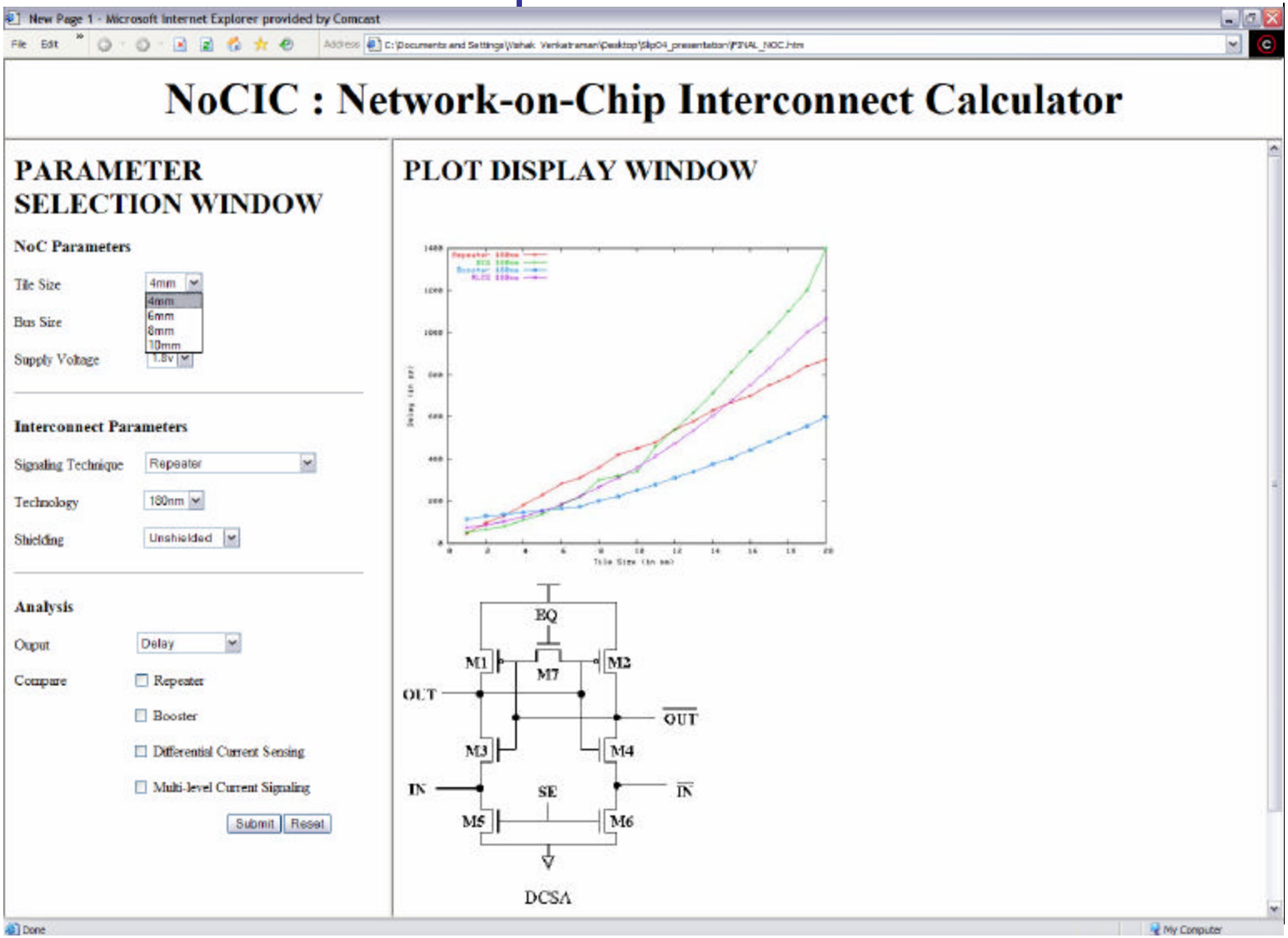

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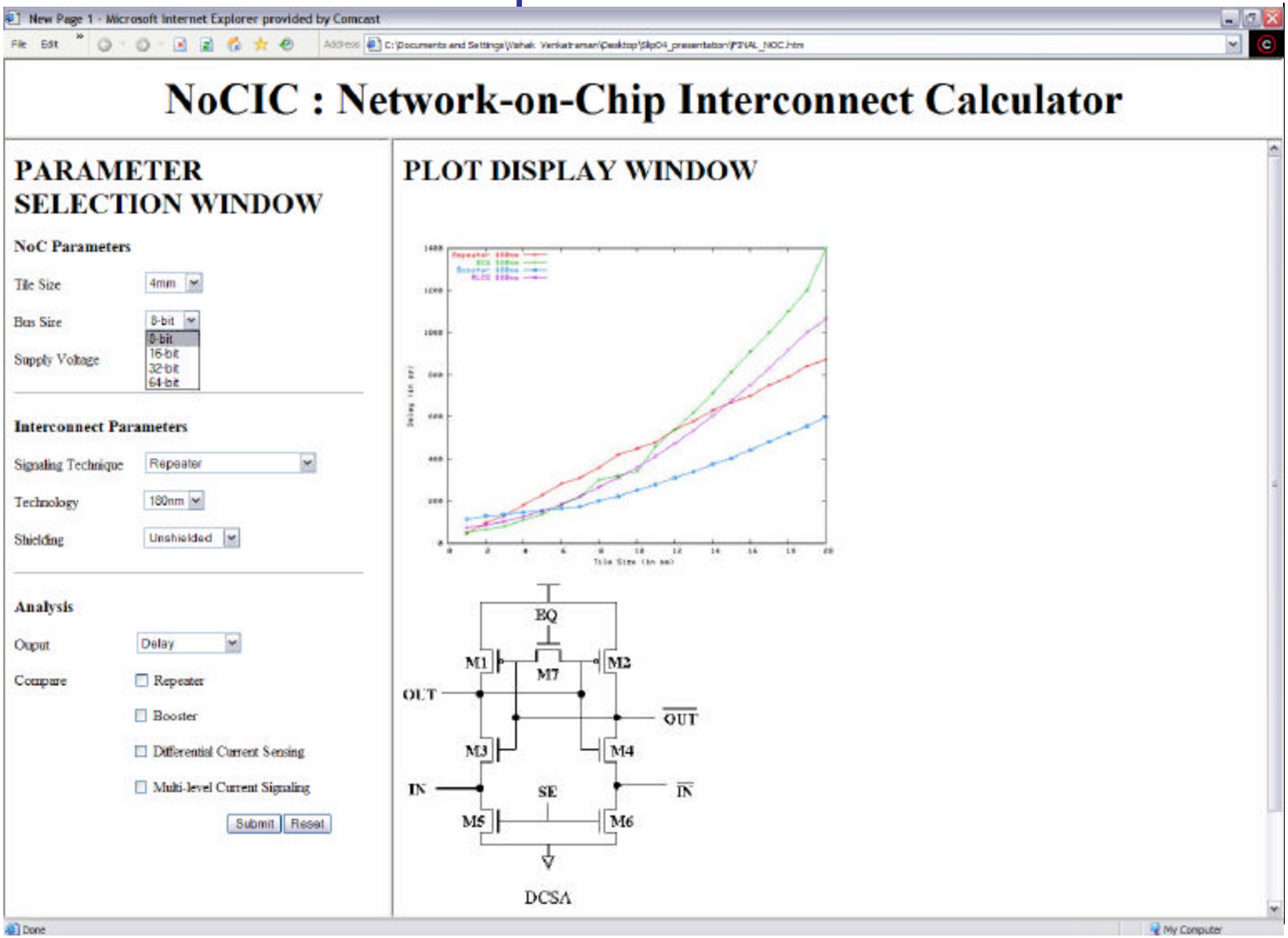

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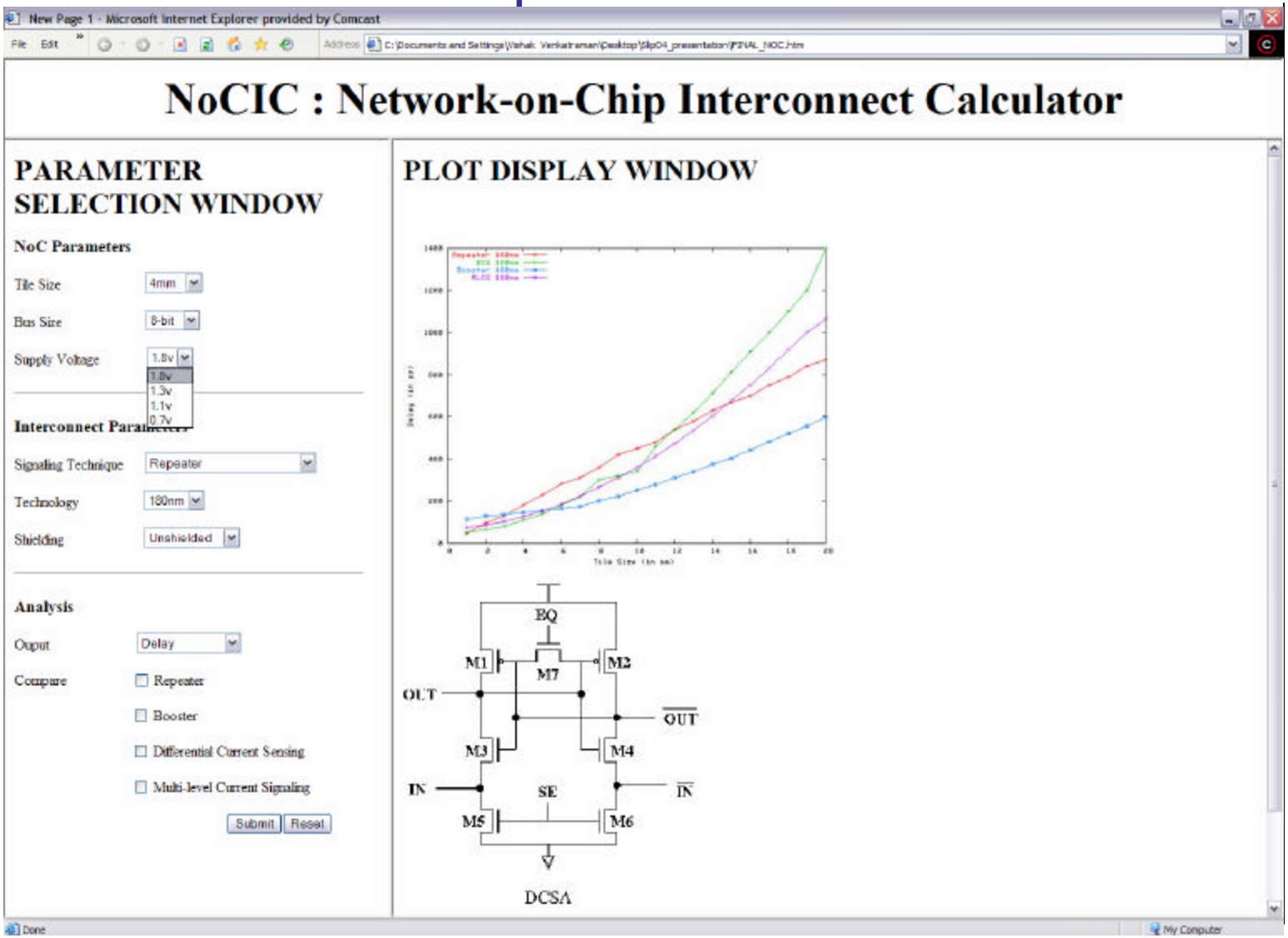

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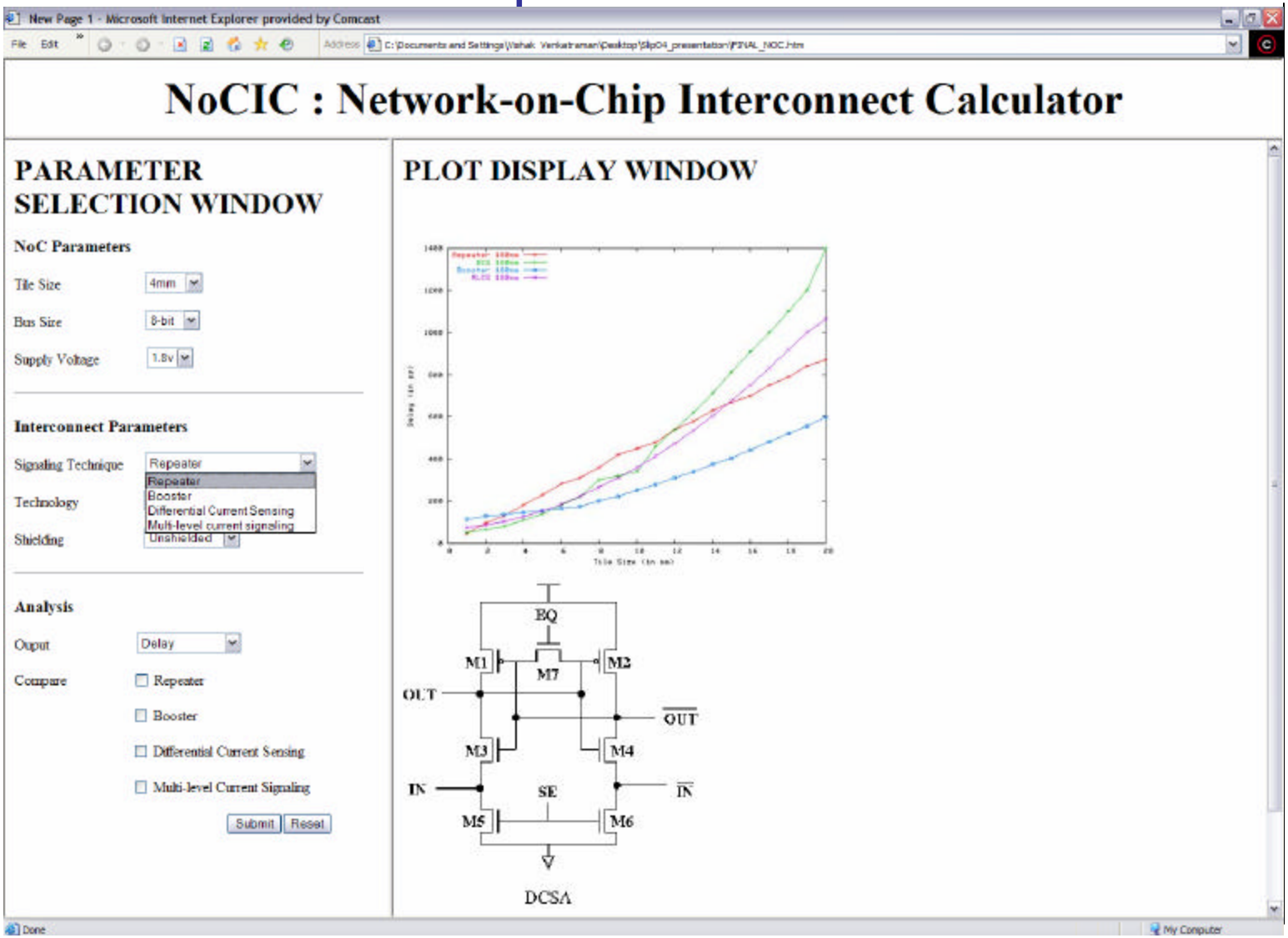

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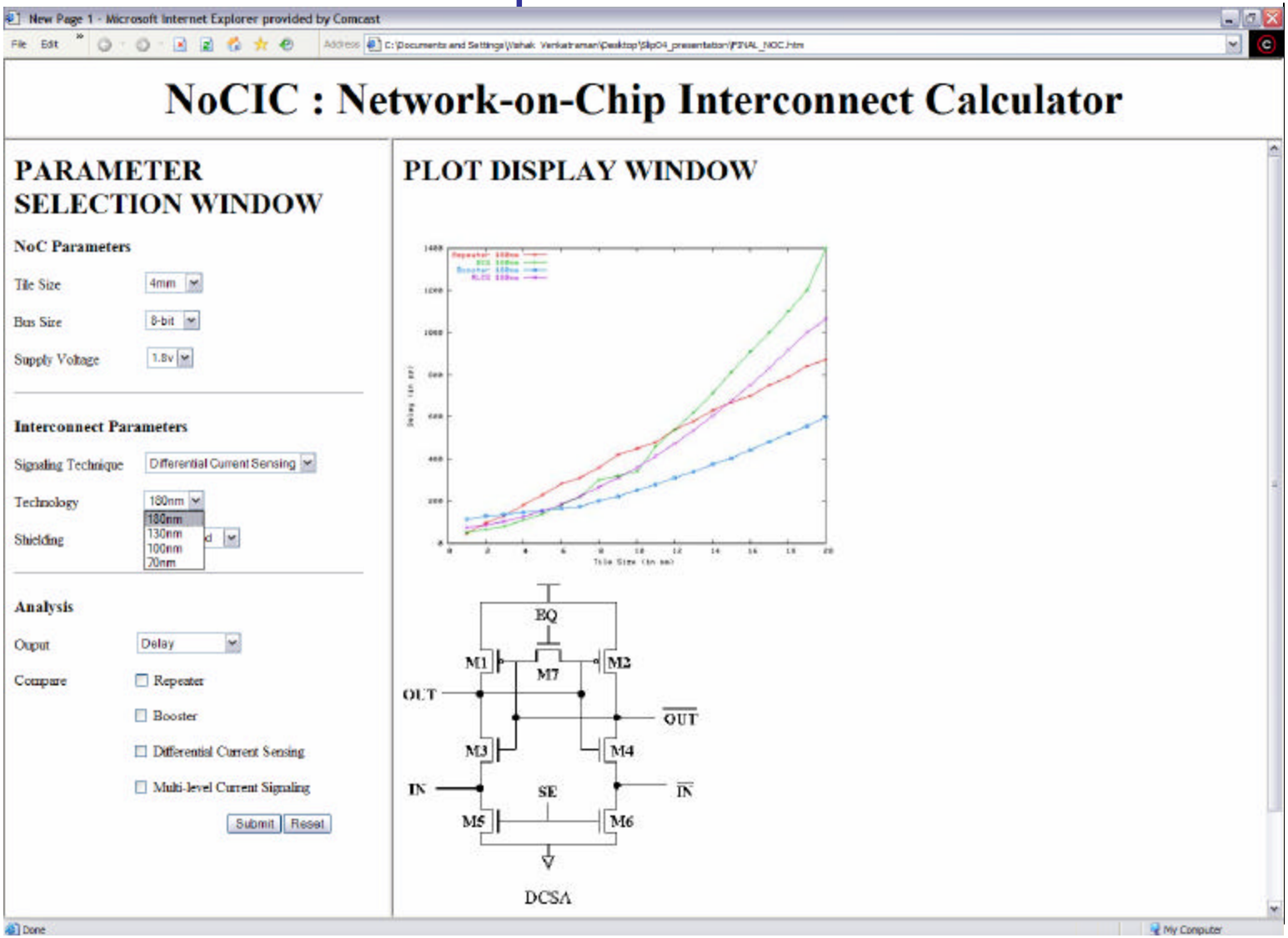

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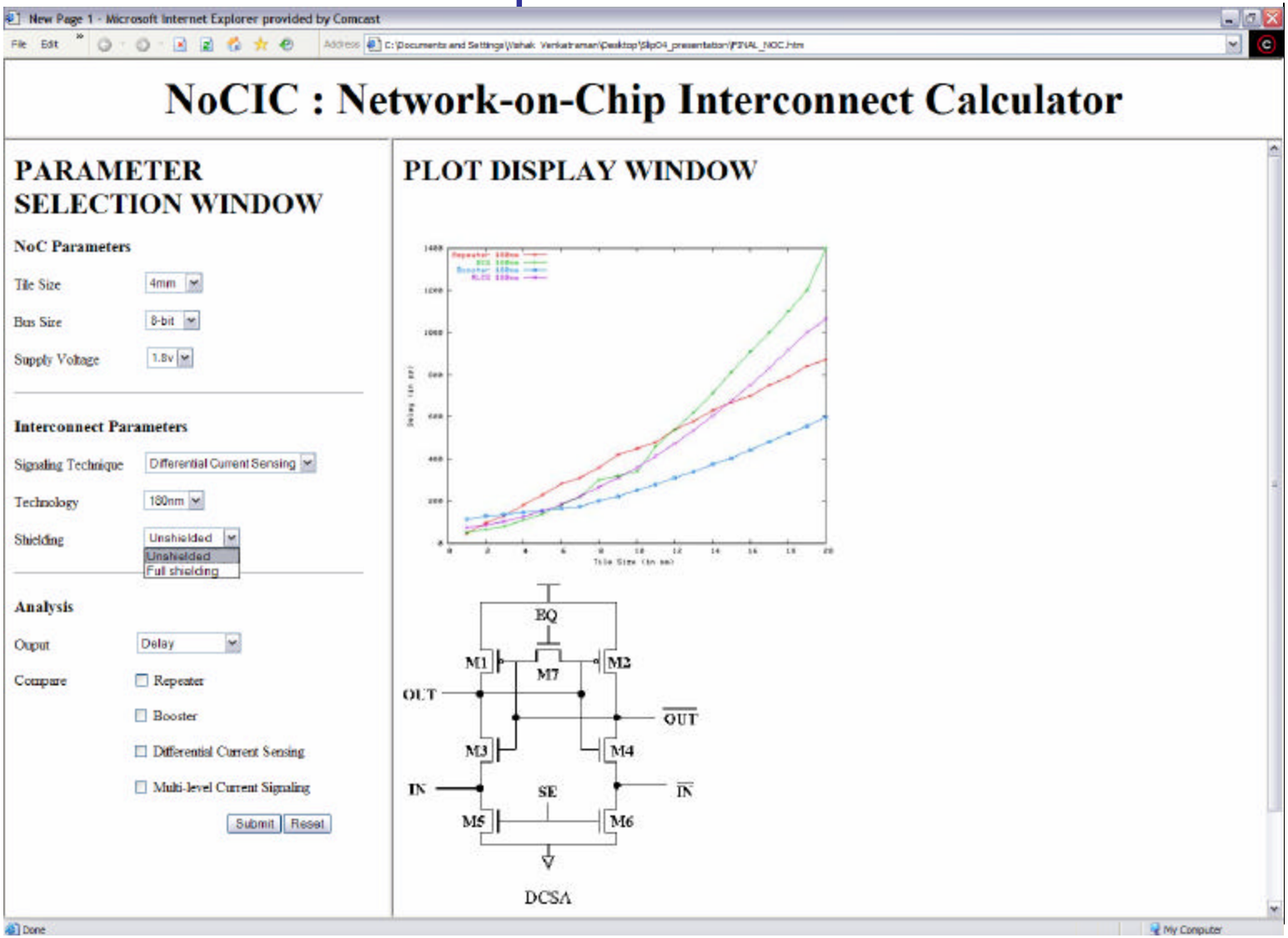

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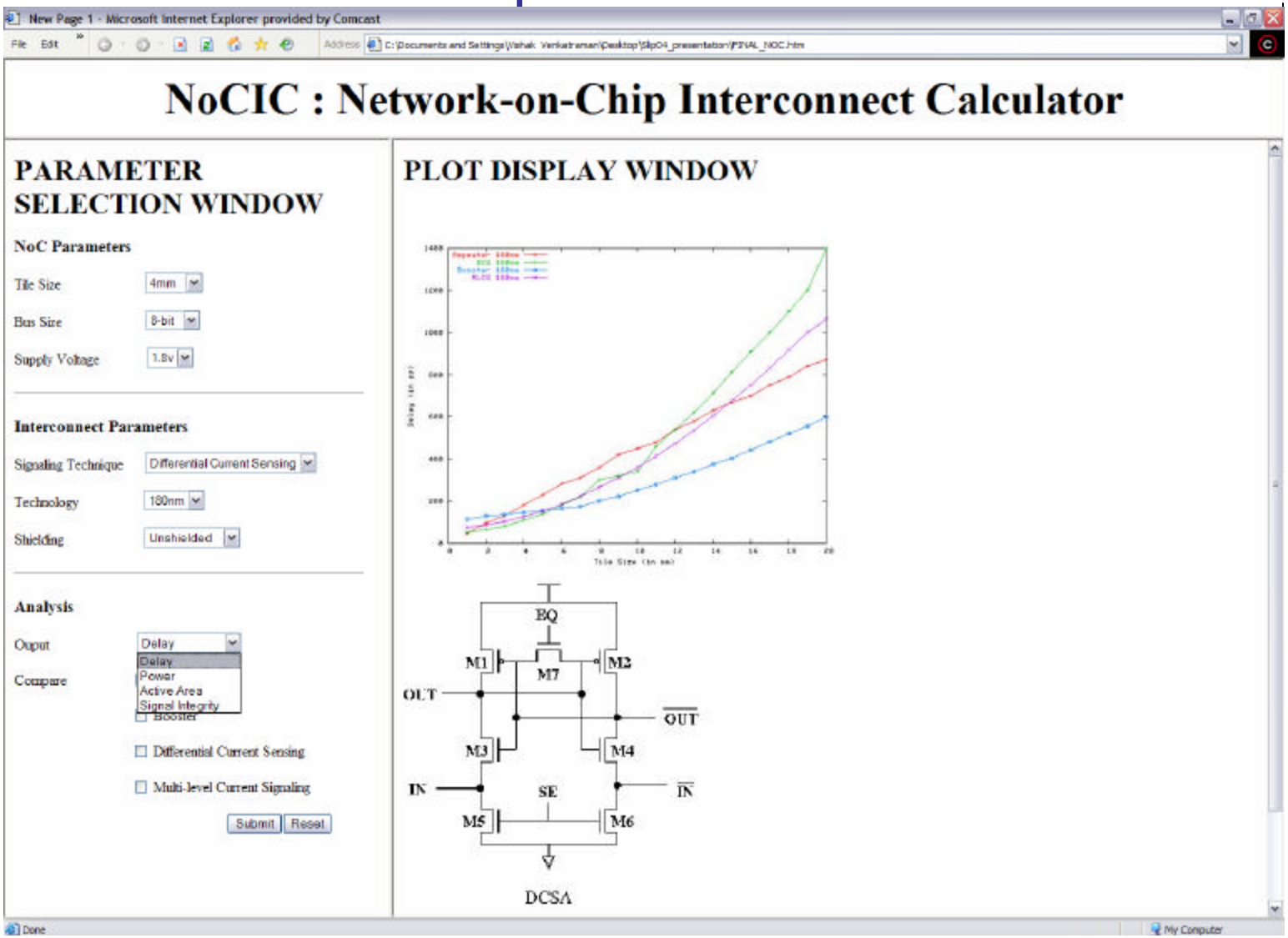

Advantages of NoCIC

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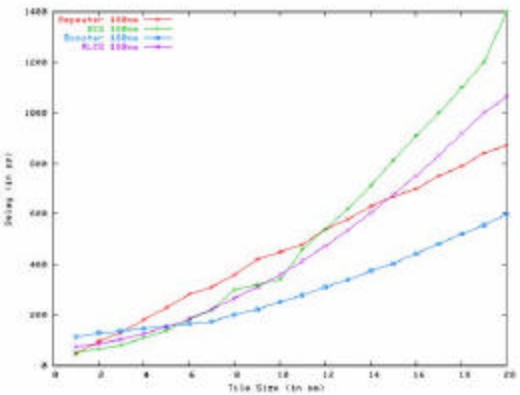

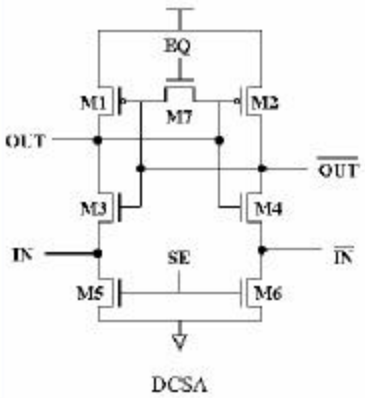

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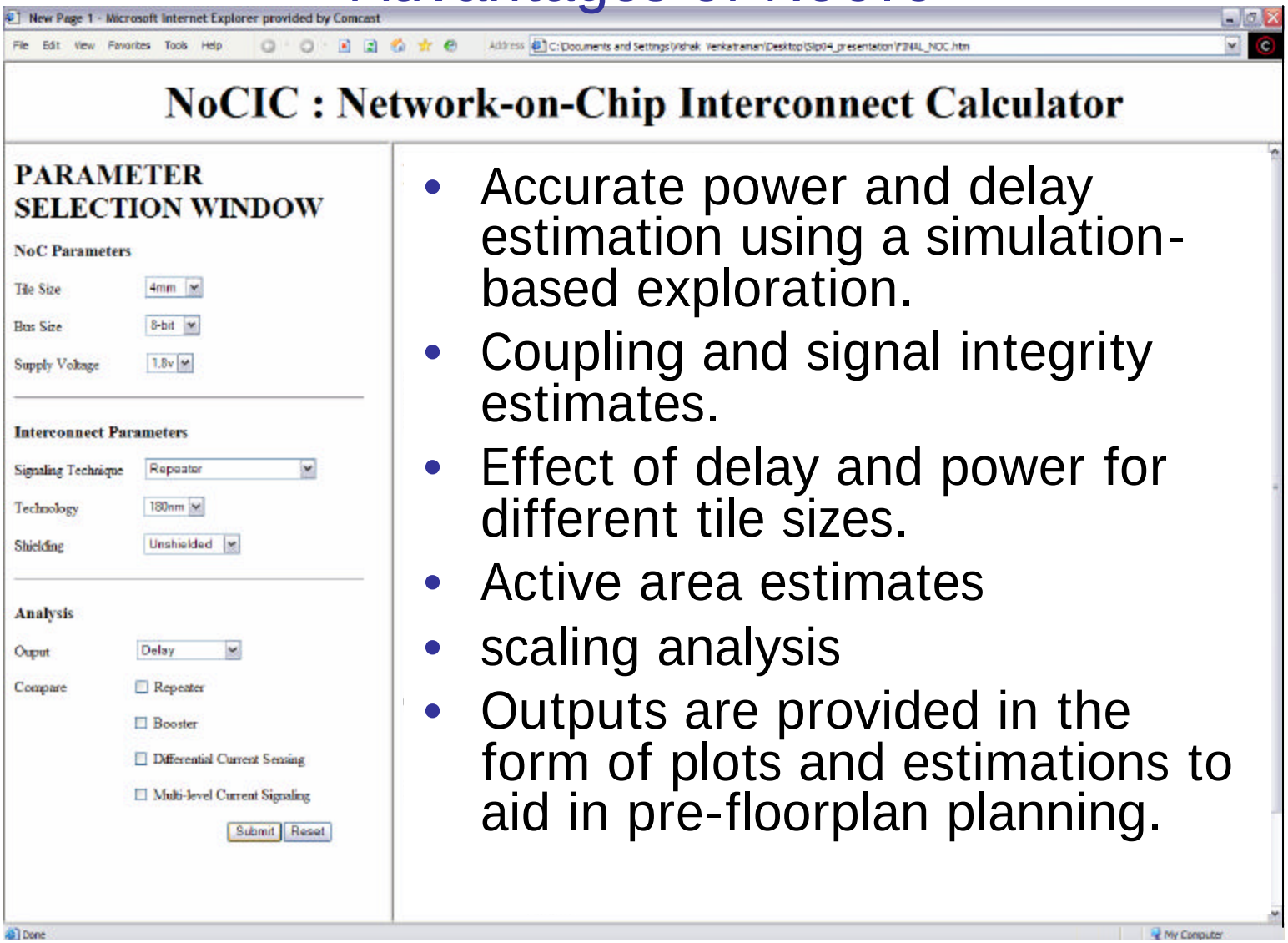
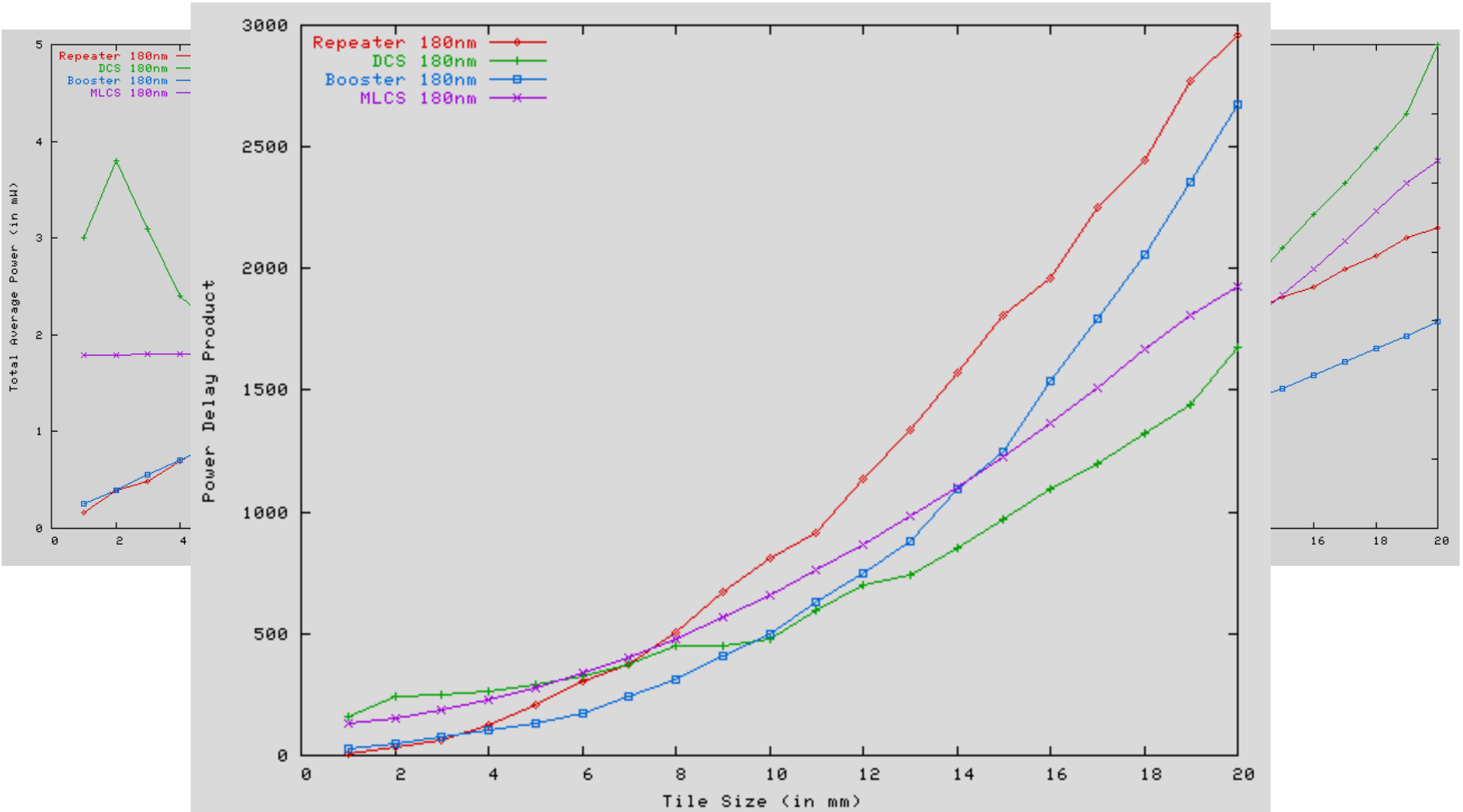
Advantages of NoCIC



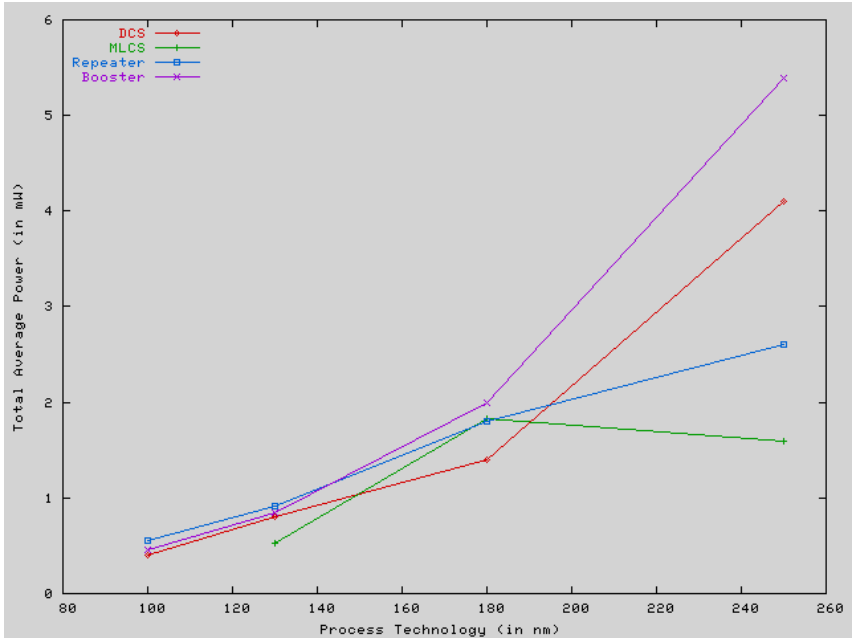
- Accurate power and delay estimation using a simulation-based exploration.
- Coupling and signal integrity estimates.
- Effect of delay and power for different tile sizes.
- Active area estimates
- scaling analysis
- Outputs are provided in the form of plots and estimations to aid in pre-floorplan planning.

Effects of tile size

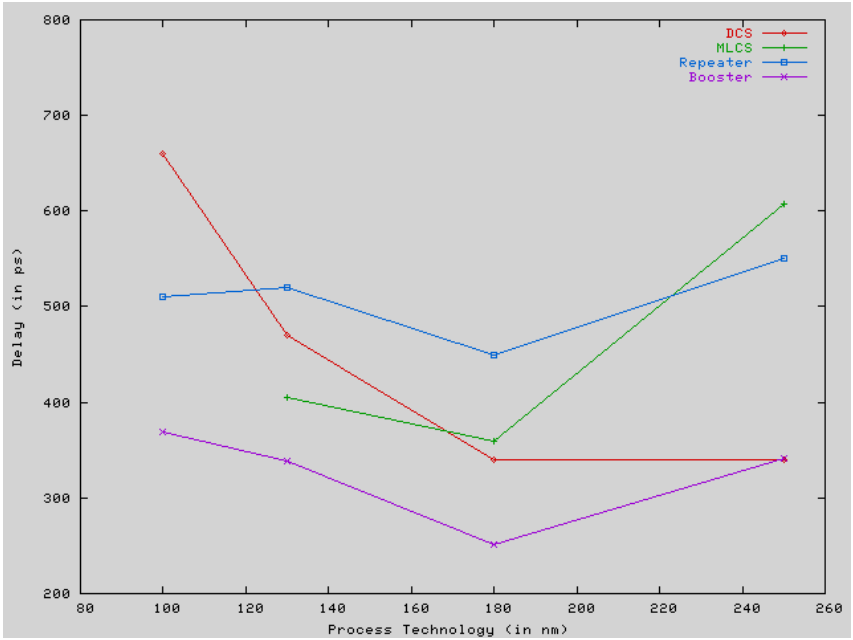


POWER DELAY PRODUCT

Scaling analysis

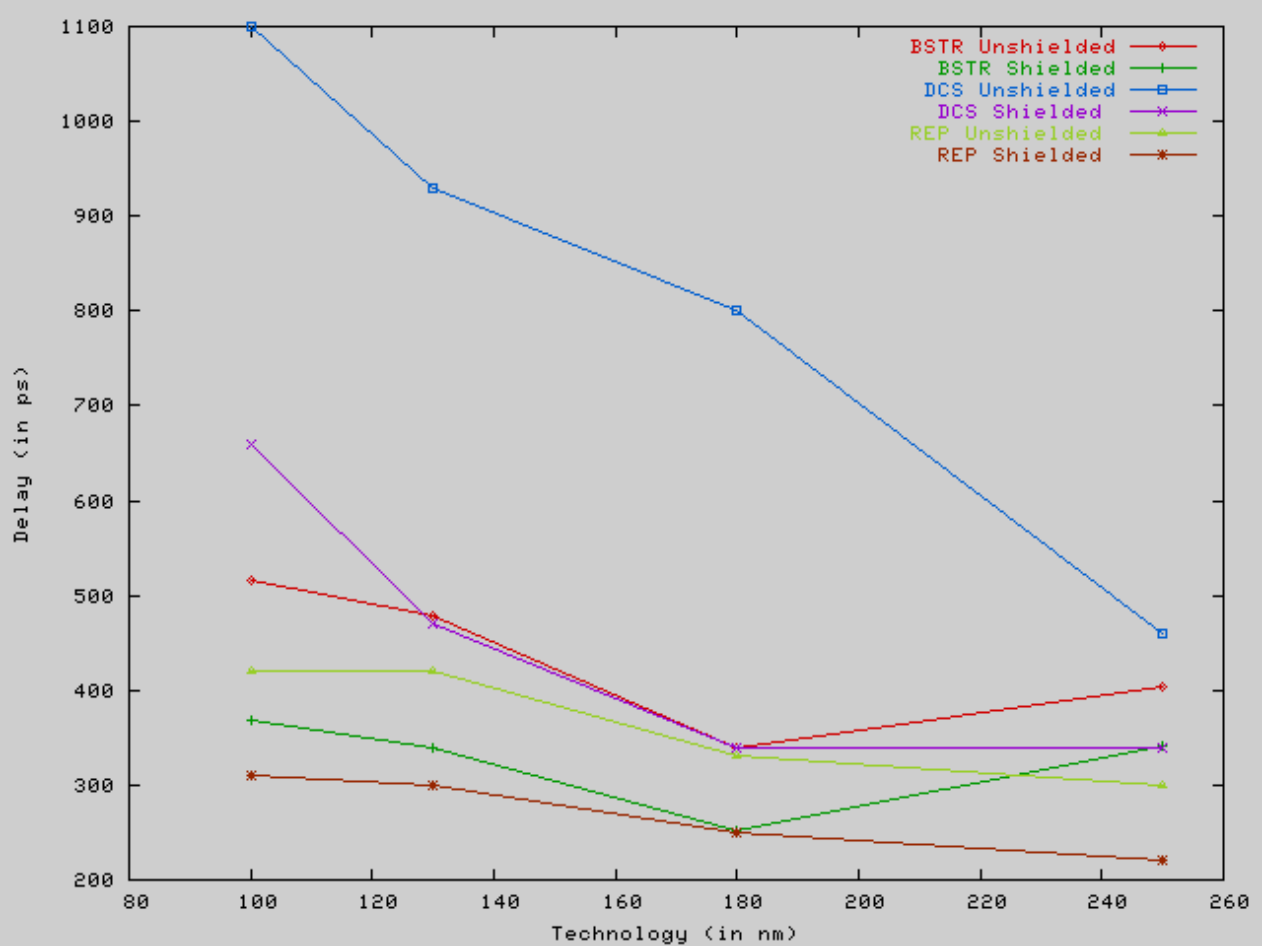


Power

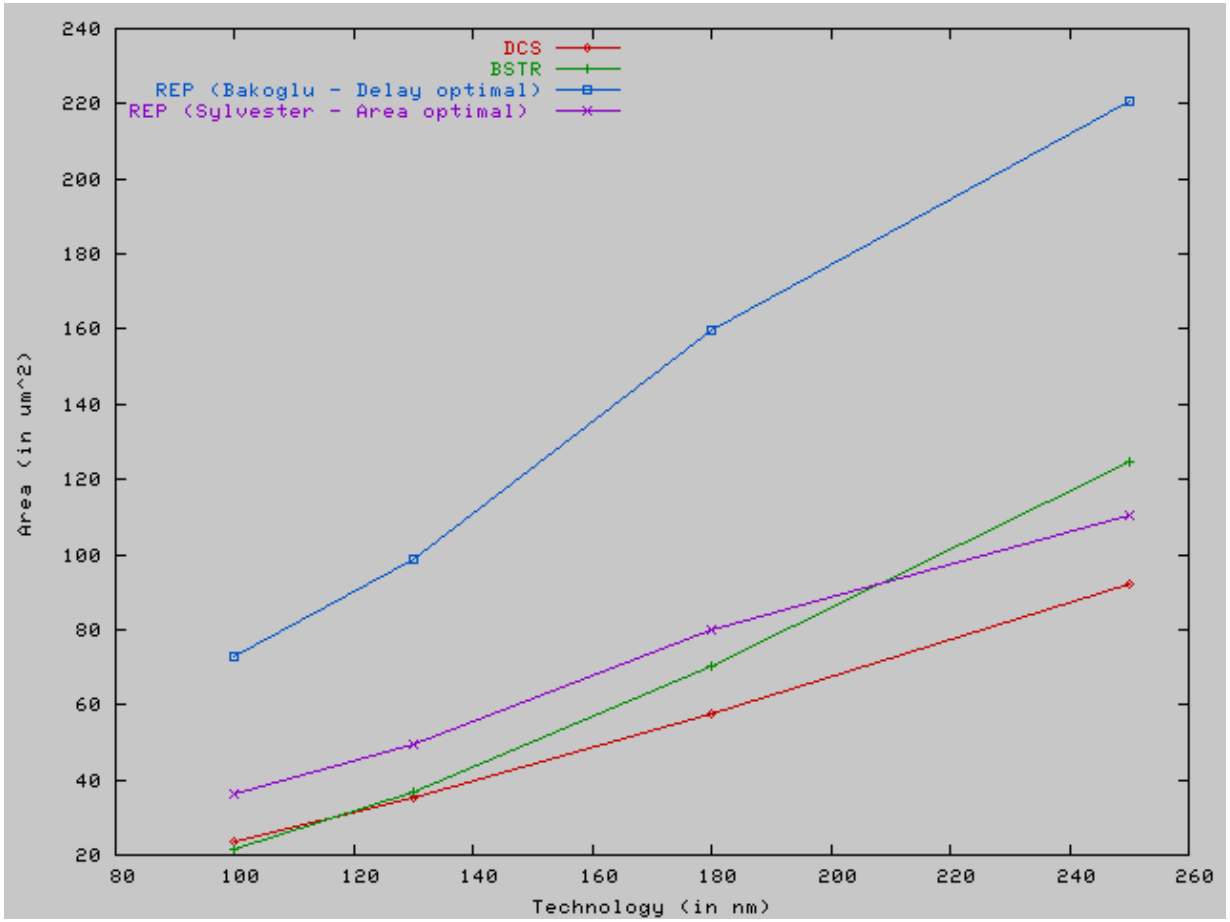


Delay

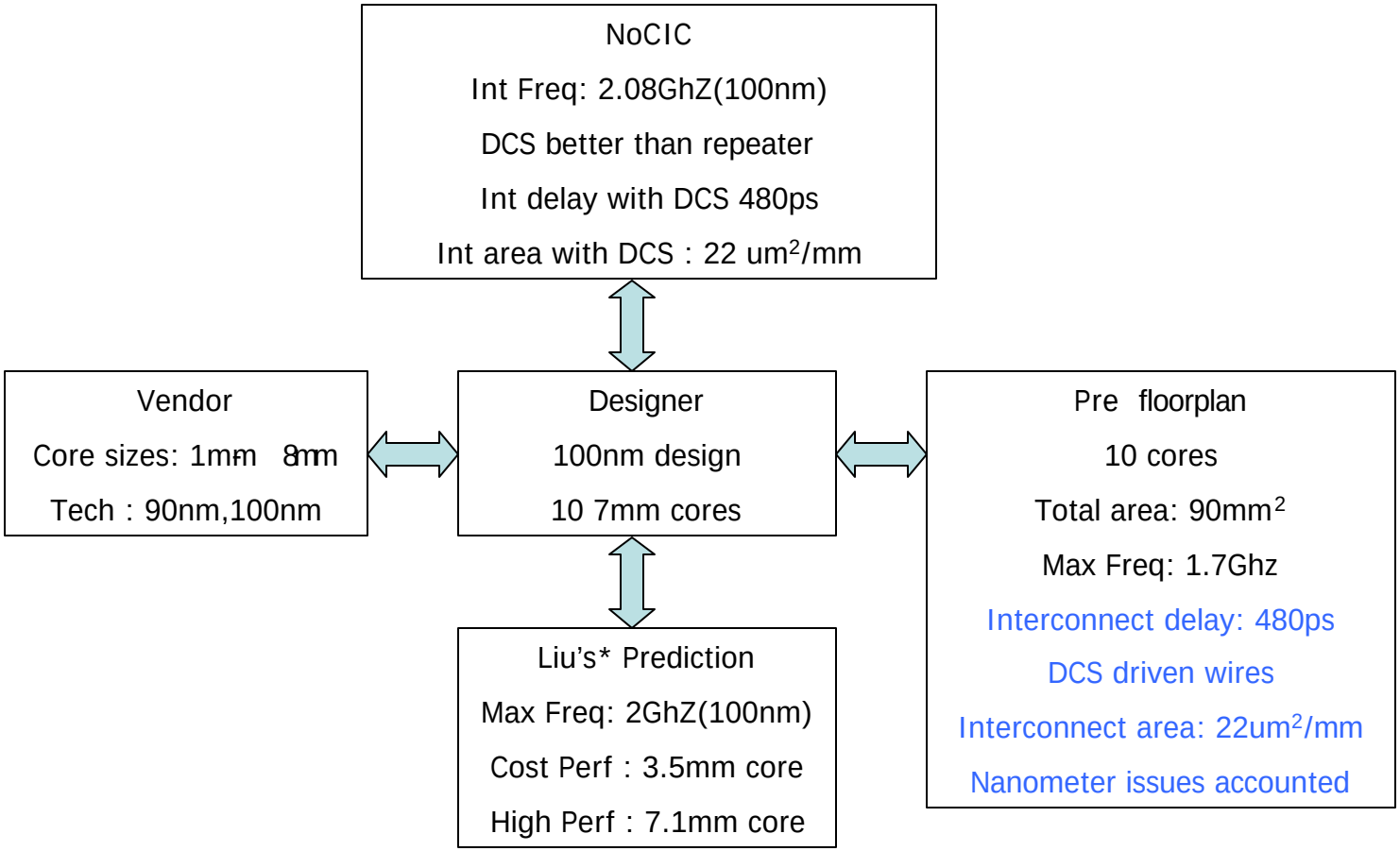
Coupling analysis



Active area analysis



Example Scenario cont...



* J. Liu et.al, System level interconnect design for network-on-chip interconnect IPs, *in proceedings of the international workshop on System level interconnect prediction, SLIP 2003*.

Conclusion

- NoCIC, a spice-based interconnect tool was implemented.
- Sample results from NoCIC was presented
  - Area and coupling analysis.
  - Effects of tile size.
  - Scaling analysis.
- This tool hopes to aid NoC architects to efficiently evaluate interconnect issues.
- Serve as a pre-floorplan tool providing detailed interconnect information.
- Provides a bridge between circuit and NoC.
- Can be used to develop new analytical models.

Future work

- Add more signaling techniques.
- Run real-time HSPICE simulations on user given values.
- Interconnect synthesis tool with optimization techniques.
- Add new parameters.
- Study of inductance effects, signal integrity and reliability.
- Feasibility of NoCIC to be added as a signaling technique analysis tool in GTX.

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ICDG

Outline

- Nanometer Design Challenges an example.
  - Nanometer Design challenges system level designers face today.
- NoC architectures proposed to cope with interconnects.
  - Need for designers to be abstracted from device and circuit level issues.
- Questions asked by system level designers in the pre-floorplan stage?
- Circuit analysis combined with analytical analysis required to answer some of those questions.
  - Existing tools do not consider other proposed interconnect signaling techniques other than repeaters.
  - Existing tools do not used a spice based approach which provides another perspective apart from the information extracted from analytical models.
- NoCIC tries to answer those questions. It is built under the fabric of expandable high performance circuit techniques and spice-based.
- High Performance Circuit techniques
  - Repeaters (dealt by other similar work like Bacpac, Genesys ...)
  - Boosters (similar to repeaters and have some closed form expressions governing parameters like delay and power)
  - Differential current sensing (relatively new and does not have convenient closed form expressions for analytical analysis)
  - MLCS (very novel and also does not have closed form expressions.)
- Why spice based? Because spice is relatively accurate, provides a different perspective than analytical models, these do not have convenient closed form expressions, when coupled with analytical analysis when available provide an exhaustive analysis. Easier to add new device models and small changes to circuits.
- Some results by NoCIC
- An example scenario in which nocic can be used.
- Conclusion
- Thank you.

Example

Vendor

Provides IP cores

90nm, 100nm, 130nm supported

Core sizes supported 1mm to 8mm.

Designer

Chooses 100nm tech.

Find an optimum core size for high performance or cost performance.

Based on Liu's predictions chooses 7.1mm core size

Tools

Liu et.al predicts

At 100nm

3.5mm core size for high performance

7.1mm core size for cost performance

Only repeaters to drive interconnect.

NoCIC predicts

Use DCS instead of repeaters.

DCS max operating frequency for 8mm tile is 2.08Ghz.

DCS is better for orthogonal coupling.

Even with 2 wires per signal area is saved.

Designer does not know how interconnect performs at 100nm and are there any other optimizations possible and how does interconnect performance vary with core size

Example Scenario

- For the tile size range of 1mm to 8mm the delay when differential current sensing is used is 110ps to 480ps at 100nm respectively.
- It can be roughly said that the interconnect frequency of operation excluding gate delay is is around 2.08GHZ at 100nm when a 8mm tile is used.
- Liu predicted that at 100nm a core size of 3.5mm is optimum for high performance and 7.1mm for cost performance.
- Suppose a designer decides to use a 7.1mm core at 100nm based on Liu's prediction and wants to find out what is the best technique for interconnects when the tile is 7.1mm
- NoCIC can estimate that differential current sensing is the best with a maximum operating frequency of 2.08GHZ at 8mm.
- Liu et.al. predicted that the maximum frequency of operation of a tile at 100nm is 2 GHZ for a high performance tile.
- This shows that interconnect performance with dcs is higher than the tile performance up to a tile size of 8mm

Nanometer Design Challenges: an example

- Wires have become potential showstoppers for performance and power
- ITRS predicts that chip size will scale up, while gate delays decrease compared to interconnect delays.

? = 0.3/ v e mm/sec (Speed of EMwaves)

In 50nm:

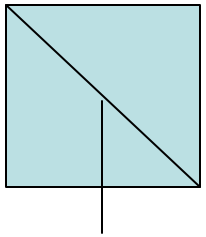
Chip die edge – 22mm, clock frequency – 10GHz

Ideal case – 1 clock period, if e = 1

Lower bound – 2 clock periods, if e = 1

Real-life signal propagation slower than lower bound

Optimistic predictions estimate propagation delays for highly optimized global wires to be between ***6 - 10clock cycles in 50nm***

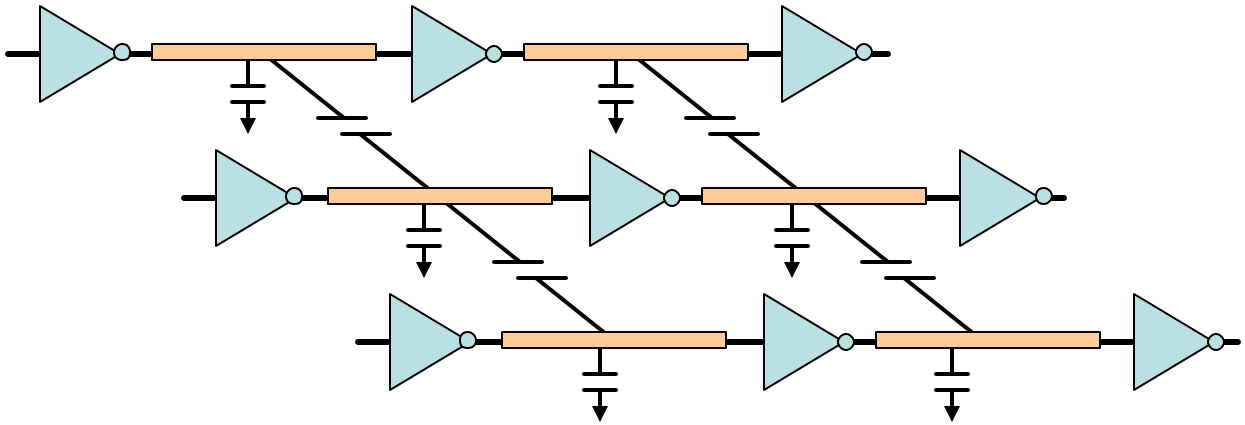


L. Benini and G. De Michelli, Networks on Chips: A New SoC Paradigm, technical article in Computer 2002.

Comparison of techniques used in NoCIC

Circuit Style	Mode	Design Issues	Advantages	Disadvantages
Repeater Insertion	Voltage	Optimum placement is important,	Delay linear with line length.	Area more for global wires
Booster Insertion	Voltage	Cannot be used if buffering is required	Does not break the line.	Cannot be combined with logic
Differential Current Sensing	Current	Sense enable synchronization is key for sensing to work	Performs well with highly capacitive lines.	Static power. Additional routing.
Multi-level Current signaling	Current	Delay sensitive to transmitter, receiver and decoder's sizing	Bandwidth improvement	Additional area. Susceptible to noise.

Repeater



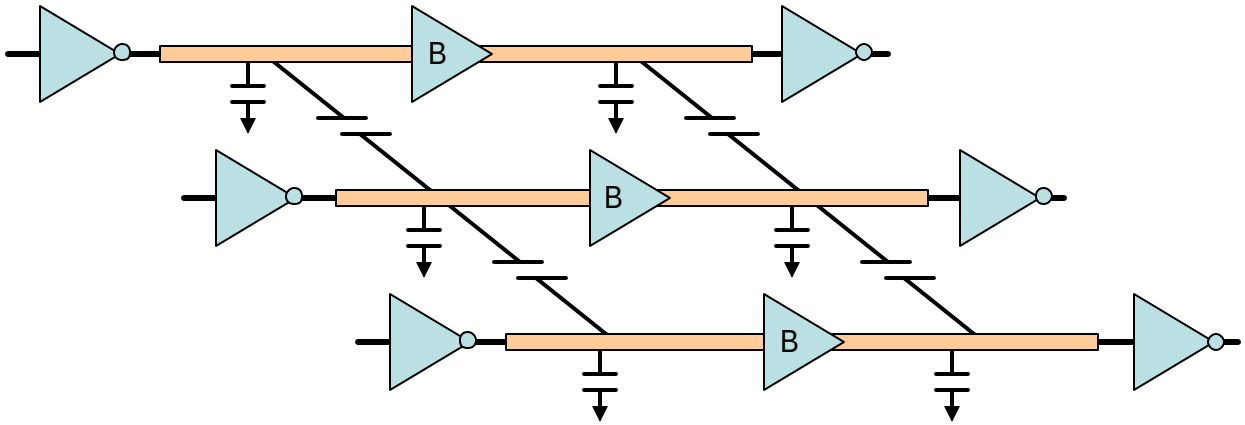
$$T_{50\%} = k\left[0.7R_o/h\,(C_{int}/k + hC_o) + R_{int}/k\,(0.4C_{int}/k + 0.7hC_o)\right]^*$$

$$k = \sqrt{0.4R_{int}C_{int} \,/\, 0.7R_oC_o}$$

$$h = \sqrt{R_oC_{int} \,/\, R_{int}C_o}$$

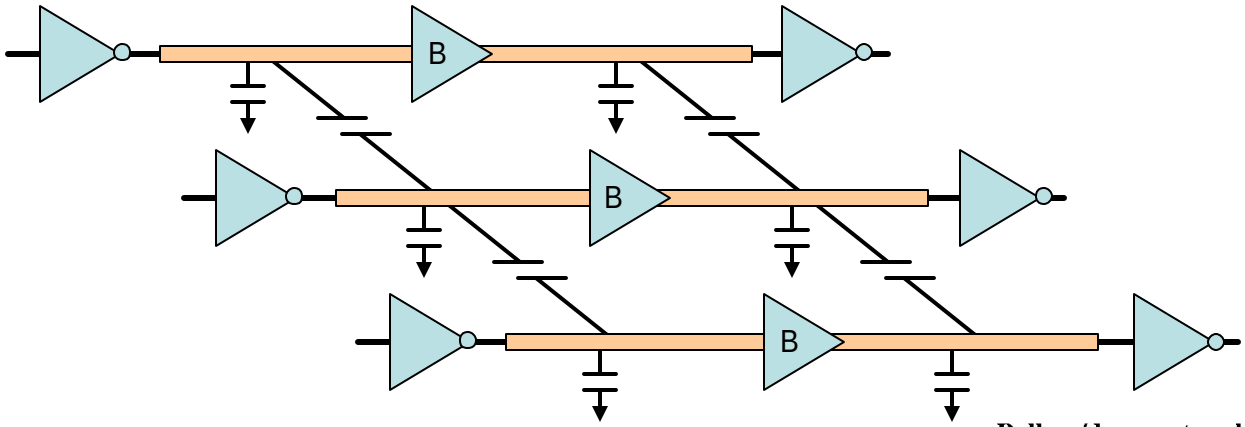
* H Bakoglu, Circuits Packaging and interconnections, Wiley international publications.

Booster*



* A Nalmalpu et,al, A Practical Approach to DSM Repeater Insertion: Satisfying Delay Constraints while Minimizing Area and Power, IEEE ASIC SOC Conf. 2001.

Booster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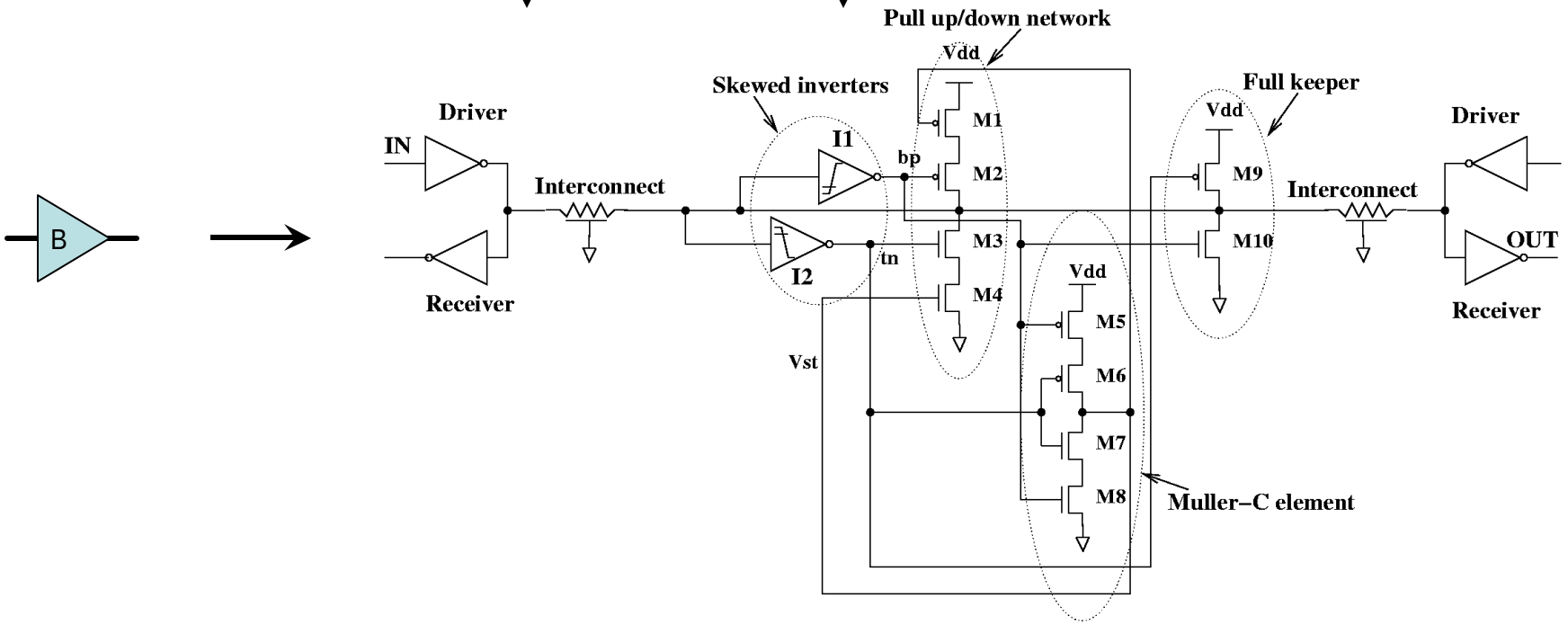
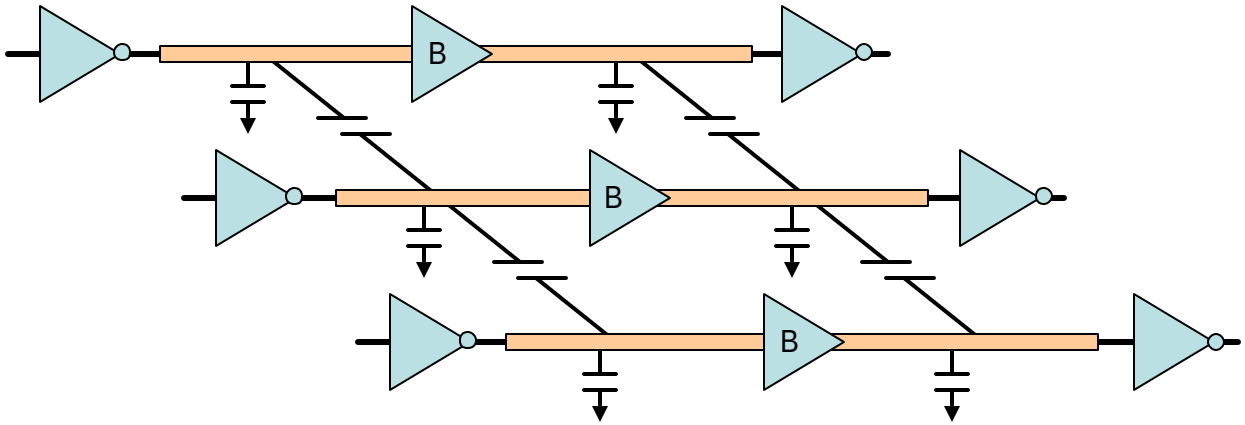
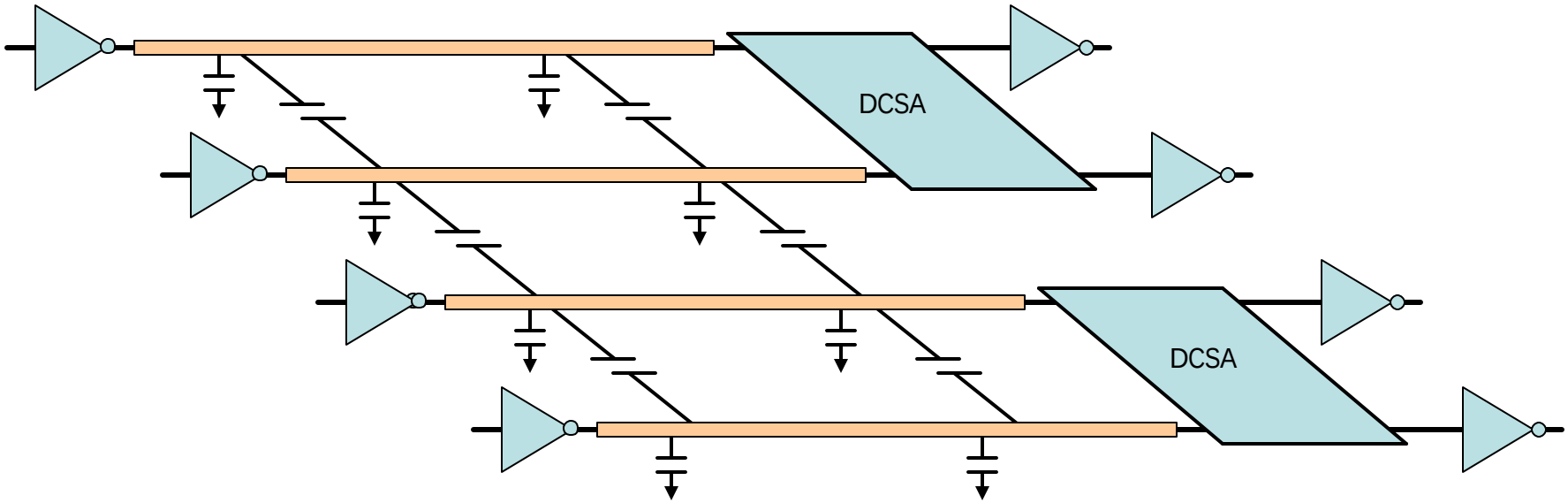

B
Pull up/down network
Vdd
Skewed inverters
Full keeper
Driver
IN
I1
M1
bp
M2
Vdd
M9
Driver
Interconnect
Interconnect
M10
OUT
M3
tn
I2
M4
Vdd
M5
Receiver
Receiver
Vst
M6
M7
M8
Muller–C element

Booster



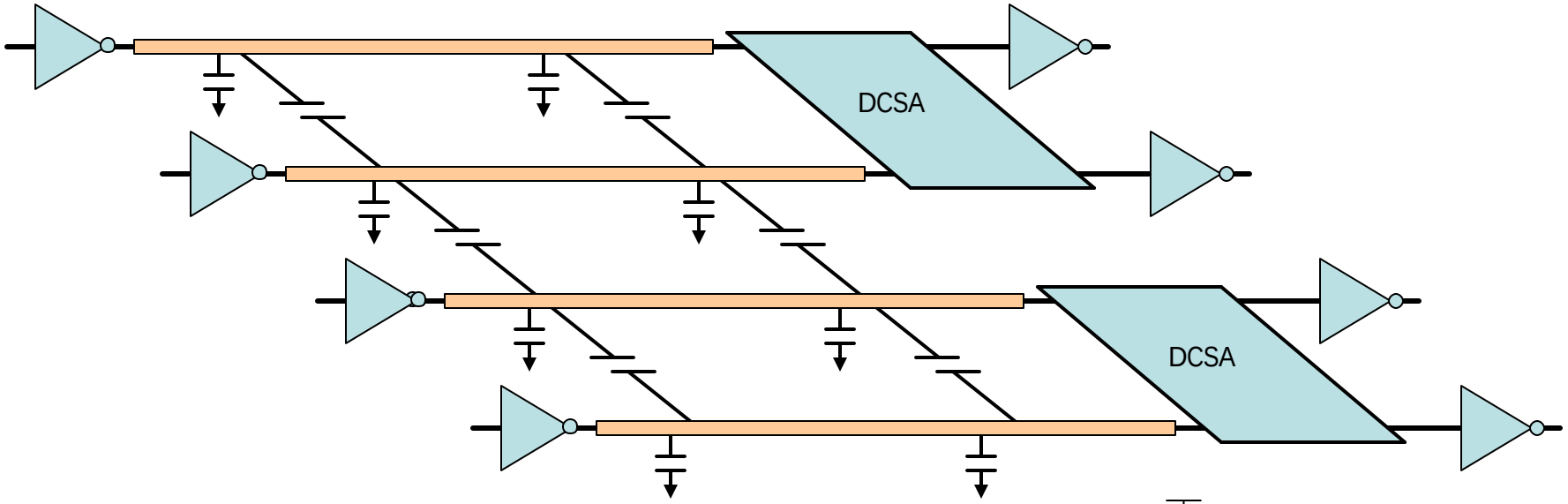
- Does not cut the line
- Bi-directional data flow

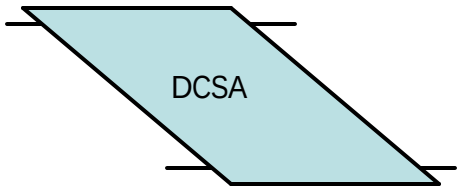
Differential current sensing*

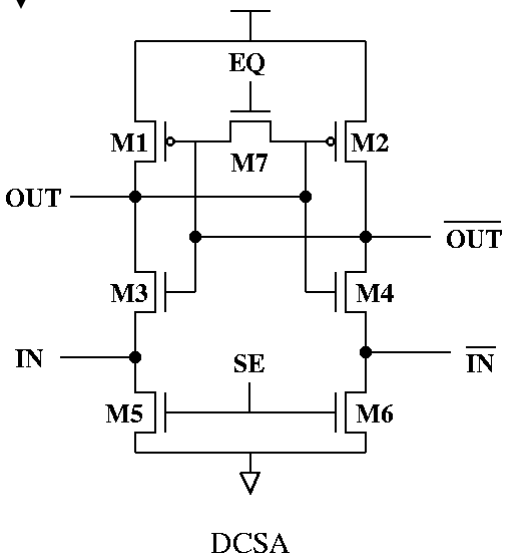


*Atul Maheshwari, Wayne Burleson, Current-sensing for Global Interconnects, Secondary Design Issues: Analy sis and Solutions, IEEE International Workshop on power and timing modeling, optimization and simulation, 2001

DCS

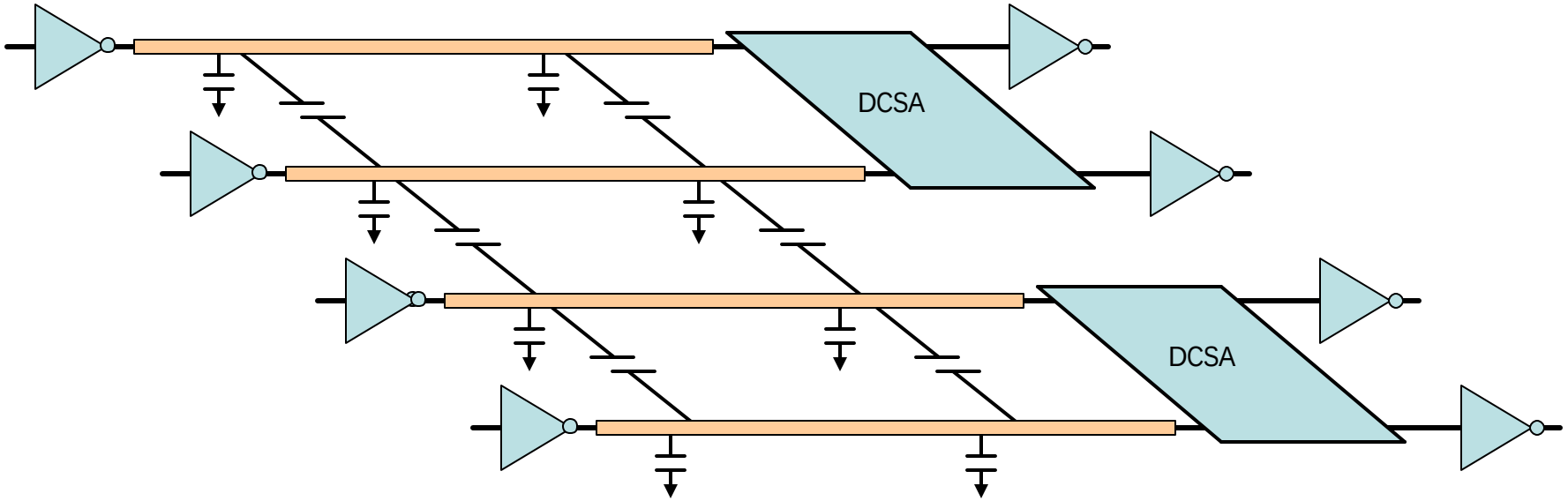






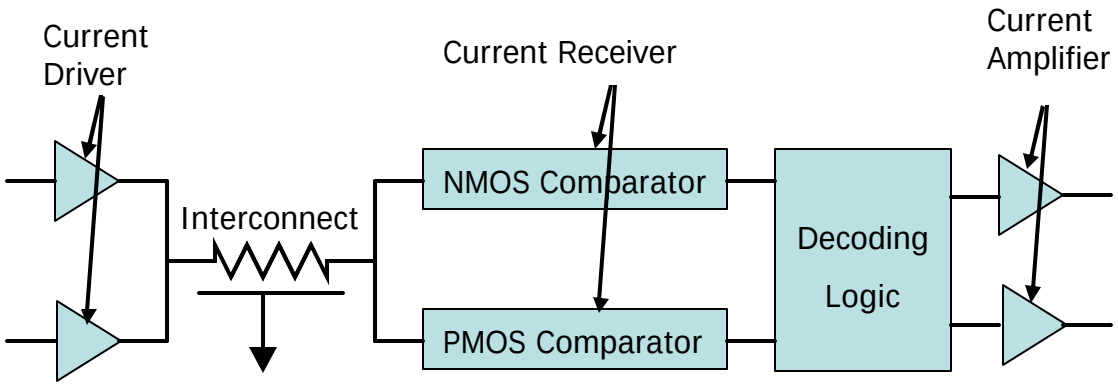
DCSA

Differential current sensing



- Differential signaling.
- Works well for highly capacitive wires.
- Orthogonal coupling not a problem since differential.

MLCS*



- Multi-level/Multi-bit signaling
- High throughput

Sriram Srinivasan, Multi-bit Signaling, chapters 3, 4, Master's Dissertation, Department of ECE, University of Massachusetts 2002

Advantages of NoC architectures

- Tiled architecture with mesh interconnect
- Point to point communication pipeline
- Allows for heterogeneous cores
  - Differing sizes, clock rates, voltages
- Regularity of the architecture eases interconnect design to a point to point communication.
- Allows for reuse of tiles.
- Regular repetition of similar wire segments which are easier to model as DSM interconnects.
- Allows the application of other high performance interconnect techniques including repeaters due to regularity in design.

NoCIC: A Spice-based Interconnect Planning Tool Emphasizing Aggressive On-Chip Interconnect Circuit Methods

V. Venkatraman, A. Laffely, J. Jang, H. Kukkamalla,
Z. Zhu & W. Burleson
Interconnect Circuit Design Group
Department of Electrical and Computer Engineering
University of Massachusetts Amherst
{vvenkatr}@ecs.umass.edu

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ICDG