ECE 636
Reconfigurable Computing
Lecture 11
Reconfigurable Computing Applications
Hardware assisted Simulated Annealing

- Use FPGA to perform FPGA placement
- Take advantage of parallelism and specialization
- Some limitations
  - Global view of cost
  - Convergence
  - Scalability
- Lots of benefits
  - Massive parallelism
  - Self-contained reconfigurable system

Courtesy: Wrighton/DeHon
Systolic Architectures

- Memory
- Compute
- Bottleneck

Compute
Memory
Compute
Memory
Compute
Memory
Compute
Memory
Compute
Strategy

- Reformulate simulated annealing allowing only local swaps
- Consider all swaps in parallel
- Maintain information in “systolic cells”
  - Represent current placement spatially
  - Construct hardware to operate on entire placement at once
Local Swaps

Local Communication

Local Swaps

Massively Parallel Operation
Individual Swap Element

- myID
- Fanin0(id, x, y)
- Fanin1(id, x, y)
- Fanin2(id, x, y)
- FaninN(id, x, y)
- Fanout0(id, x, y)
- Fanout1(id, x, y)
- Fanout2(id, x, y)
- Fanout2N(id, x, y)

- Left data in
- Left data out
- Position chain in
- Position chain out
- Right data in
- Right data out
- Up data in/out
- Down data in/out

- Randomness
- Arithmetic Unit
- PosChain(id, x, y)
- counter
- myX, myY
Linear Wirelength Improvement

Apex4 Benchmark

![Graph showing linear wirelength improvement](image-url)
Choosing 400 Cooling Steps

Normalized Linear Wirelength Metric vs. swapsPerInterval for various benchmarks.

- alu4.net
- apex2.net
- apex4.net
- bigkey.net
- clma.net
- des.net
- diffeq.net
- dsip.net
- elliptic.net
- ex1010.net
- ex5p.net
- frisc.net
- misex3.net
- pdc.net
- s298.net
- s38417.net
- s38584.1.net
- seq.net
- spla.net
- seq.net
- tseng.net
VPR Comparison Methodology

Netlists from FPGA Place and Route Challenge

Placed Design

vpr -fast Placer

Routed Design

vpr Router

Placed Design

Systolic Placement Algorithm

Routed Design

vpr Router

Configuration Options

Record Statistics (channel utilization, critical path delay)
Speedups

- VPR on 2.2 GHz Xeon Workstation
- 500x for ex5p
  - 18% channel growth
- 1200x for spla
  - 41% channel growth
- More opportunity for speedups with better cooling schedules
- Better quality with better cost functions
- Feasible on a Virtex2000E part
Networking Application: Reconfigurable Firewall

- Networking hardware well suited for reconfigurable hardware
  - Target signatures change often
  - Massive quantities of stream-based data
  - Repetitive operations

- Connecting up to a realistic networking environment is hard
  - Washington University experimental setup one of the best
  - Shows importance of both memory and processing capability

- Numerous experiments performed over the past five years

Courtesy: Lockwood
Network Routing

- FPGAs popular in network hardware
- New protocols implemented directly in silicon
- Easy to upgrade in the field
- Washington University Gigabit Switch (WUGS)
  - Switch provides up to 160 Gbps of bandwidth.
FPGA-based Router

- FPX module contains two FPGAs
- NID – network interface device
  - Performs data queuing
- RAD – reprogrammable application device
  - Specialized control sequences

Figure 4: FPX Printed Circuit Board
Reconfigurable Data Queuing

- Data may be congested.
- FPGA can be programmed for virtual channels.
Hardware Setup

- Stacked boards part of system
- Scalable to multiple boards
- Allows for cooling, power.

Figure 2: Original configuration of WUGS backplane with line card (side view)
IP Lookup Function

- RAD can be used to evaluate packet headers.
- Headers evaluated in groups of four bits
FPX Hardware in WUGS-20 Switch
System-On-Chip Firewall

Xilinx XCV2000E FPGA

Payload Scanner
TCAM Filter
Extensible Module(s)
Flow Buffer
Queue Manager
Packet Scheduler

Interfaces to Off-Chip Memories

SDRAM 2 Controller
SDRAM 1 Controller
Free List Manager
SRAM 1 Controller

Payload Match Bits
Flow ID

Data input from Gigabit Ethernet or SONET Line Card

Data output to switch, Gigabit Ethernet, or SONET Line Card

Layered Protocol Wrappers
Content Matching Module

From Protocol Wrappers

dataen_out_appl
   d_out_appl
   sof_out_appl
   eof_out_appl
   sod_out_appl
   tca_out_appl

regex_app (given)

32

To existing MP1 circuit

dataen_appl_in
d_appl_in
sof_appl_in
eof_appl_in
sod_appl_in
tca_appl_in

8

To extended Bits of CAM

Matched
ready_l

clk
reset_l
enable_l

wrapper_module.vhd
Packet matching w/ Content Addressable Memory

Sample Packet:
- Source Address = 128.252.5.5 (dotted.decimal)
- Destination Address = 141.142.2.2 (dotted.decimal)
- Source Port = 4096 (decimal)
- Destination Port = 50 (decimal)
- Protocol = TCP (6)
- Payload = “Consolidate your loans. CALL NOW”
  - Payload Lists = { General SPAM (0), Save Money SPAM (1) }
  - Content Vector = “00000011” (binary) = x”03” (hex)
Sample Filter

- Source Address = 128.252.0.0 / 16
- Destination Address = 141.142.0.0 / 16
- Source Port = Don’t Care
- Destination Port = 50
- Protocol = TCP (6)
- Payload includes general SPAM (List 0)

DROP the packet: It matches the filter
Packet Classifier with FlowID

Flow ID

Resulting Flow Identifier

Flow List

Priority Encoder

Mask Matchers

Value Comparators

Payload Match Bits

Source Address

Destination Address

Source Port

Destination Port

Protocol

Bits in IP Header

--- CAM Table ---

CAM MASK [1]

CAM VALUE [1]

CAM MASK [2]

CAM VALUE [2]

CAM MASK [3]

CAM VALUE [3]

CAM MASK [N]

CAM VALUE [N]
Other Modules Implemented

° IPv6 Tunneling Module
  • Tunnels IPv6 over IPv4

° Statistics Module
  • Event counter

° Fast IP Lookup (FIPL)
  • Longest Prefix Match
  • MAE-West at 10M pkts/second

° Traffic Generator
  • Per-flow mixing

° Packet Content Scanner
  • Reg. Expression Search

° Video Recoder
  • Motion JPEG

° Embedded Processor
  • KCPSM

° Data Queueing
  • Per-flow queue in SDRAM

° IPv4 CAM Filter
  • 104 Bit header matching