
ECE 636

Reconfigurable Computing

Lecture 3

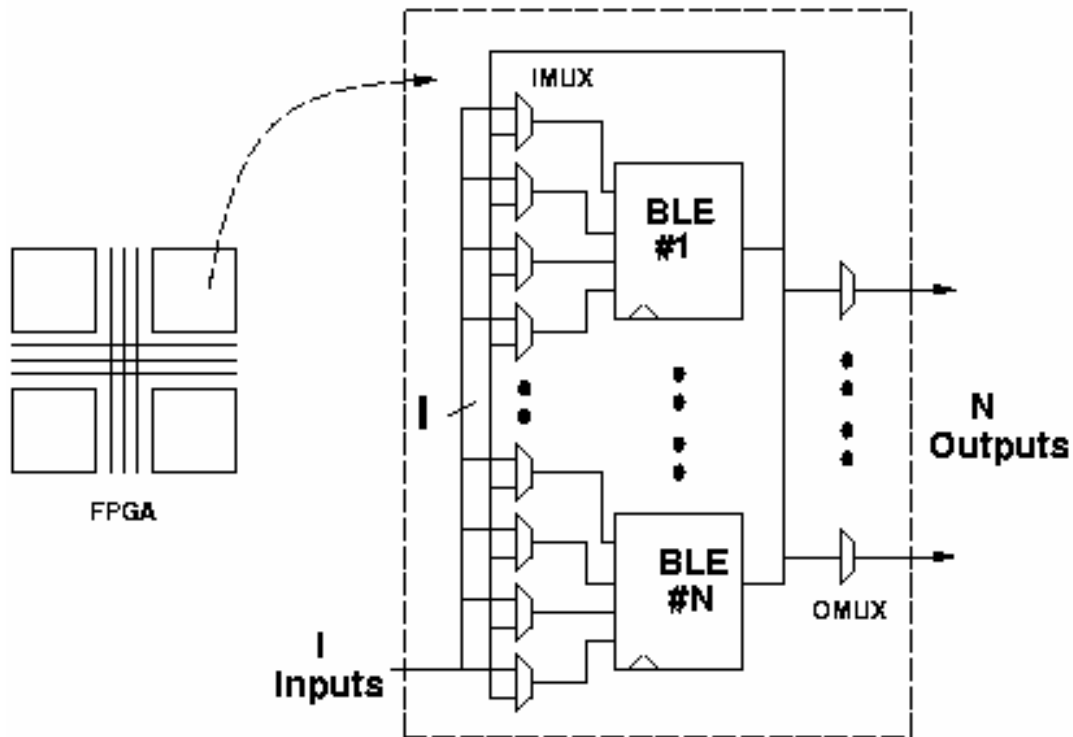
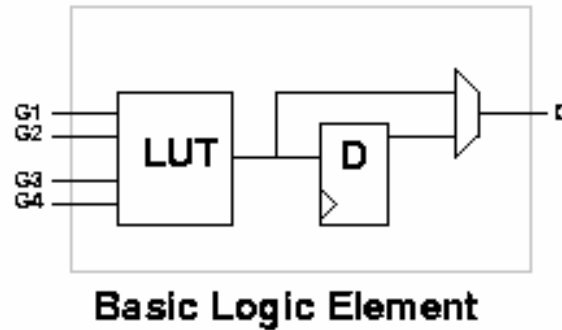
Field Programmable Gate Arrays II



Overview

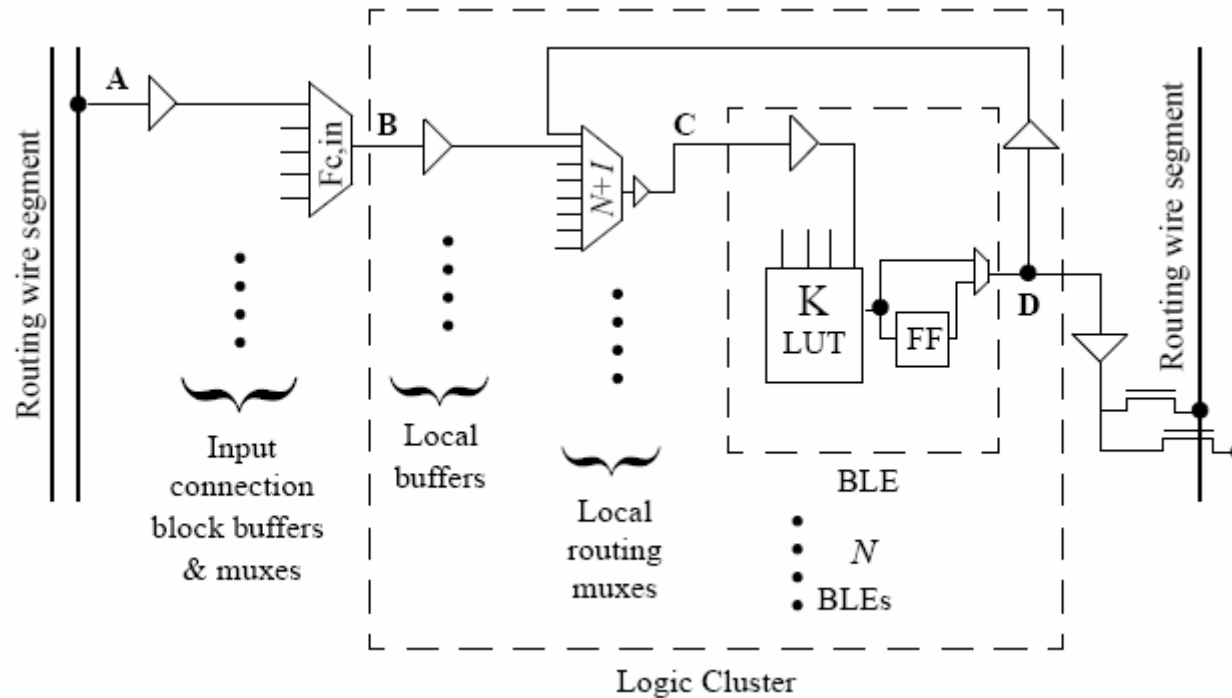
- **Anti-fuse and EEPROM-based devices**
- **Contemporary SRAM devices**
 - **Wiring**
 - **Embedded**
- **New trends**
 - **Single-driver wiring**
 - **Power optimization**

Architectural Issues – Ahmed and Rose



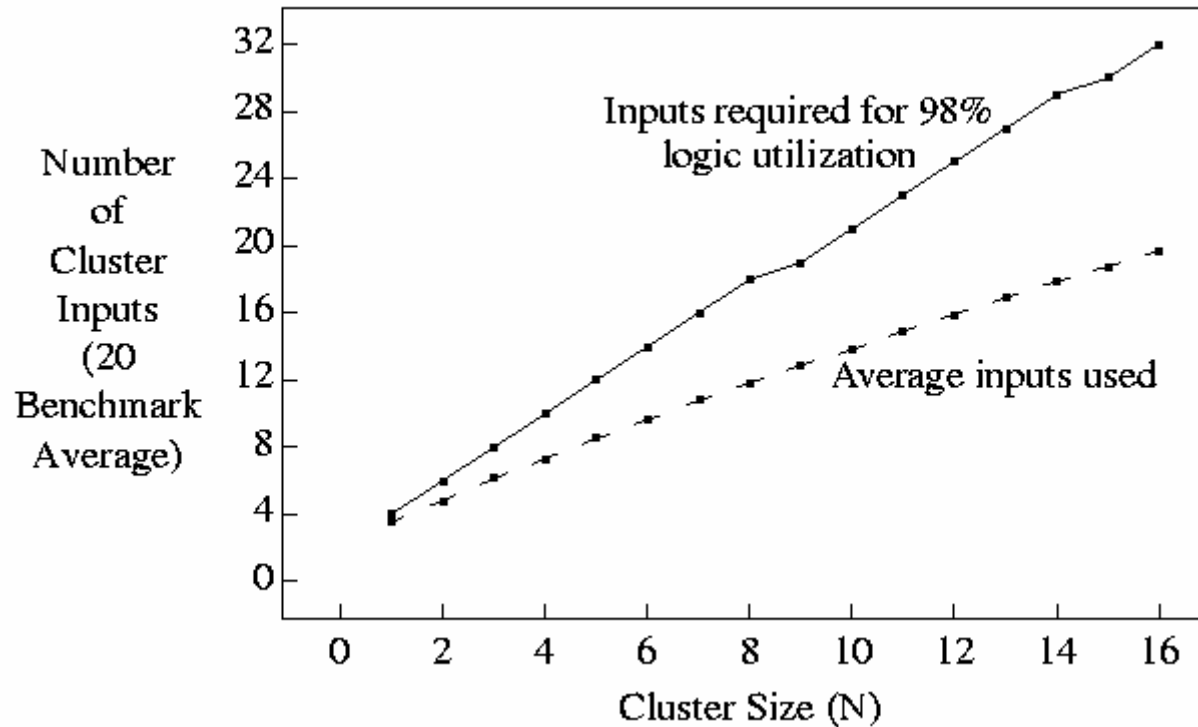
- What values of N , I , and K minimize the following parameters?
 - Area
 - Delay
 - Area-delay product
- Assumptions
 - All routing wires length 4
 - Fully populated IMUX
 - Wiring is half pass transistor, half tri-state
 - 180 nm
 - Routing performed with $W_{\min} + 30\%$ tracks

Architectural Issues – Ahmed and Rose



- **Differences from modern commercial FPGAs**
 - Channel wires driven by muxes
 - Limited intra-cluster mux population
 - Carry chain/other circuitry
- **Still provides interesting analysis**

Number of Inputs per Cluster



- Lots of opportunities for input sharing in large clusters (Betz – CICC'99)
- Reducing inputs reduces the size of the device and makes it faster.
- $I = K/2 * (N + 1)$

Effect of N and K on Area

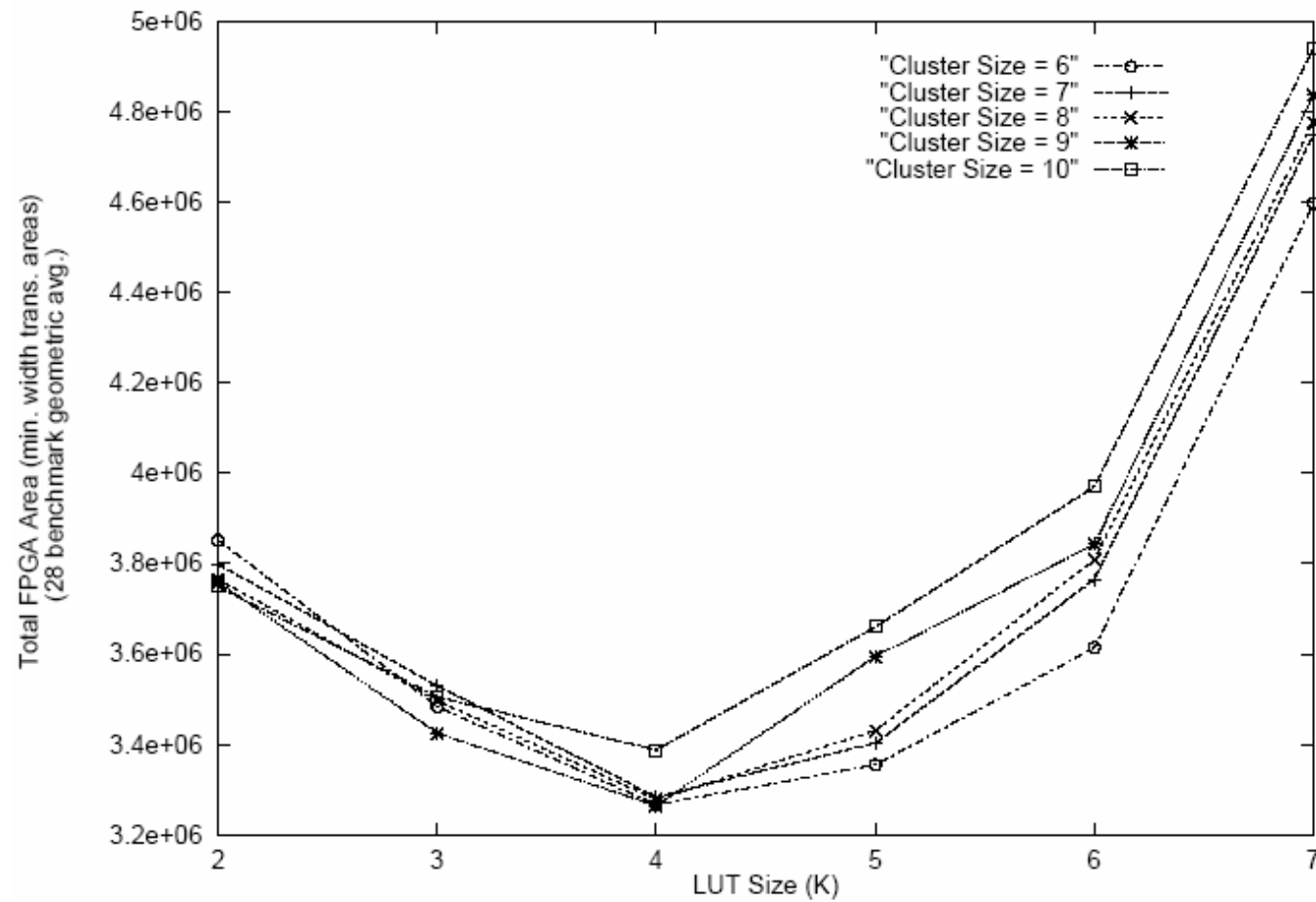
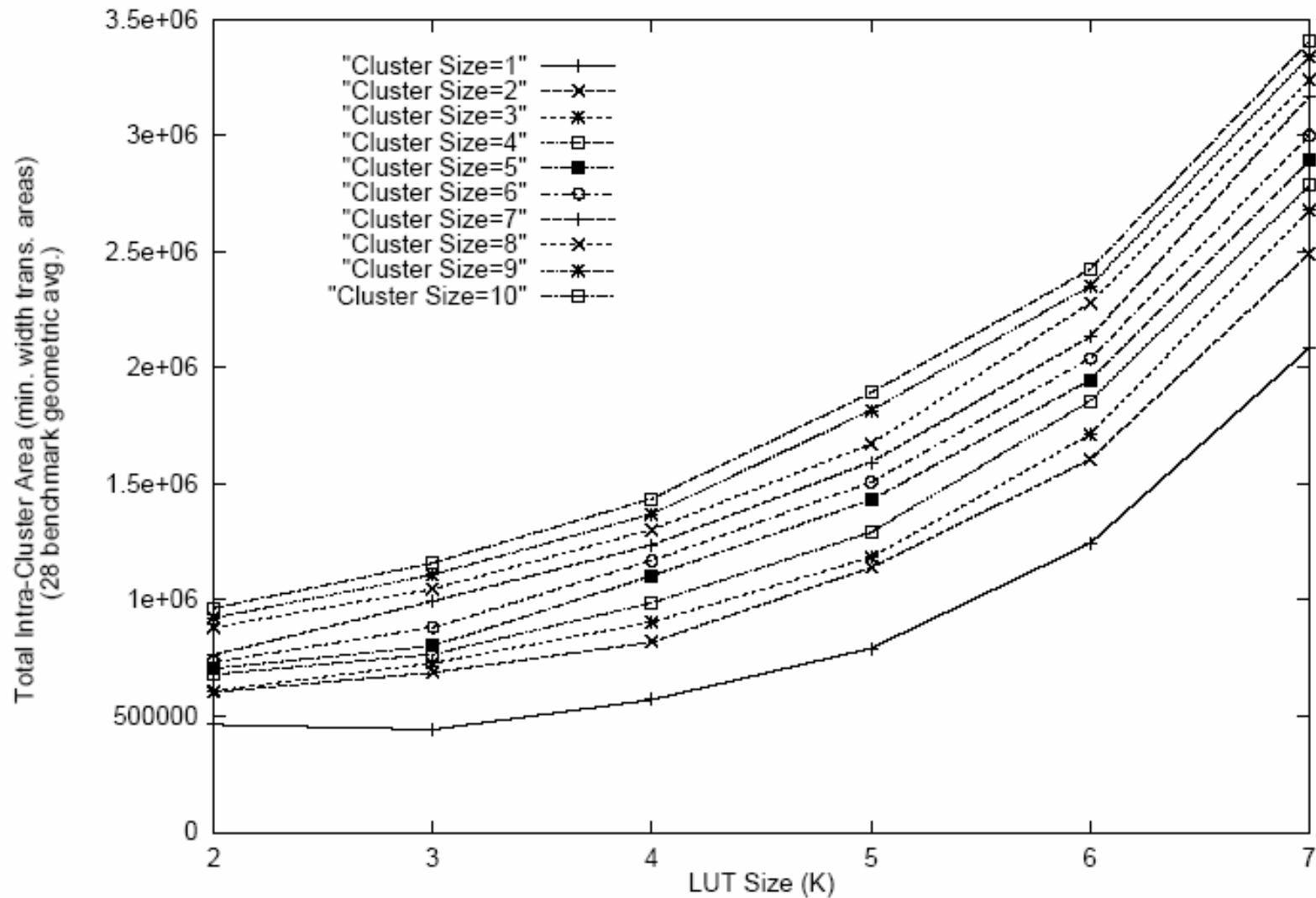


Fig. 8. Total Area for Clusters of Size 6 to 10

Looks like cluster size $N = 6-8$ is good, $K = 4-5$

Effect of N and K on Area

Intra-cluster area



Effect of N and K on Area

Inter-cluster area

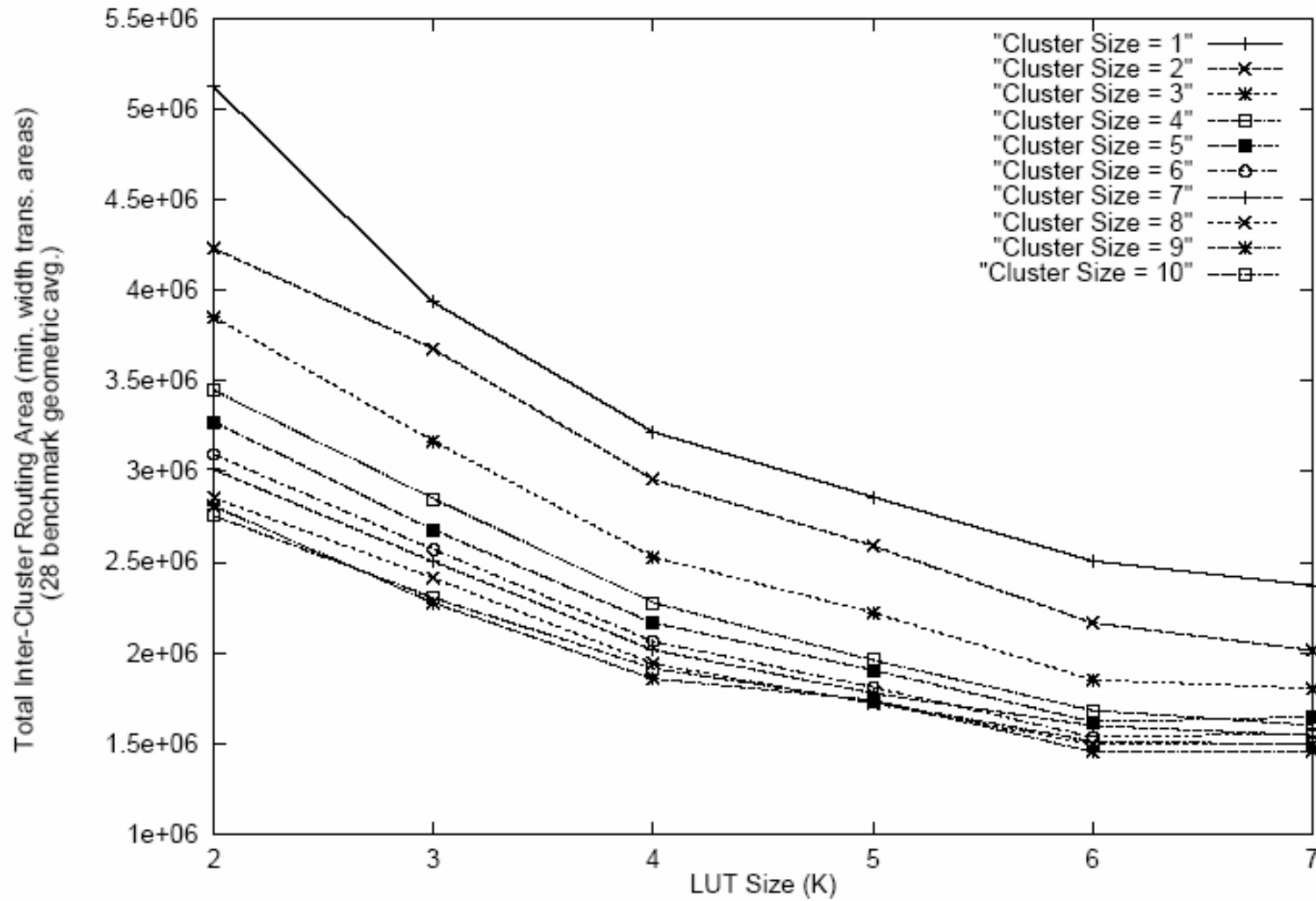


Fig. 12. Inter-Cluster Routing Area

Effect of N and K on Performance

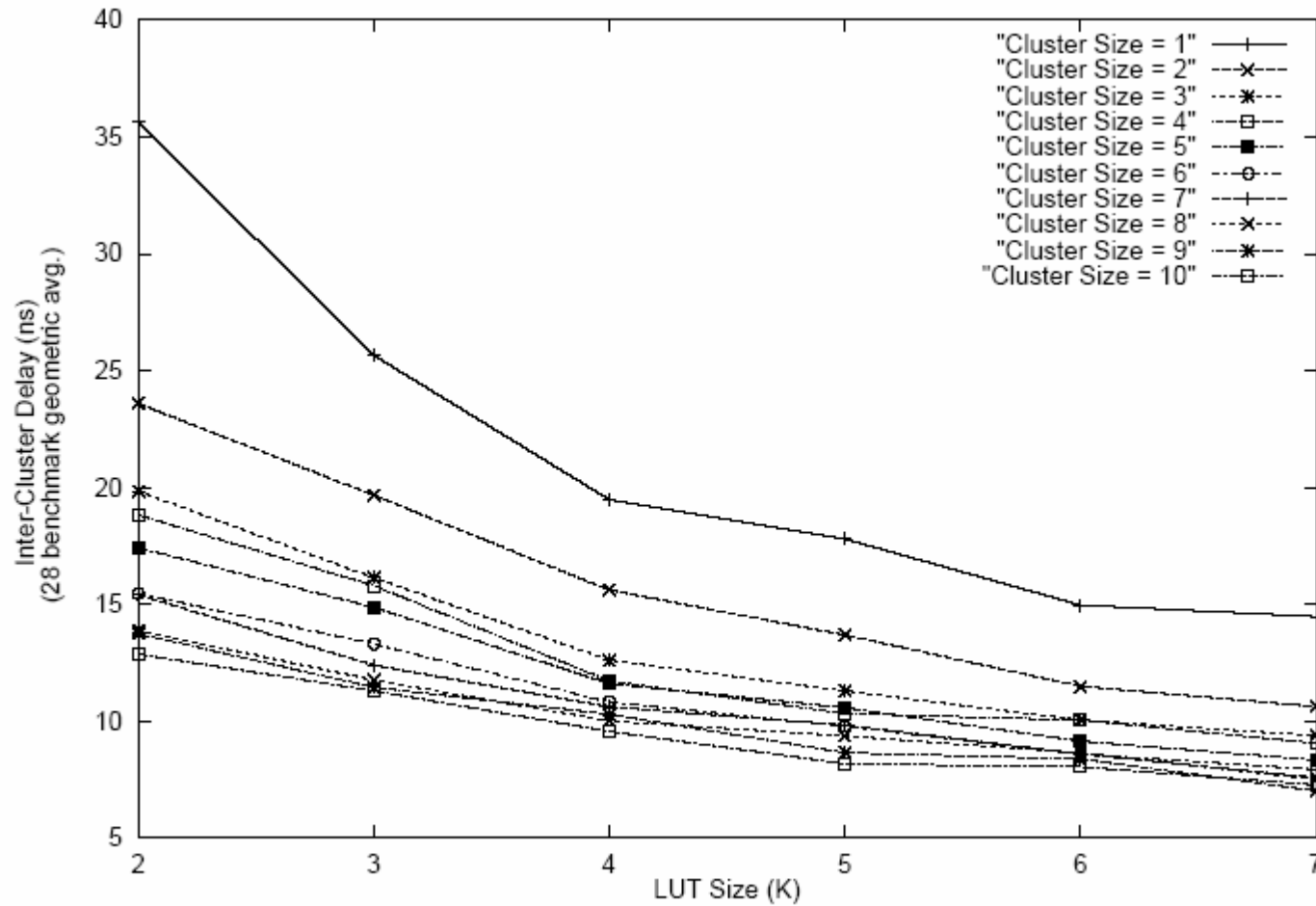


Fig. 17. Total Inter-Cluster Delay for Clusters of Size 1 to 10

Inconclusive: Big K and $N > 3$ value looks good

Effect of N and K on Area-delay product

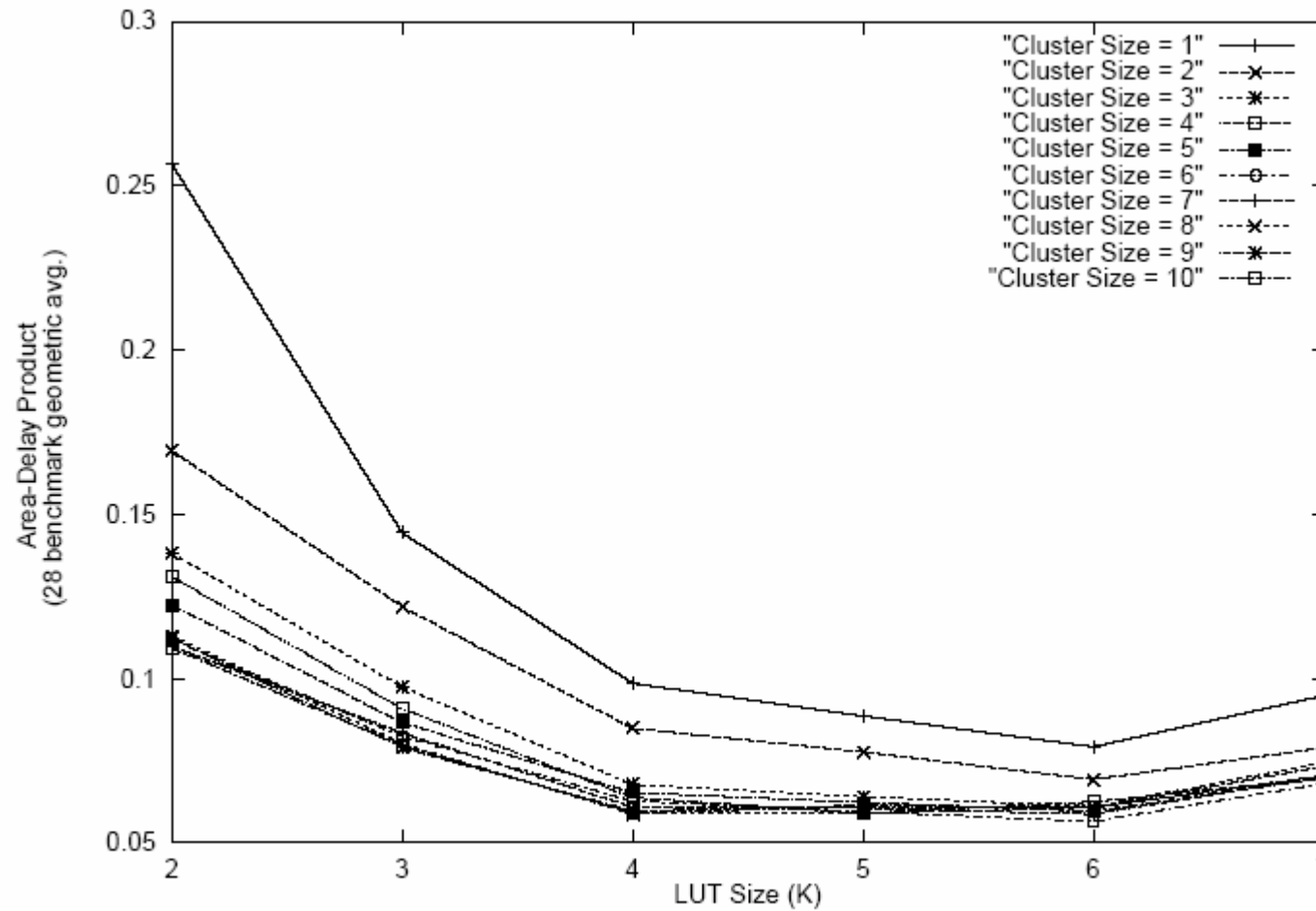


Fig. 20. Area-Delay Product for Clusters of Size 1 to 10

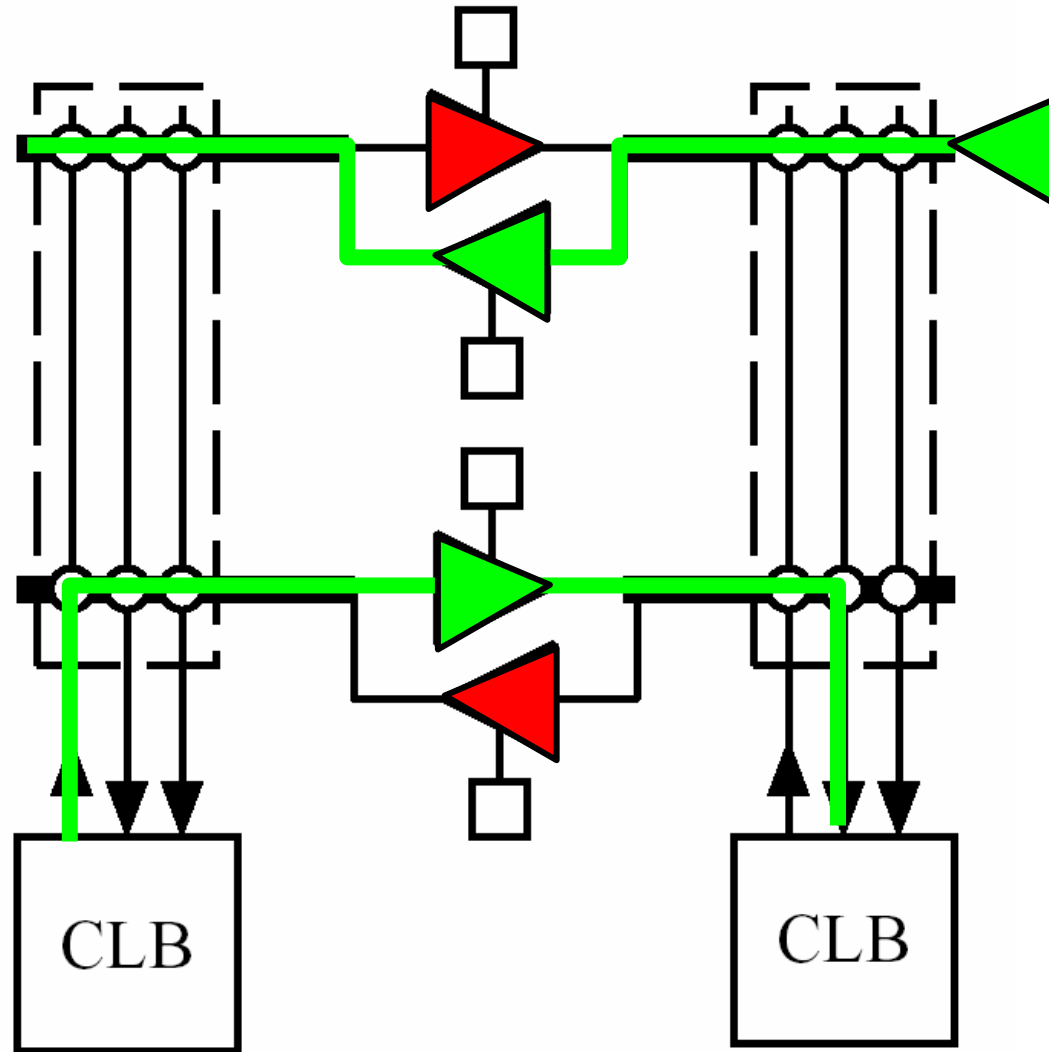
K = 4-6, N= 4-10 looks OK

Motivation: Bidirectional Wires

Problem

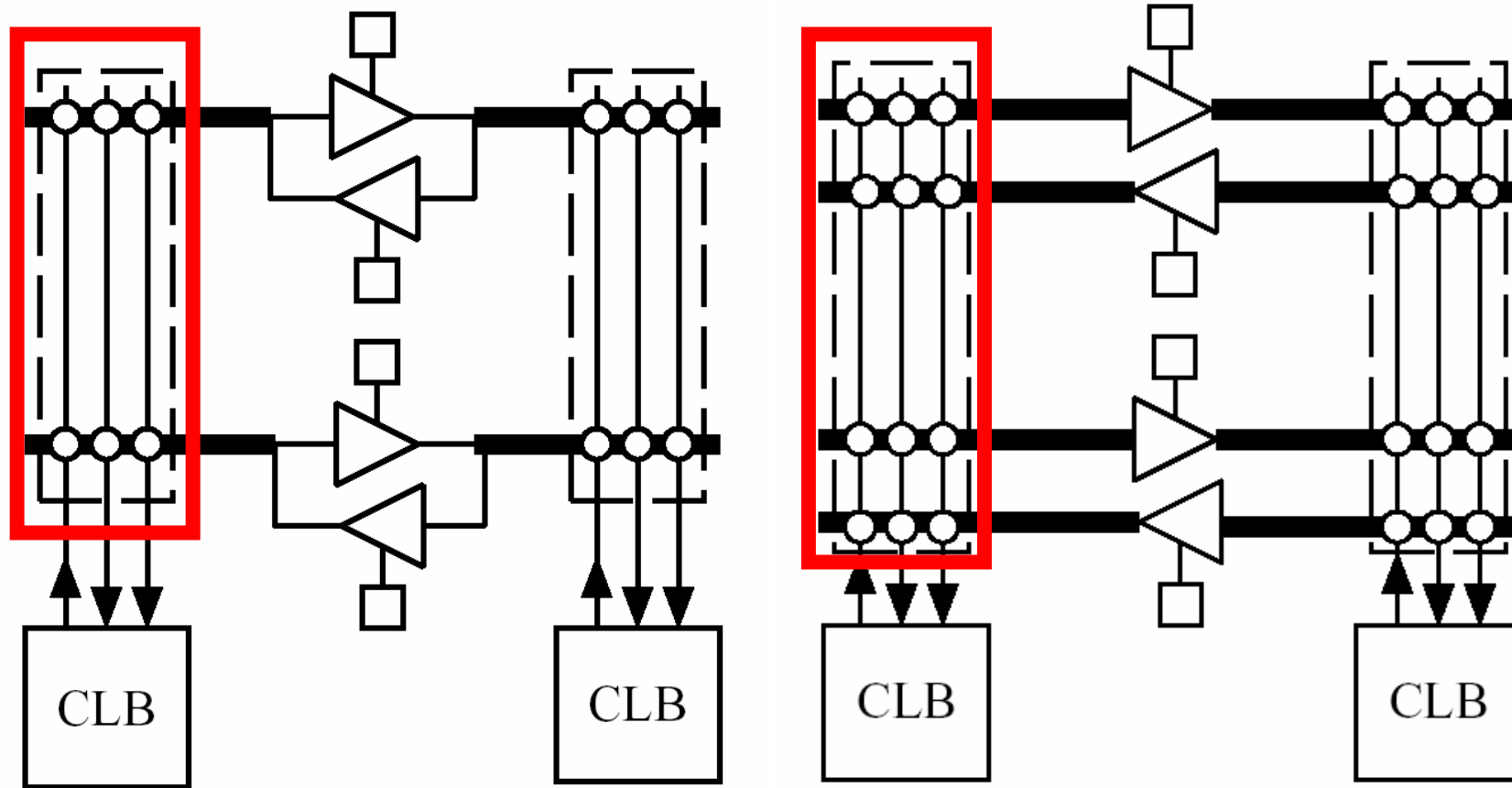
Half of
**Tristate
Buffers** Left
Unused

Buffers
Dominate
Size of
Device

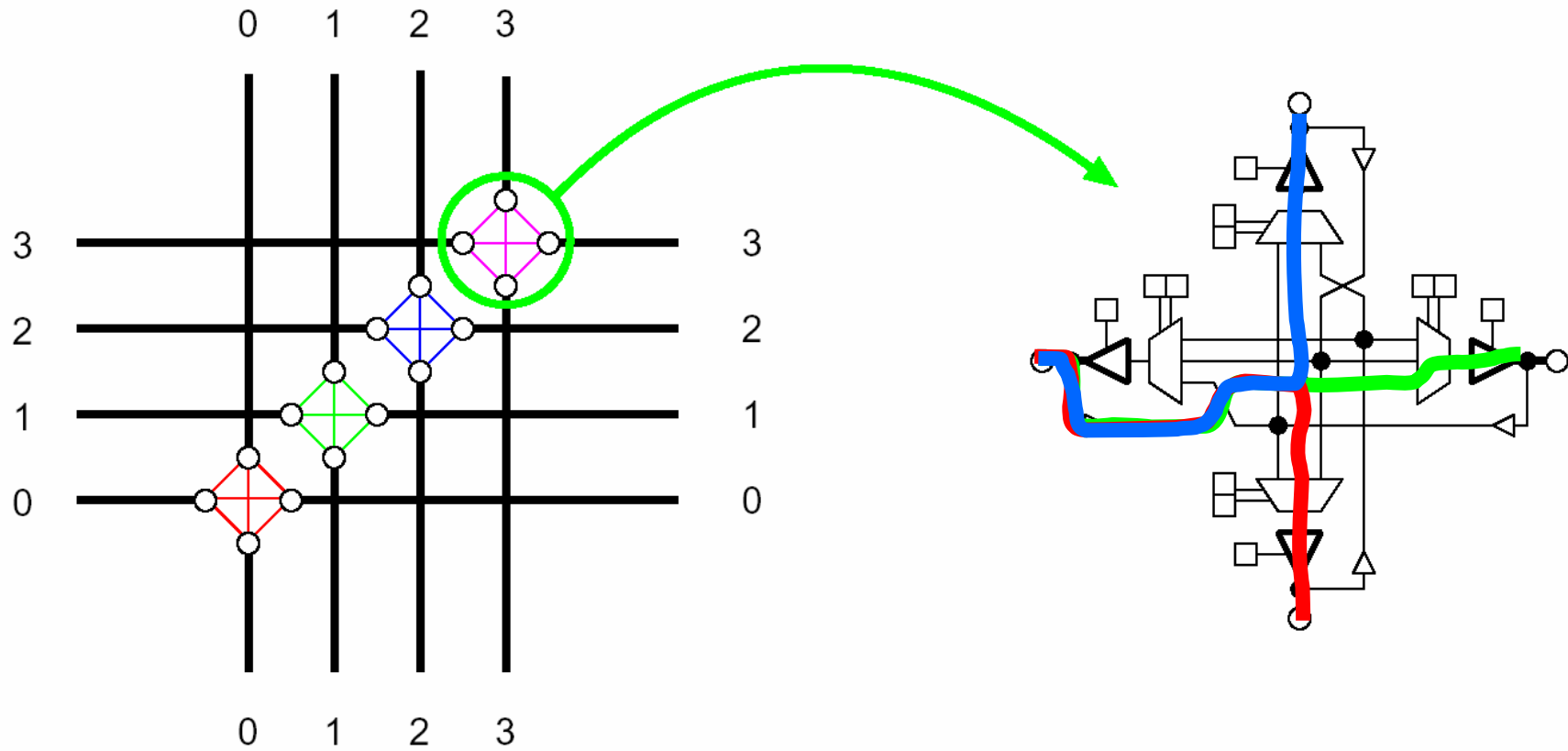


Courtesy: Lemieux

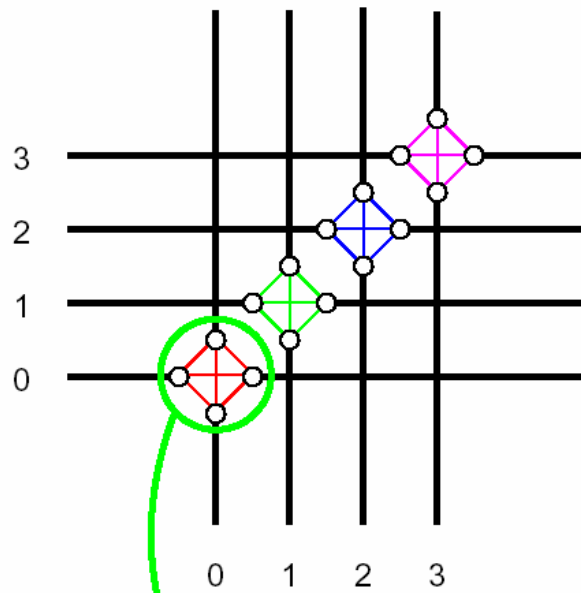
Bidirectional vs Directional



Bidirectional Switch Block

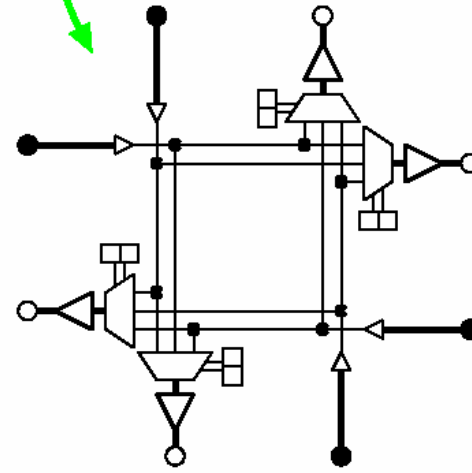
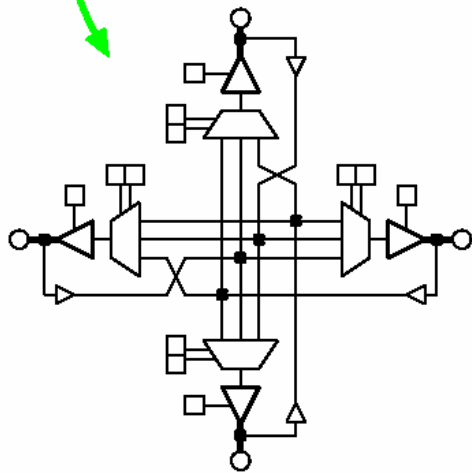
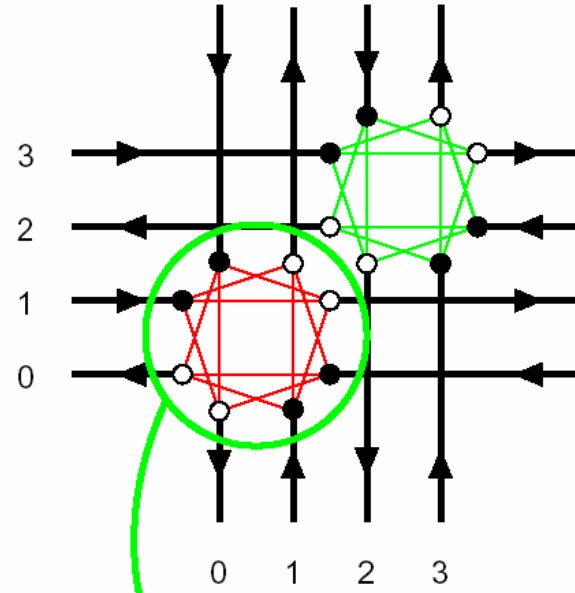


Directional versus Bidirectional Switch Block

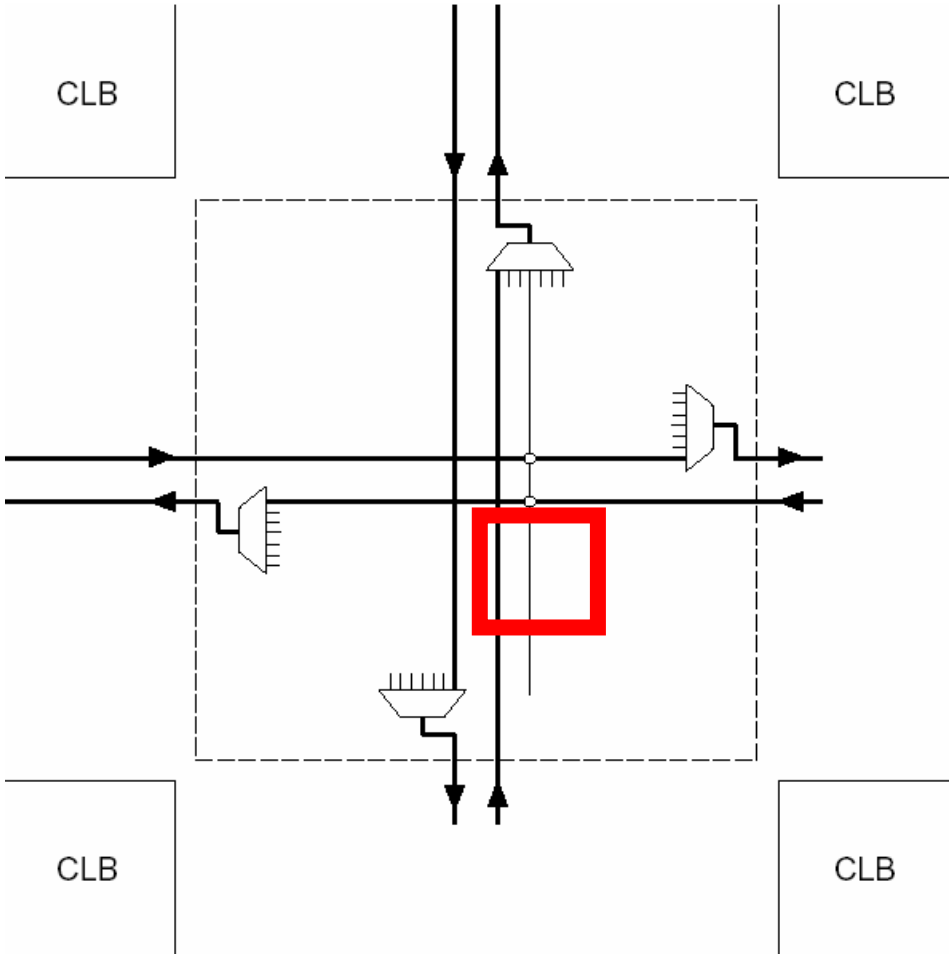


Switch Block:

Directional has **Half as Many** Switch Elements

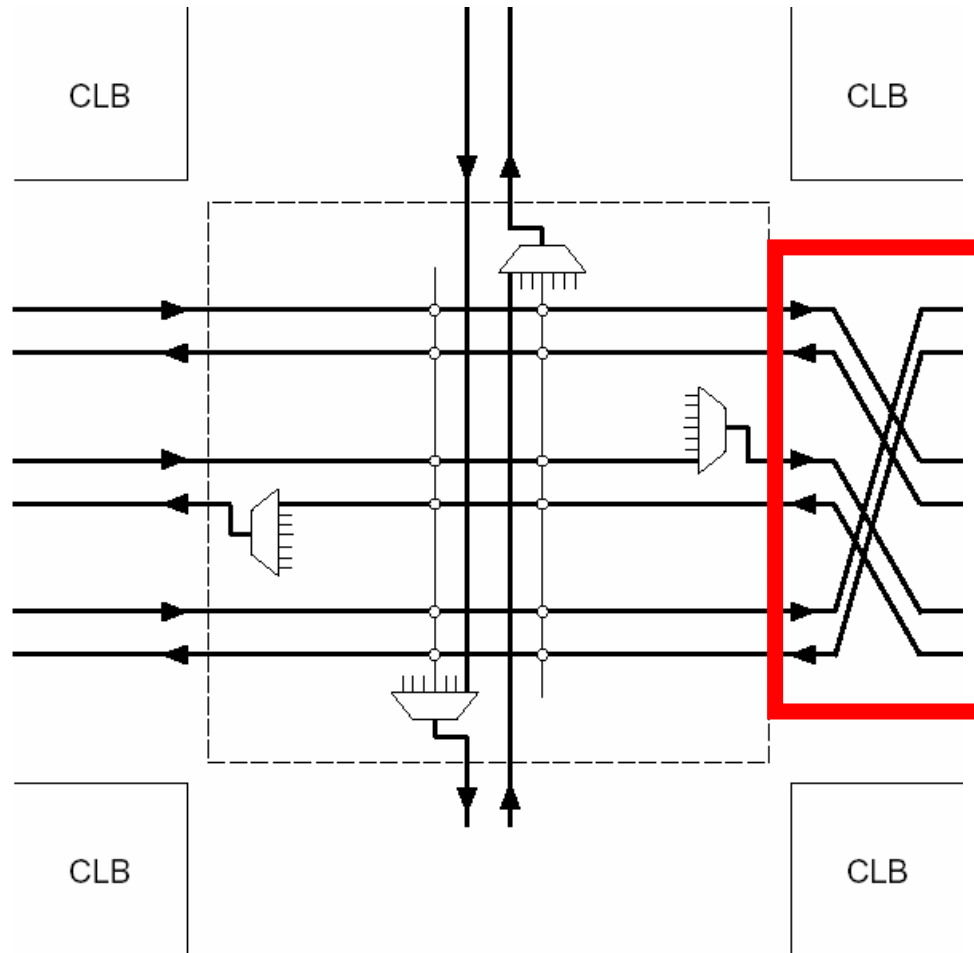


Building up Long Wires **Connect MUX Inputs**



TURN UP from wire-ends to mux

Building up Long Wires



Add wire twisting

Directional Wire Summary

◦ Pros and Cons

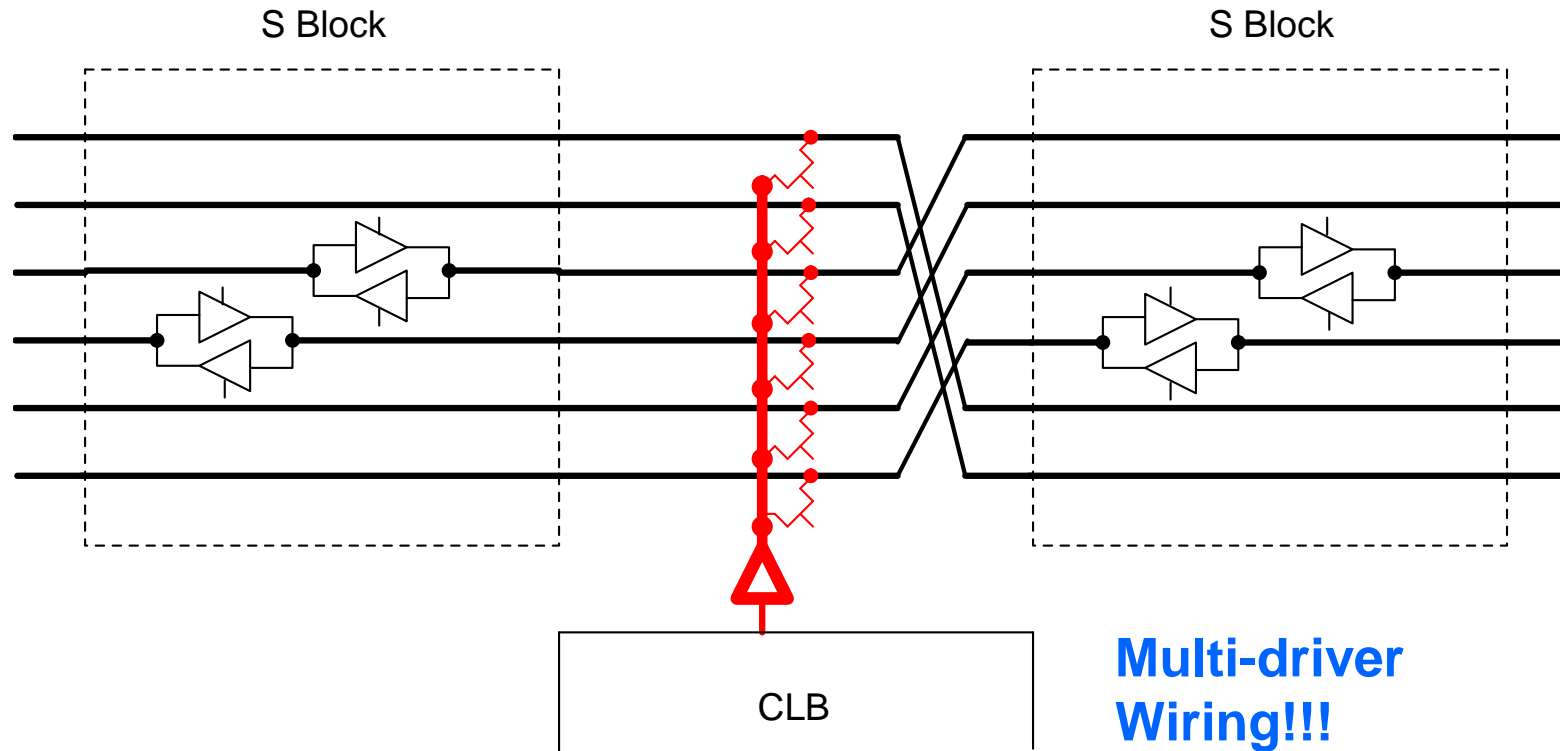
- **Good**

- **Potential area savings**
- **What does this do to CAD tools?**

- **Bad**

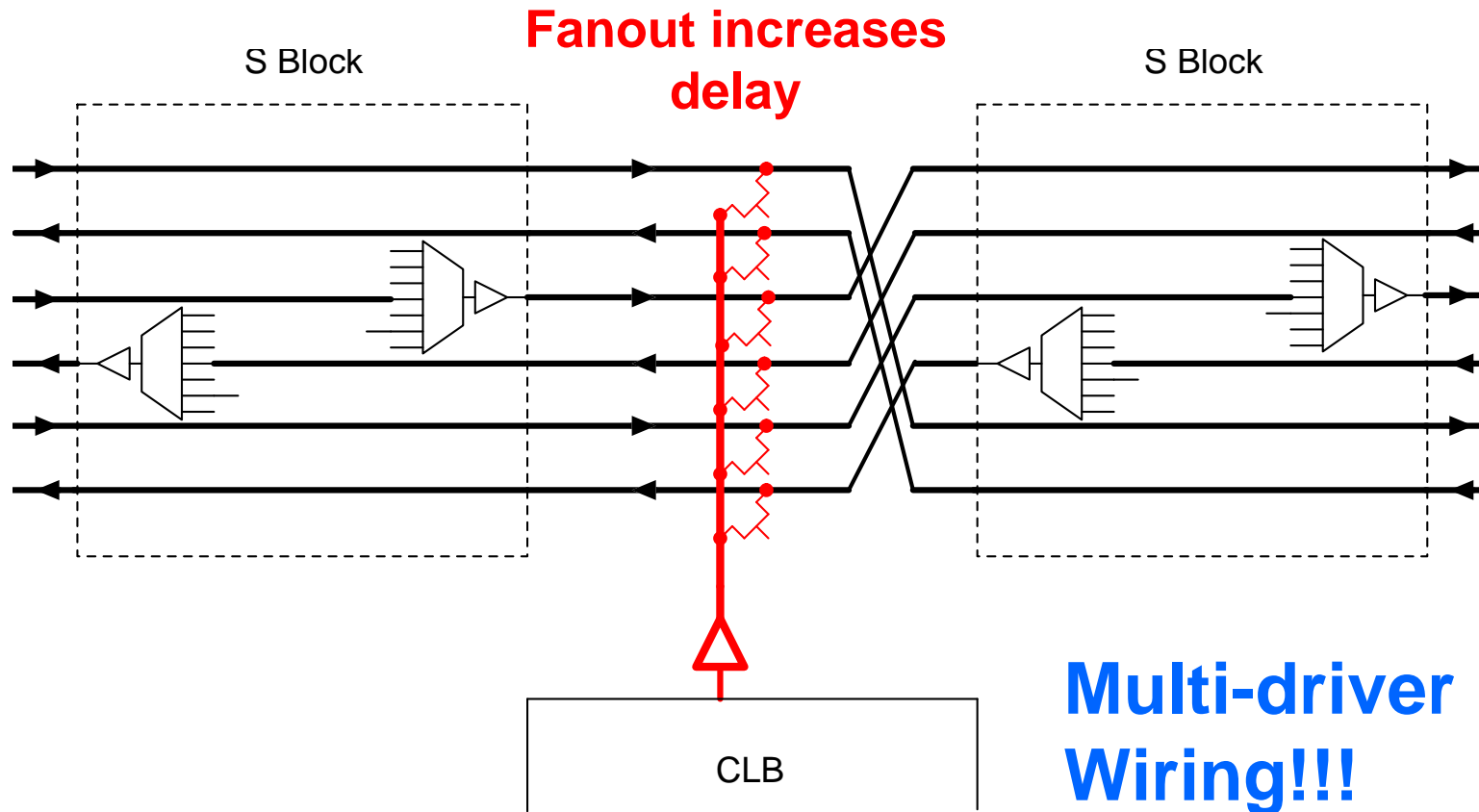
- **Big input muxes, slower**
- **Bigger quantum size (2*L)**
- **Detailed-routing architecture is different (need new switch block)**

Bidirectional Wiring: Outputs are Tristates



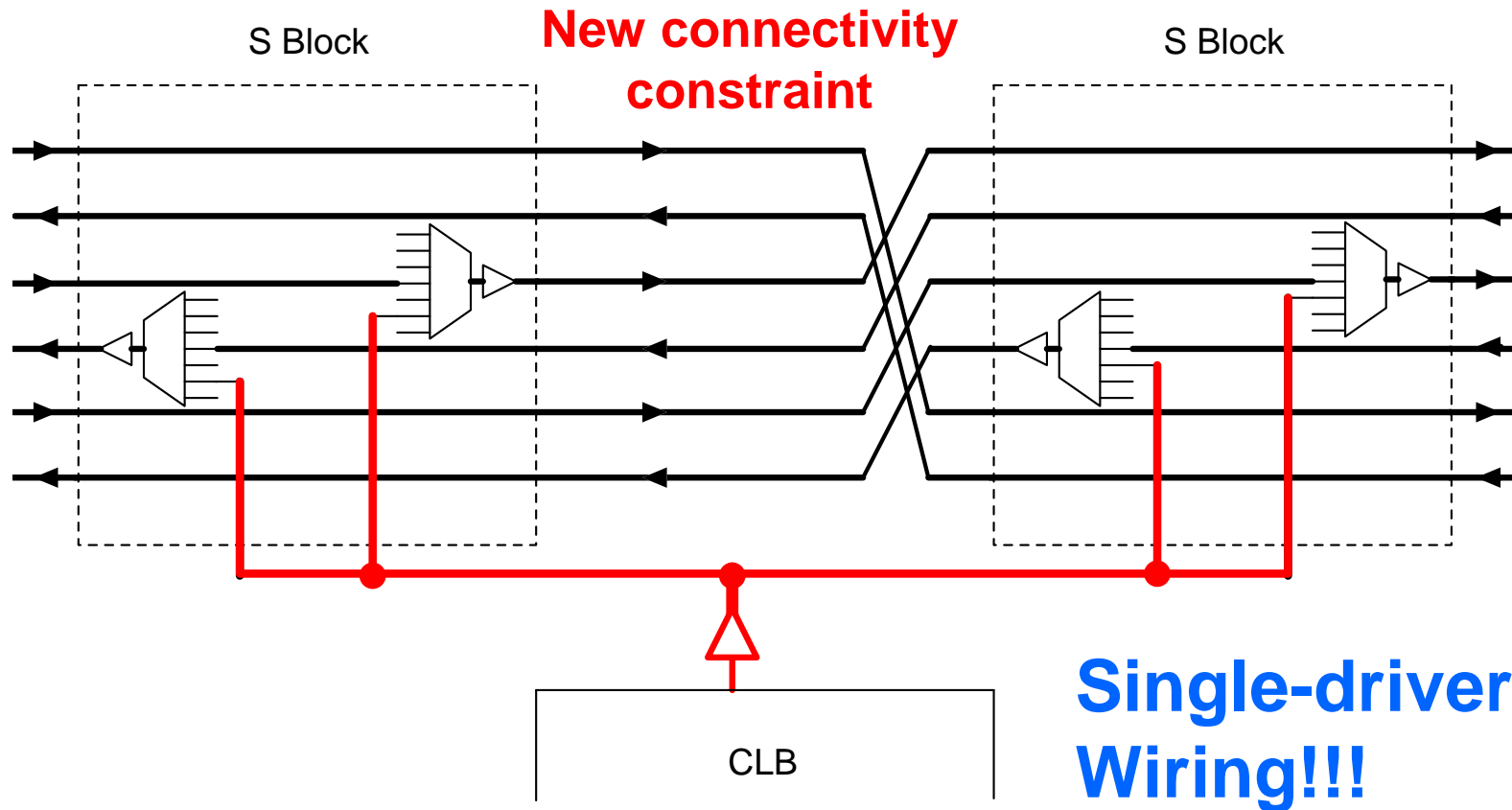
Bidir Architecture

Directional Wiring: Outputs **can be** Tristates



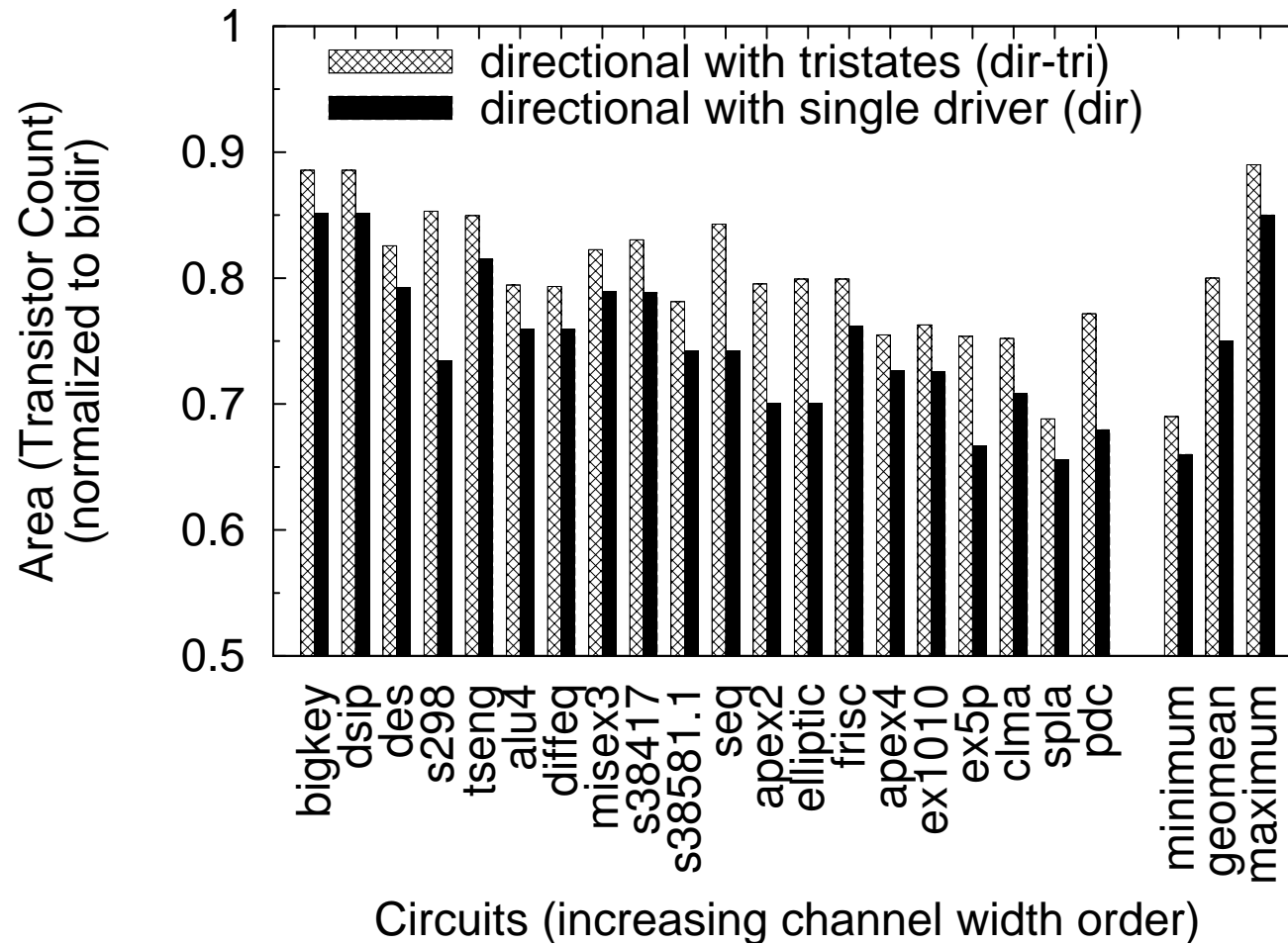
Dir-Tri Architecture

Directional Wiring: Outputs **can use** switch block muxes

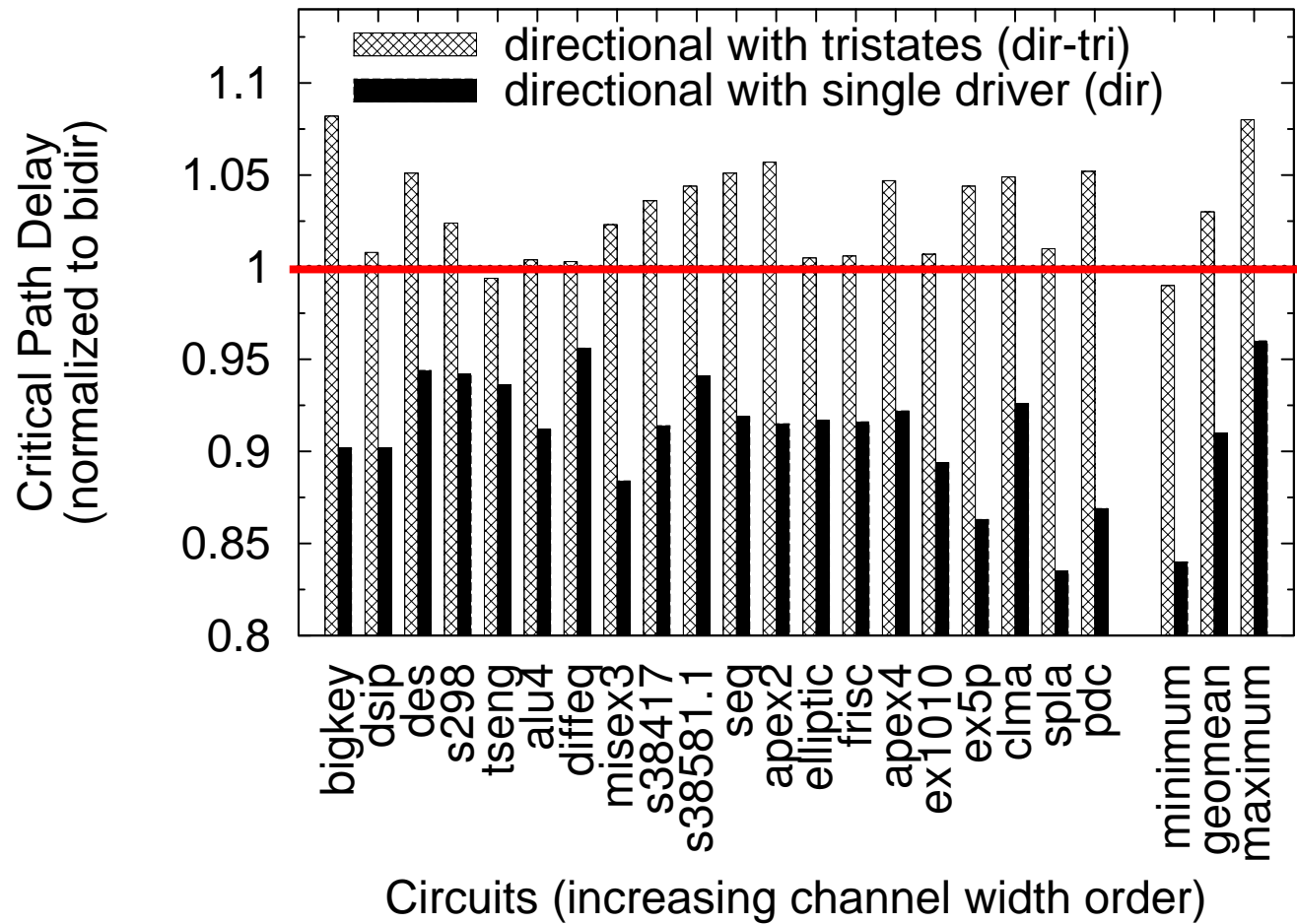


Dir Architecture

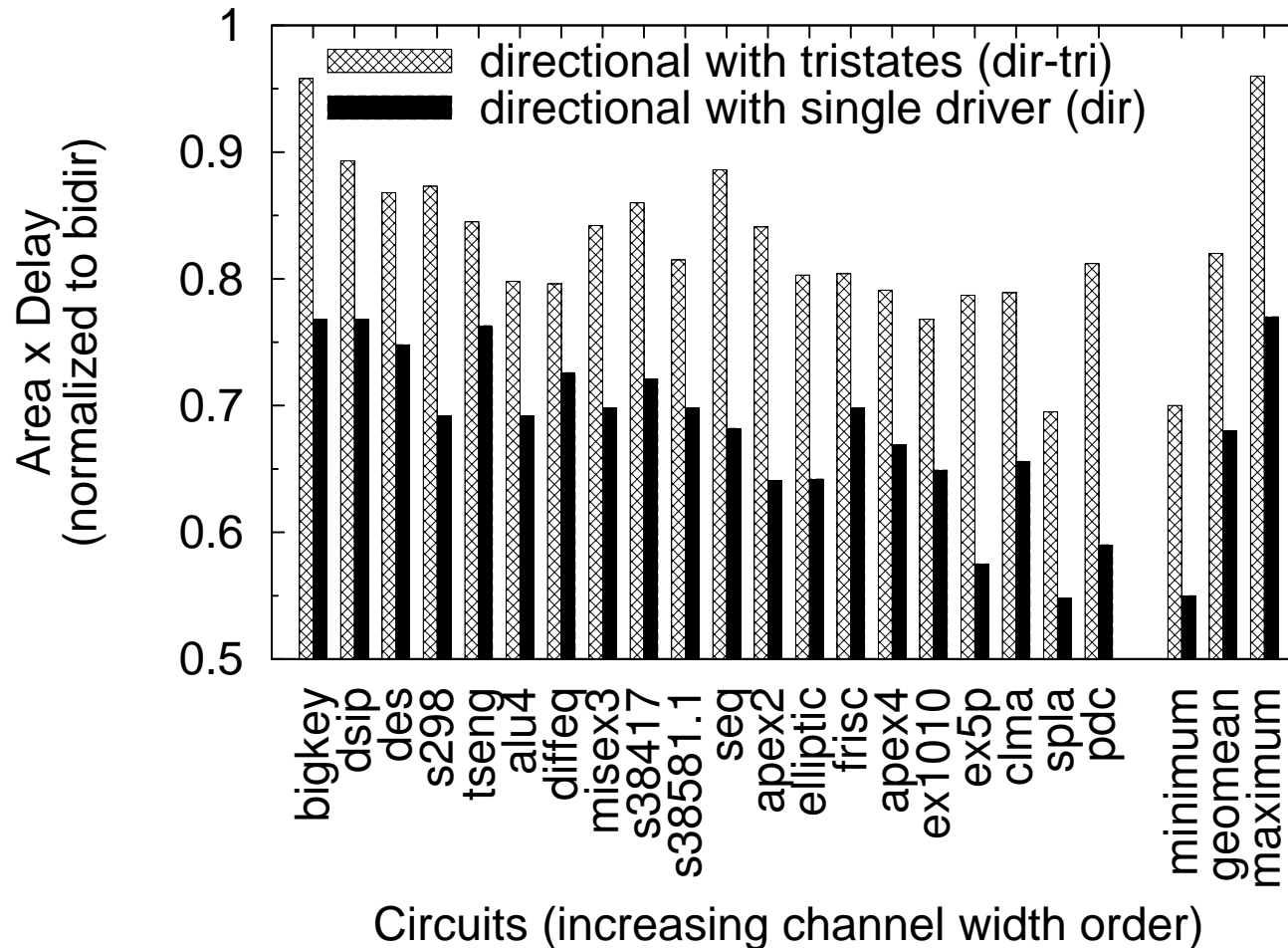
Area (Transistor Count)



Delay



Area-Delay Product



Stratix II paper

◦ Goals

- Improve device performance by ~50% (24% achieved from process shrink)
- Reduce area by ~50% (40% achieved from process shrink)

◦ Process (90 nm – down from 130 nm for Stratix)

◦ Use Ahmed results to explore larger LUT size

◦ Look into fast routing

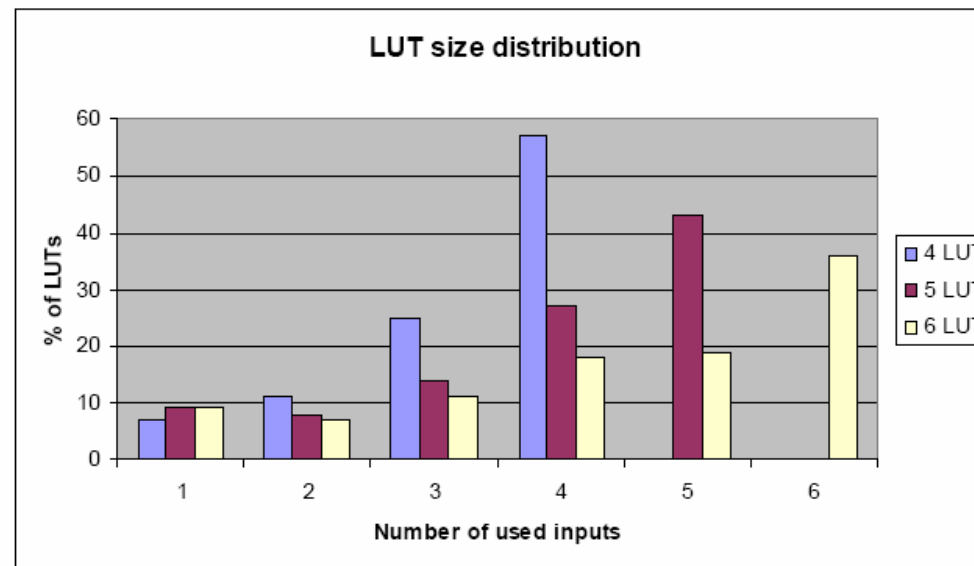


Figure 3: LUT input pin usage distribution

First 6-LUT Option – Composable LUT

- Lots of issues

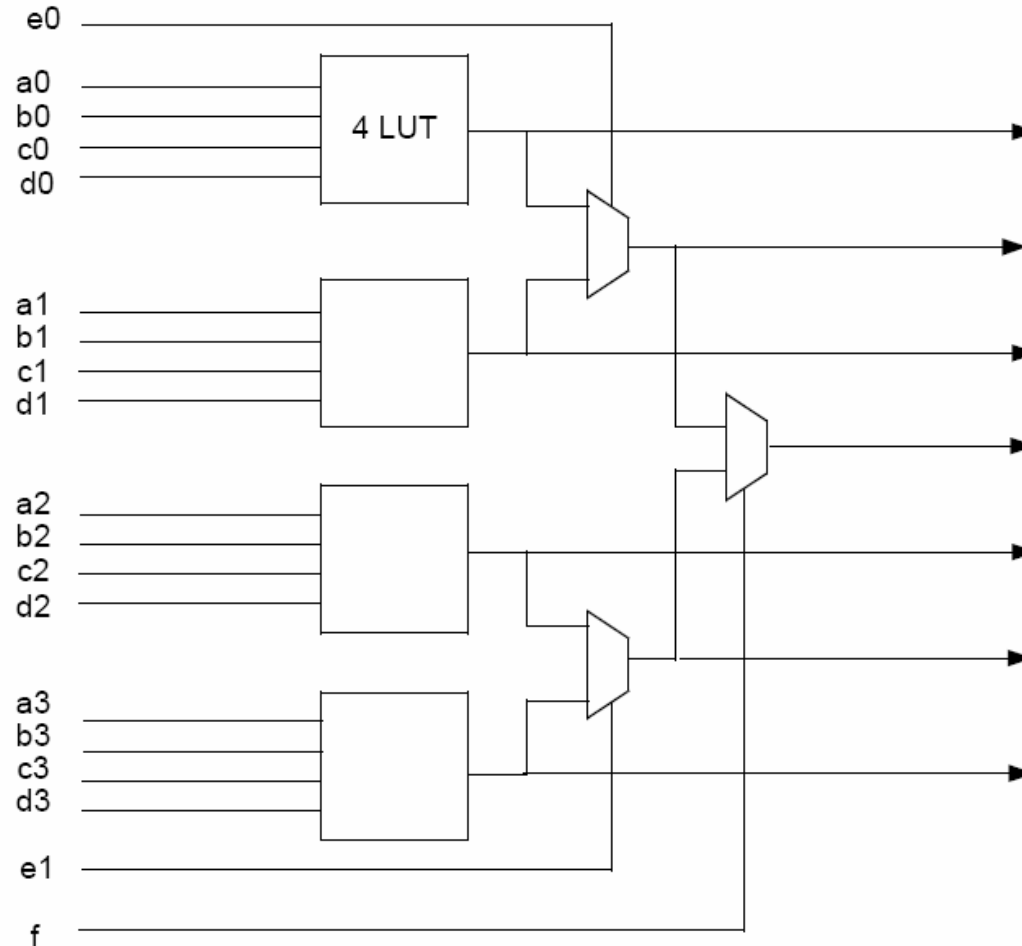
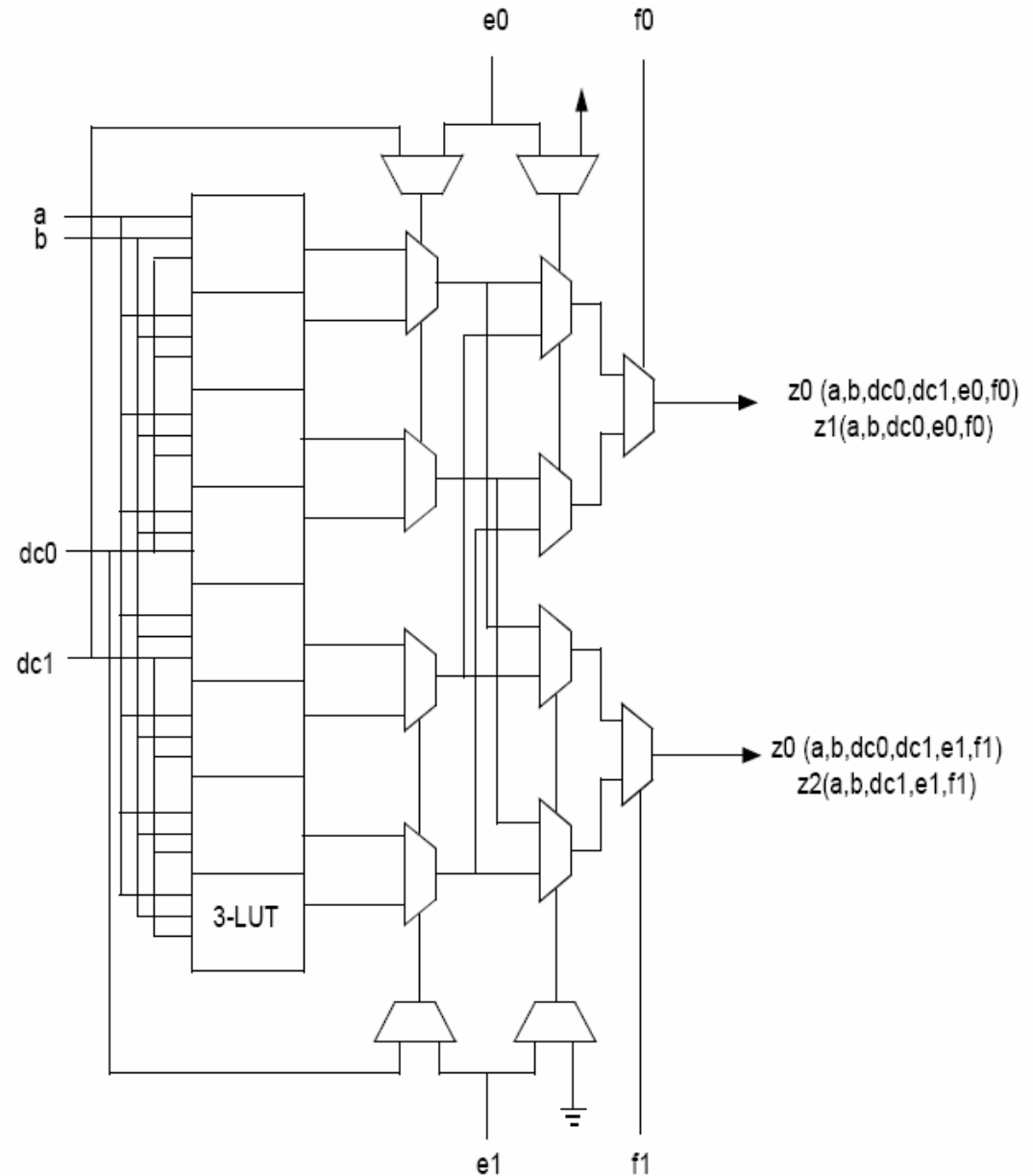


Figure 4: Composable 6-LUT constructed from 4-LUTs

Third 6-LUT Option – Shared LUT

- **More complicated, but efficient**

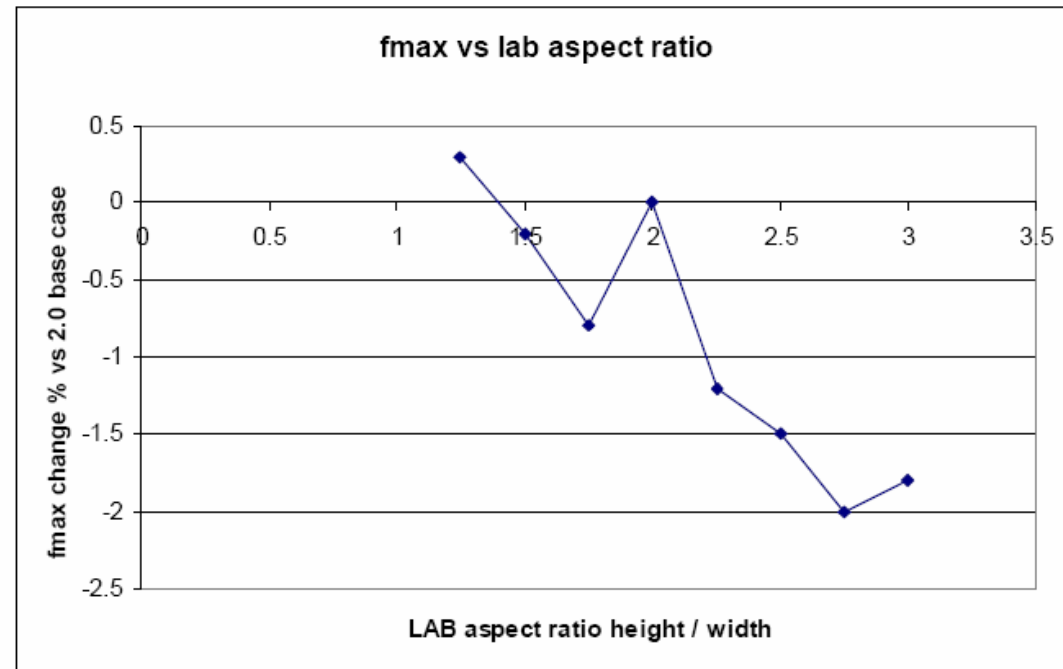


Cluster size selection for Stratix II

- Bias towards slightly smaller cluster size due to size issues

LAB Size Results Summary

#ALEs per LAB	# LAB lines	Channel Width	Fmax	LAB Area
6	30	188	-4%	5.50%
8	38	212	2%	1.50%
10	46	236	0%	0%
12	54	260	1%	0.30%
14	62	274	2%	0.50%



Fast connections for routing

◦ **Note mux construction**

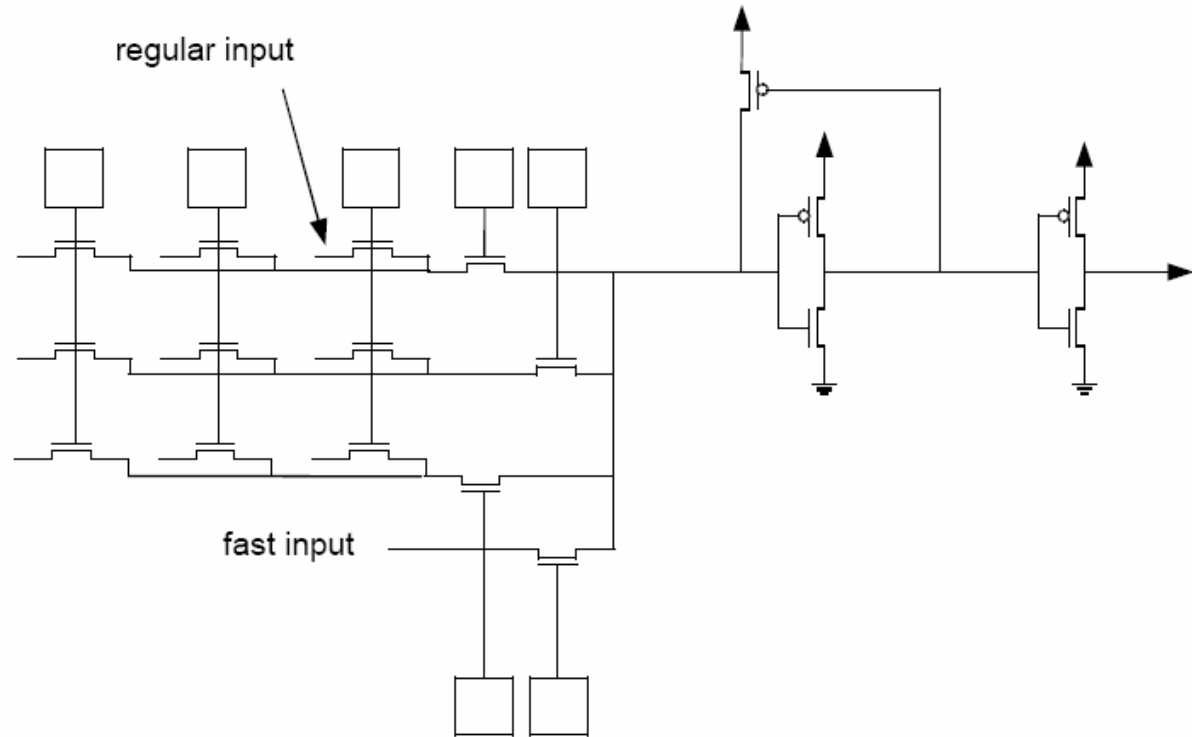


Figure 9: Fast inputs to routing multiplexers

Fast connections for routing

Table 2: Effect of adding fast inputs to routing multiplexers

Fast Inputs per Routing Mux	Fmax All Circuits	Fmax Circuits > 5K LEs	Fmax Circuits >10K LEs
1 Fast	5.7%	5.6%	2.7%
2 Fast	4.0%	3.5%	0.9%
All Fast	7.6%	7.8%	7.7%

- **1 Fast option was chosen due to experimental noise**

Summary

- **Recent work has reexamined values of N and K inside the cluster**
- **Performance remains an important issue although power is gaining**
- **Single-driver wiring reduces area and leads to improved performance**
- **Commercial architectures are quite advanced**
 - **Rely heavily on CAD tools**

Next topic: FPGA placement and routing