Practice Problems Solution

1) Solve the attached problem on the single-cycle MIPS processor

a) Generate control signals for beq, lw, and sw instructions

<table>
<thead>
<tr>
<th>Instr</th>
<th>RegDst</th>
<th>Branch</th>
<th>MemRead</th>
<th>MemtoReg</th>
<th>MemWrite</th>
<th>ALUSrc</th>
<th>RegWrite</th>
</tr>
</thead>
<tbody>
<tr>
<td>beq</td>
<td>x</td>
<td>1</td>
<td>0 or x</td>
<td>x</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>add</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>sw</td>
<td>x</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

b) Determine the critical (longest) path for the single-cycle MIPS processor

The longest path is I-Mem - Registers - ALU - D-Mem - Mux - Registers. The lw instructions go through all these components. So the latency is 350+190+180+400+25+190ps = 1335 ps

c) If you can reduce the latency of one component by 20%, which component would you choose? Explain your selection

D-mem registers would be the best choice because the 20% reduction would save 80ps in the Critical path. This would enable the processor to run faster. Reducing critical path delay is the key, not the common case delay.

2) Patterson and Hennessy; Exercise 4.1 (except with sub instead of and).

Control signals:

<table>
<thead>
<tr>
<th>RegWrite</th>
<th>MemRead</th>
<th>ALUMux</th>
<th>MemWrite</th>
<th>ALUOp</th>
<th>RegMux</th>
<th>Branch</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>0 (Reg)</td>
<td>0</td>
<td>sub</td>
<td>1 (ALU)</td>
<td>0</td>
</tr>
</tbody>
</table>

Resources performing a useful function: All except Data Memory and branch Add unit
Resource outputs that are not used: Branch Add
Resources that produce no outputs: Data Memory
3) Patterson and Hennessy; Exercise 4.2.

Which existing blocks (if any) can be used for this instruction?

All except branch Add unit

Which new functional blocks (if any) do we need for this instruction? What new signals do we need (if any) from the control unit to support this instruction?

Nothing except MUXes and associated control signal

4) The logic latencies for individual stages in a processor are listed. Compute the following

   a) What is the minimum clock period for a pipelined and a non-pipelined processor using these parameters

   For a non-pipelined processor, the sum of latencies of all stages is the clock period which is 320+ 380+360+420+180= 1660ps

   b) What is total latency of a MIPS lw instruction in an unpipelined processor? What is the throughput of a large series of lw instructions with no stalls or hazards?

   From (a), the minimum clock period is 1660ps,

   Throughput is 1/1660ps. This equals 602.41 million instructions per second (MIPS) since one ps is 1/10^{12} seconds