

**ECE 667 - Spring 2011**  
**Synthesis and Verification of Digital Systems**

**Homework #5: SAT, Equivalence Checking, FSM Reachability, Retiming**

1. (20 pts) For this problem consult the slides on Boolean SAT and CNF presented by Girish Paladugu and Monissa Mohan in class (see the link from the lecture page).

Consider the two-output Boolean network represented by the following netlist (same as in Problem 2 of Homework 3):

$$w = a \cdot b; \quad y = w + c; \quad x = c' + d; \quad f_1 = (x \cdot y)'; \quad f_2 = bx'$$

- (a) Write a CNF clause for each gate in the network and create a CNF formula for the entire network with outputs  $f_1, f_2$
- (b) Solve the CNF formula for  $f_1 = 1$  using DPLL algorithm or similar method. Show the essential steps of your procedure (choices made, reduction of the clauses, constant propagation, etc.).
- (c) Create a CNF formula to find an input combination for which:
- $f_1 = 0$  and  $f_2 = 1$ ; and
  - $f_1 = 1$  and  $f_2 = 0$ .

Look at Homework 3 for a hint on how to approach it in a systematic way. Comment on your solution, compare to your result in Homework 3.

2. (10 pts) In the following, refer to slide 35 (Equivalence Checking) in Girish's presentation. Prove one of the following statements (choose one).

- (a) For the two circuits to be equivalent, the output of the miter  $z = 1$  must be unsatisfiable (unSAT).
- (b) Given a Boolean function  $F$  and some property  $p$ , for the function  $F$  to satisfy property  $p$ , the formula  $F \wedge \bar{p}$  must be unSAT.

3. (25 pts) Consider the synchronous network in Fig. 9.8 of DeMicheli (p. 463). Compute legal retiming for clock period  $\phi = 22$  for the network.

- (a) Construct the register path weight matrix  $W$  and the path delay matrix  $D$  for this network and determine current period  $\phi$  using only the information contained in these two matrices (not from the circuit!).
- (b) Formulate all retiming constraints for  $\phi = 22$ . Compute the retiming vector  $R$  and draw the final retimed network showing the position of registers. Report the number of registers in the network. What is the actual clock period  $\phi^*$  obtained with this retiming? Show all the steps of your procedure.
- (c) Find legal retiming which minimizes the number of registers for value of  $\phi^*$  computed above. Show the formulation of the optimization problem. Use ILP software to solve the problem. Compare the results with part (a).
- (d) Compute legal retiming for clock period  $\phi^*$  obtained in part (a) using relaxation algorithm *FEAS*. Clearly show all the steps of the procedure, and sketch the final optimized network. What is the actual clock period  $\phi$  obtained with this method?

4. (20 pts)

Consider two FSMs,  $M1$  and  $M2$ , shown below, with initial states  $s1$  and  $s4$ , respectively.

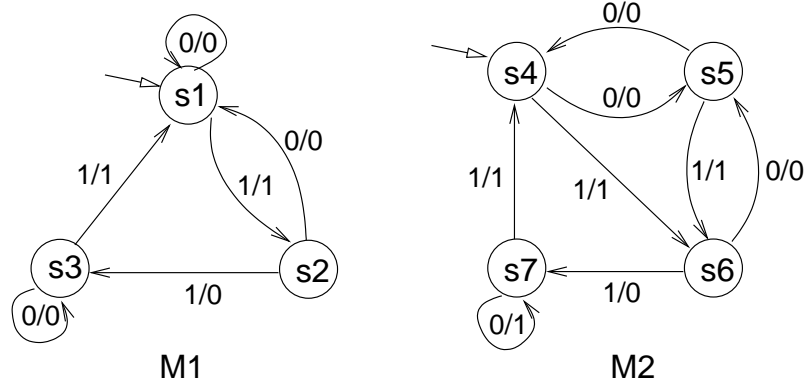


Figure 1: Two STGs for Problem 4

- (a) Construct the state transition graph (STG) of the product machine. Identify all strongly connected components (SCCs) of the product machine and label each as either reachable or unreachable. Show the transitions from all states, including unreachable states.
  - (b) Are the two machines equivalent? Apply Algorithm *BFS\_FSM* (Section 7.8, p. 303 Hachtel/Somenzi) to the product machine to prove or disprove their equivalence. In case of non-equivalence, produce a minimum length error trace. Check the correctness of your result by simulating both machines with the found error trace (if any).
5. (25 pts) Consider again the product FSM in Problem 4. Use the implicit FSM traversal technique to compute all states that are reachable from the initial state  $(s1, s4)$  in one clock cycle.

Derive transition relations for the product machine, and compute the image of the initial state  $C = \{s_1, s_4\}$  under this transition relation. Give Boolean expressions for the reached states. Examine the output associated with the reached states to see if they produce errors.

(Feel free to use any of the logic minimization technique or whatever other tools you may need to simplify your labor.)