Maciej Ciesielski

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PROFESSIONAL PREPARATION

1983 **Ph.D., Electrical Engineering**, University of Rochester, Department of Electrical Engineering, Rochester, N.Y.

1974 **M.S., Electrical Engineering**, Institute of Electron Technology, Warsaw Technical University, Warsaw, Poland.

APPOINTMENTS

1987-present **University of Massachusetts**, Amherst, MA, ECE Department. Professor (since 2003) and Associate Department Head.

1986 - 1987 **University of Lowell**, Computer Science Department, Lowell, MA. Assistant Professor.

1983 - 1986 **GTE Laboratories**, Computer Science Laboratory, Waltham, MA. Senior Member of Technical Staff.

RESEARCH INTEREST

- Electronic Design Automation (EDA).
- Formal verification and design validation of digital systems.
- High-level and logic synthesis.
- VLSI design.

PATENTS:

M. Ciesielski, at al. *Behavioral Transformations for Hardware Synthesis and Code Optimization based on Taylor Expansion Diagrams*, US patent, 7,472,359, Dec. 2008.

MAJOR AWARDS

- Elevated to IEEE Fellow for "Contributions to logic synthesis and formal verification of arithmetic circuits", 2020.
- Residential First-Year Experience *Student Choice Award*, University of Massachusetts Amherst, 2013.
- Doctorate *Honoris Causa*, Université de Bretagne Sud, Lorient, France, May 2008.

SELECTED PUBLICATIONS (last 5 years)

- M. Ciesielski, A. Yasin, J. Dasari, "Functional Verification of Arithmetic Circuits: Survey of Formal Methods", 25th Intl. Symposium on Design & Diagnostics of Electronic Circuits and Systems (DDECS-2022), March 2022.
- Atif Yasin, Tiankai Su, Sebastien Pillement, Maciej Ciesielski, "Hardware-based Implicit Rewriting for Square-root Verification", Design, Automation and Test in Europe Conference, DATE-2020, pp. 532-537, March 2020.
- Dinesh Narasimhara, Suraj Rao, Akshaya Waingade, Atif Yasin, Maciej Ciesielski, "Dual Approach to Solving SAT in Hardware", IEEE 15th International Conference on Design & Technology of Integrated Systems in Nanoscale Era, DTIS 2020.
- Tiankai Su, Atif Yasin, Sbastien Pillement, Maciej J. Ciesielski, "Formal Verification of Constrained Arithmetic Circuits using Computer Algebraic Approach", ISVLSI 2020, pp. 386-391, 2020.
- Atif Yasin, Tiankai Su, Sebastien Pillement, Maciej Ciesielski, "Functional Verification of Hardware Dividers using Algebraic Model", 2019 IFIP/IEEE 27th International Conference on Very Large Scale Integration (VLSI-SoC), Cusco, Peru, Oct. 2019.

- Atif Yasin, Tiankai Su, Sebastien Pillement, Maciej Ciesielski, "Formal Verification of Integer Dividers: Division by a Constant", Internatinal Conf of VLSI, ISVLSI-2019, July 2019.
- M. Ciesielski, Tiankai Su, Atif Yasin, Cunxi Yu, "Understanding Algebraic Rewriting for Arithmetic Circuit Verification: a Bit-Flow Model", IEEE Trans. on Computer-Aided Design, 39(6): 1346-1357 (2020); early version April 2019.
- Cunxi Yu and M. Ciesielski, "Formal Analysis of GF Arithmetic - Parallel Verification and Reverse Engineering", IEEE Trans. on CAD, Vol. 38, No. 2, pp. 354-365, Feb. 2019.
- Cunxi Yu, Tiankai Su, Atif Yasin, Maciej Ciesielski, "Spectral Approach to Verifying Non-linear Arithmetic Circuits", ASPDAC, Japan, Jan. 21-24, 2019.
- Cunxi Yu, Atif Yasin, Tiankai Su, Alan Mishchenko, Maciej Ciesielski, "Rewriting Environment for Arithmetic Circuit Verification", 22nd International Conference on Logic Programming, Artificial Intelligence and Reasoning (LPAR-22), EPIC Series in Computing, Vol. 57, pp. 656-666, Nov. 16-21, 2018.
- Cunxi Yu, Maciej Ciesielski, Alan Mishchenko, "Fast Algebraic Rewriting Based on And-Inverter Graphs", IEEE Trans. on CAD, (DOI 10.1109/TCAD.2017.2772854) Vol. 37, No. 9, pp. 1907-1911, Sept. 2018.
- Cunxi Yu, Chau-Chin Huang, Gi-Joon Nam, Mihir Choudhury, Victor N. Kravets, Andrew Sullivan, Maciej Ciesielski, Giovanni De Micheli, "End-to-End Industrial Study of Retiming", ISVLSI-2018, pp. 203-208, Hong Kong, July 9-11, 2018.
- Tiankai Su, Atif Yasin, Cunxi Yu, Maciej Ciesielski, Computer Algebraic Approach to Verification and Debugging of Galois Field Multipliers, IEEE Intl. Symposium on Circuits and Systems (ISCAS), May 27-30, pp. 1-6, 2018.
- Cunxi Yu and M. Ciesielski, "Formal Analysis of GF Arithmetic Circuits - Parallel Verification and Reverse Engineering", IEEE Trans. on Computer-Aided Design, arXiv:1802.06870v1, pp. 1-13, Feb. 2018. Also in 38(2): 354-365 (2019).
- C. Yu, M. Ciesielski,, "Formal Analysis of Galois Field Arithmetic Circuits - Parallel Verification and Reverse Engineering", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), in final (second) review, Jan. 2018.

SOFTWARE DEVELOPED and published on WWW

- BDS, BDD-based Logic Synthesis System: http://www.ecs.umass.edu/ece/labs/vlsicad/bds/bds.html
- TDS, CAD for Data-Flow Design Optimization: hhttp://www.ecs.umass.edu/ece/labs/vlsicad/tds.html
- Parallel Distributed and Multi-core Simulation: https://bitbucket.org/tariq786/parallel_simulations/src

INSTITUTIONAL and PROFESSIONAL SERVICE

- IEEE, Life Fellow.
- Associate Department Head, since Sept. 2006
- Distinguished Erasmus Mundus Scholar (MS Program), Univ. Kaiserslautern, 2012-2019.
- General Chair of ICCD-2020 and ICCD-2021.
- Technical Program Committees: DDECS 2019 - 2023, GLSVLSI 2010-13, DATE 2010, CFV 2008-2013, VLSI 2001. Session chairman: HLDVT 2009, DAC 2006. Program Committee Topics Chair: ECECS-2002.
- Member of Centre National de la Recherche Scientifique (CNRS) accreditation team evaluating Laboratoire Informatique, Robotique et Microelectronique de Montpellier, France, June 2002.
- Invited tutorials and panels: Univ. Torino, Univ. Trento, Bremen University, Univ. Politecnica de Catalunya, Univ. Madrid, Telecom Bretagne, UBS/UBO France, ICCD 2015, ISCAS 1989, ISCAS 1994.
- Reviews: NSF panels, proposals, misc. journal/conference papers.

Ph.D. ADVISING (UMass):

Graduated 21 Ph.D. students and taught over 4,500 students during the 35-year tenure at UMass.