Maciej Ciesielski

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PROFESSIONAL PREPARATION

1983 **Ph.D., Electrical Engineering**, University of Rochester, Department of Electrical Engineering, Rochester, N.Y.

1974 **M.S., Electrical Engineering**, Institute of Electron Technology, Warsaw Technical University, Warsaw, Poland.

APPOINTMENTS

1987-present **University of Massachusetts**, Amherst, MA, ECE Department. Professor (since 2003) and Associate Department Head.

1986 - 1987 **University of Lowell**, Computer Science Department, Lowell, MA. Assistant Professor.

1983 - 1986 **GTE Laboratories**, Computer Science Laboratory, Waltham, MA. Senior Member of Technical Staff.

RESEARCH INTEREST

- Electronic Design Automation (EDA).
- Formal verification and design validation of digital systems.
- High-level and logic synthesis.
- VLSI design.

PATENTS:

M. Ciesielski, at al. *Behavioral Transformations for Hardware Synthesis and Code Optimization based on Taylor Expansion Diagrams*, US patent, 7,472,359, Dec. 2008.

MAJOR AWARDS

- Doctorate *Honoris Causa*, Université de Bretagne Sud, Lorient, France, May 2008.
- Residential First-Year Experience *Student Choice Award*, University of Massachusetts Amherst, 2013.

RESEARCH FUNDING (since 2011)

- National Science Foundation, "Word-level Abstraction of Arithmetic Gate-level Circuits", M. Ciesielski (sole PI), Award No. CCF-1617708, $450,000, 06/15/2016 - 05/31/2019;
- National Science Foundation, "Data-flow Approach to Verification of Arithmetic Circuits", M. Ciesielski (sole PI), Award No. CCF-1319496, $374,000, 09/2013 - 08/2016.
- National Science Foundation, "Advances in Distributed Spatial-Parallel Event-Driven HDL Simulation", M. Ciesielski (sole PI), Award No. CCF-1017530, $475,000; 09/2010 - 08/2014.

SELECTED PUBLICATIONS (since 2011)

- C. Yu, M. Ciesielski,, "Formal Analysis of Galois Field Arithmetic Circuits - Parallel Verification and Reverse Engineering", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), in final (second) review, Jan. 2018.
- C. Yu, X. Zhang, D. Liu, M. Ciesielski, D. Holcomb, "Incremental SAT-based Reverse Engineering of Camouflaged Logic Circuits", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), TCAD.2017.2652220, pp. 1647 - 1659, Oct. 2017.
- C. Yu, M. Choudhury, D. Geiger, A. Sullivan and M. Ciesielski, "Advanced Datapath Synthesis using Graph Isomorphism", 2017 International Conference On Computer Aided Design (ICCAD'17), Nov. 2017.
- T. Su, C. Yu, A. Yasin, and M. Ciesielski, "Formal Verification of Truncated Multipliers using Algebraic Approach", 2017 IEEE Computer Society Annual Symposium on VLSI (ISVLSI'17), pp. 415-420, July 2017.

- C. Yu, D. Holcomb, M. Ciesielski, "Reverse-Engineering Irreducible Polynomials in GF(2^m) Arithmetic Circuits", Design, Automation and Test in Europe Conference, DATE 2017, pp. 1558-1563, March 2017.
- Cunxi Yu, Maciej Ciesielski, "Efficient Parallel Verification of Galois Field Multipliers", ASP-DAC 2017, pp. 238-243, January 2017.
- C. Yu, W. Brown, D. Liu, A. Rossi, M. Ciesielski, "Formal Verification of Arithmetic Circuits by Function Extraction", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 35(12): pp. 2131-2142, Dec. 2016.
- C. Yu, M. Ciesielski, "Analyzing Imprecise Adders using BDDs - A Case Study", IEEE Computer Society Annual Symposium on VLSI (ISVLSI-2016), pp. 152-157, July 2016.
- C. Yu, M. Ciesielski, "Formal Verification using Dont-care and Vanishing Polynomials", IEEE Computer Society Annual Symposium on VLSI (ISVLSI-2016), pp. 284-289, July 2016.
- C. Yu, M. Choudhury, A. Sullivan, M. Ciesielski, "DAC-Aware Logic Synthesis of Datapaths", Design Automation Conference (DAC-2016), pp. 135:1-135:6 , June 2016.
- C. Yu, M. Ciesielski, "Automatic Word-level Abstraction of Datapaths", 2016 IEEE International Symposium on Circuits and Systems (ISCAS-2016), pp. 1718-1721, May 2016.
- L. Amar, M. Ciesielski (presenters), "Synthesis and Verification of Arithmetic Circuits", 2015 IEEE International Conference on Computer Design (ICCD), Oct. 2015.
*http : //rpsonline.com.sg/rps2prod/iccd*2015*/html/tutorial.html*
- S. Ghandali, C. Yu, D. Liu, W. Brown, M. Ciesielski, "Logic Debugging of Arithmetic Circuits", IEEE Computer Society Annual Symposium on VLSI (ISVLSI) 2015, pp. 113-118, July 2015.
- L. Amar, P. Gaillardon, A. Mishchenko, M. Ciesielski, G. Micheli, "Exploiting Circuit Duality to Speed up SAT", IEEE Computer Society Annual Symposium on VLSI (ISVLSI-2015), pp. 101-106, July 2015.
- M. Ciesielski, C. Yu, D. Liu, W. Brown, A. Rossi, "Verification of Gate-level Arithmetic Circuits by Function Extraction", ACM Design Automation Conference (DAC), pp. 52-57, June 2015.
- C. Yu, Walter Brown, Maciej Ciesielski, "Verification of Arithmetic Datapath Designs using Word-level Approach - A Case Study", IEEE Intl. Symp. Circuits & Systems (ISCAS), pp. 1862 - 1865, May 2015.
- M. Ciesielski, W. Brown, D. Liu, A. Rossi, "Function Extraction from Arithmetic Bit-level Circuits" , IEEE Computer Society Annual Symposium on VLSI (ISVLSI-2014), pp. 356-361, July 2014
- T.B. Ahmad, M. Ciesielski, "Parallel Multi-core Verilog HDL Simulation using Domain Partitioning", IEEE Computer Society Annual Symposium on VLSI (ISVLSI), pp. 619-624, July 2014.
- M. Ciesielski, W. Brown, D. Liu, A. Rossi, "Function Extraction from Arithmetic bit-level Circuits", (interactive presentation), Design Automation Conference (DAC-2014), June 2014.
- T. Ahmad, M. Ciesielski, "Fast Time-Parallel C-based Event-Driven RTL Simulation", Design and Diagnostics of Electronic Circuits and Systems, (DDECS-14), pp. 71-76, April 2014.
- T. Ahmad and M. Ciesielski, "Fast STA Prediction-based Gate-Level Timing Simulation", Design Automation and Test in Europe, (DATE-2014), pp. 248.1–248.6, March 2014.
- M. Ciesielski, W. Brown, A. Rossi, "Arithmetic Bit-level Verification using Network Flow Model", Haifa Verification Conference, (HVC'13), Nov. 2013.
- D. Kim, M. Ciesielski, S. Yang, "Multi-Level Temporal-parallel Event-driven Simulation", *IEEE Transactions on CAD*, 32(6), pp. 845-857, June 2013.
- D. Gomez-Prado, M. Ciesielski, R. Tessier, "FPGA Latency Optimization using System-level Transformations and DFG Restructuring", *DATE-2013*, pp. 1553-1558, March 2013.
- T.B. Ahmad, M. Ciesielski, D. Kim, and S. Yang, "Application of Parallel Distributed Event Driven Simulation for Accelerating Hardware Verification," Advances in Distributed and Parallel Computing (ADPC 2012), pp. 54-59, Sept. 2012.
- T.B. Ahmad, N. Kim, B. Min, A. Kalia, M. Ciesielski, and S. Yang, "Scalable Parallel Event-driven HDL Simulation for Multi-Cores", Intl. Conf. on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design, SMACD-12, pp. 217-220, Sept. 2012.
- T.B. Ahmad, N. Kim, B. Min, A. Kalia, M. Ciesielski, and S. Yang, "Scalable Parallel Event-driven HDL Simulation for Multi-Cores," Work in progress (WIP) interactive presentation, Design Automation Conference, (DAC 2012), June 2012.
- S. Yang, T.Ahmad, M. Ciesielski, "Scalable Parallel Event-driven HDL Simulation for Multi Cores", Design Automation Conference (WIP session), pp. 1-4, June 2012.
- S. Yang, T.Ahmad, M. Ciesielski, "Scalable Parallel Event-driven HDL Simulation for Multi Cores", Design Automation Conference (WIP session), June 2012.

- M.A. Basith, T. Ahmad, A. Rossi, M. Ciesielski, "Algebraic Approach to Arithmetic Design Verification" *Formal Methods in CAD*, FMCAD-11, pp. 67-71, Oct. 2011.
- S. Banerjee, J. Mathew, S. Mohanty, D.K. Pradhan, M. Ciesielski, "A Variation-Aware TED-based Approach for Nano-CMOS RTL Leakage Optimization", in *Journal of Low Power Electronics*, JOLPE, Vol.7, No. 4, pp. 471-481, Dec. 2011.
- D. Kim, M. Ciesielski, K. Shim, S.Yang, "Temporal Parallel Simulation: A Fast Gate-Level HDL Simulation using Higher Level Models", Design, Automation and Test in Europe, DATE'11, pp. 1584-1589, March 2011.
- D. Kim, M. Ciesielski, S.Yang, "A New Distributed Event-Driven Gate-Level HDL Timing Simulation by Accurate Prediction", Design, Automation and Test in Europe, DATE'11, pp. 547-550, March 2011.
- S. Banerjee, J. Mathew, D. Pradhan, S. Mohanty, M. Ciesielski, "Variation-Aware TED - Based Approach for Nano-CMOS RTL Leakage Optimization" VLSID 2011, pp. 304-309, Jan. 2011.

SOFTWARE DEVELOPED and published on WWW

- BDS, BDD-based Logic Synthesis System: http://www.ecs.umass.edu/ece/labs/vlsicad/bds/bds.html
- TDS, CAD for Data-Flow Design Optimization: hhttp://www.ecs.umass.edu/ece/labs/vlsicad/tds.html
- Parallel Distributed and Multi-core Simulation: https://bitbucket.org/tariq786/parallel_simulations/src

INSTITUTIONAL and PROFESSIONAL SERVICE

- IEEE, Senior Member. Associate Department Head, since Sept. 2006
- Distinguished Erasmus Mundus Scholar (MS Program), Univ. Kaiserslautern, 2012-2018.
- Technical Program Committees: GLSVLSI 2010-13, DATE 2010, CFV 2008-2013, VLSI 2001. Session chairman: HLDVT 2009, DAC 2006. Program Committee Topics Chair: ECECS-2002.
- Invited tutorials and panels: Univ. Torino, Univ. Trento, Bremen University, Univ. Politecnica de Catalunya, Univ. Madrid, Telecom Bretagne, UBS/UBO France, ICCD 2015, ISCAS 1989, 1994.
- Reviews: NSF panels 2014, 2011, 2009, 2007, 2001, 1999; Reviewer: proposals, journal/conference papers.

Ph.D. ADVISING (UMass):

Graduated 19 Ph.D. students and taught over 4,000 students during the 30-year tenure at UMass.