# Maciej Ciesielski

Department of Electrical & Computer Engineering
University of Massachusetts, Amherst, MA 01003
*ciesiel@ecs.umass.edu*
tel: (413) 545-0401, fax: (413) 545-4611
*http://www.ecs.umass.edu/ece/labs/vlsicad/ciesielski.html*

## PROFESSIONAL PREPARATION

**1983** **Ph.D., Electrical Engineering**, University of Rochester, Department of Electrical Engineering, Rochester, N.Y.

**1974** **M.S., Electrical Engineering**, Institute of Electron Technology, Warsaw Technical University, Warsaw, Poland.

## APPOINTMENTS

**1987-present** **University of Massachusetts**, Amherst, MA, ECE Department.
Professor (since 2003) and Associate Department Head.

**1986 - 1987** **University of Lowell**, Computer Science Department, Lowell, MA.
Assistant Professor.

**2002-present** **LogicMill Technology, LLC**, Amherst, MA - founder and president.

**1983 - 1986** **GTE Laboratories**, Computer Science Laboratory, Waltham, MA.
Senior Member of Technical Staff.

## RESEARCH INTEREST

- Formal verification; arithmetic functional verification.
- Design validation and simulation-based verification; parallel simulation.
- Logic and high-level synthesis.

## SELECTED PUBLICATIONS

- C. Yu, W. Brown, D. Liu, A. Rossi, M. Ciesielski, "Formal Verification of Arithmetic Circuits by Function Extraction", IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, May 2016.
- C. Yu, M. Choudhury, A. Sullivan, M. Ciesielski, "DAC-Aware Logic Synthesis of Datapaths", Design Automation Conference (DAC), pp. 1 - 6, June 2016.
- C. Yu, M. Ciesielski, "Automatic Word-level Abstraction of Datapaths", 2016 IEEE International Symposium on Circuits and Systems (ISCAS), pp. 1 - 6, May 2016.
- S. Ghandali, C. Yu, D. Liu, W. Brown, M. Ciesielski, "Logic Debugging of Arithmetic Circuits", IEEE Computer Society Annual Symposium on VLSI (ISVLSI) 2015, pp. 113-118, July 2015.
- L. Amar, P. Gaillardon, A. Mishchenko, M. Ciesielski, G. Micheli, "Exploiting Circuit Duality to Speed up SAT", IEEE Computer Society Annual Symposium on VLSI (ISVLSI-2015), pp. 101-106, July 2015.
- M. Ciesielski, C. Yu, D. Liu, W. Brown, A. Rossi, "Verification of Gate-level Arithmetic Circuits by Function Extraction", ACM Design Automation Conference (DAC), pp. 52-57, June 2015.
- C. Yu, Walter Brown, Maciej Ciesielski, "Verification of Arithmetic Datapath Designs using Word-level Approach - A Case Study", IEEE Intl. Symp. Circuits & Systems (ISCAS), pp. 1862 - 1865, May 2015.
- M. Ciesielski, W. Brown, D. Liu, A. Rossi, "Function Extraction from Arithmetic Bit-level Circuits" , IEEE Computer Society Annual Symposium on VLSI (ISVLSI), pp. 356-361, July 2014
- T.B. Ahmad, M. Ciesielski, "Parallel Multi-core Verilog HDL Simulation using Domain Partitioning", IEEE Computer Society Annual Symposium on VLSI (ISVLSI), July 2014.
- T. Ahmad and M. Ciesielski, "Fast STA Prediction-based Gate-Level Timing Simulation", DATE-2014, pp. 248.1-248.6, March 2014.
- M. Ciesielski, W. Brown, A. Rossi, "Arithmetic Bit-level Verification using Network Flow Model", Haifa Verification Conference, HVC-2013, pp. 327-343, Nov. 2013.

- D. Kim, M. Ciesielski, S. Yang, "MULTES: Multi-Level Temporal-parallel Event-driven Simulation", *IEEE Transactions on CAD*, 32(6), pp. 845-857, June 2013.
- D. Gomez-Prado, M. Ciesielski, R. Tessier, "FPGA Latency Optimization using System-level Transformations and DFG Restructuring", Design, Automation and Test in Europe, DATE-2013, pp. 1553-1558, March 2013.
- T.B. Ahmad, M. Ciesielski, D. Kim, and S. Yang, "Application of Parallel Distributed Event Driven Simulation for Accelerating Hardware Verification," Advances in Distributed and Parallel Computing (ADPC 2012), pp. 54-59, Sept. 2012.
- M.A. Basith, T. Ahmad, A. Rossi, M. Ciesielski, "Algebraic Approach to Arithmetic Design Verification" *Formal Methods in CAD*, FMCAD-2011, pp. 67-71, Oct. 2011.
- S. Banerjee, J. Mathew, S. Mohanty, D.K. Pradhan, M. Ciesielski, "A Variation-Aware TED-based Approach for Nano-CMOS RTL Leakage Optimization", in *Journal of Low Power Electronics*, JOLPE, Vol.7, No. 4, pp. 471-481, Dec. 2011.
- A. Mishchenko, N. Een, R. K. Brayton, S. Jang, M. Ciesielski, T. Daniel, "Magic: An Industrial-Strength Logic Optimization, Technology Mapping, and Formal Verification Tool", IWLS-2010, pp. 124-127, June 2010.
- M. Ciesielski, D. Gomez-Prado, Q.Ren, J. Guillot, E. Boutillon, "Optimization of Data Flow Computations using Canonical TED Representation", *IEEE Transactions on Computer-Aided Design*, Vol. 28, No. 9, pp. 1321 - 1333, Sept. 2009.
- M. Ciesielski, J. Guillot, D. Gomez-Prado, E. Boutillon, "High-Level Transformations of Data Flow Computations using Canonical TED Representation", *Design & Test of Computers*, pp. 46-57, July/Aug 2009.
- M. Ciesielski, A.M. Jabir, D. Pradhan, invited book chapter "Canonical Graph-based Representations for Verification of Arithmetic and Data Flow Designs", 75 pages, in *Practical Design Verification*, ed. D.K. Pradhan, I.G. Harris, Cambridge University Press, 2009, pp. 173-245.
- D. Gomez-Prado, Q. Ren, M. Ciesielski, J. Guillot, E. Boutillon, "Optimizing Data Flow Graphs to Minimize Hardware Implementation", *Design, Automation and Test in Europe*, DATE-09, pp. 117-122, 2009.
- D. Kim, M. Ciesielski, K. Shim, S.Yang, "Temporal Parallel Gate-level Timing Simulation", *IEEE High Level Design Verification and Test*, HLDVT-08, pp. 111-116, Nov 2008.
- M. Ciesielski, S. Askar, D. Gomez-Prado, J. Guillot, E. Boutillon, "Data-Flow Transformations using Taylor Expansion Diagrams" *Design, Automation and Test in Europe Conference*, DATE-07, pp. 455-460, 2007.
- M. Ciesielski, P. Kalla, and S. Askar, "Taylor Expansion Diagrams: A Canonical Representation for Verification of Dataflow Designs", IEEE Trans. Computers, Vol. 55 (9), Sept. 2006, pp. 1188-1201.
- Z. Zeng, K.R. Talupuru, and M. Ciesielski, "Functional Test Generation based on Word-level SAT", in *Journal of Systems Architecture*, Elsevier Publishers, Vol.51(8), pp.488-511, Aug. 2005.
- C. Yang, M. Ciesielski, "BDS: A BDD-based Logic Optimization System", *IEEE Trans. on Computer-Aided Design*, Vol. 21, No. 7, pp 866-876, July 2002.

**PATENTS:**
M. Ciesielski, at al. *Behavioral Transformations for Hardware Synthesis and Code Optimization based on Taylor Expansion Diagrams*, US patent, 7,472,359, Dec. 31, 2008.

**INSTITUTIONAL and PROFESSIONAL SERVICE**

- IEEE, Senior Member.
- Associate Department Head, since Sept. 2006
- Distinguished Erasmus Mundus Scholar (MS Program), Univ. Kaiserslautern, Germany, 2012-2015.
- Technical Program Committees: GLSVLSI 2010-13 Track Chair; DATE 2010, CFV 2008-2012, VLSI 2001. Session chairman: HLDVT 2009, DAC 2006. Program Committee Topics Chair: ECECS-2002.
- Invited tutorials and panels: Univ. Politecnica de Calaunya, Univ. Madrid, Telecom Bretagne, UBS/UBO France, ISCAS 1989, 1994. Ad hoc reviewer, proposals and refereed journal and conference papers.

**SOFTWARE DEVELOPED and published on WWW**

- BDS, BDD-based Logic Synthesis System: http://www.ecs.umass.edu/ece/labs/vlsicad/bds/bds.html
- TDS, CAD for Data-Flow Design Optimization: hhttp://www.ecs.umass.edu/ece/labs/vlsicad/tds.html

**HONORS and AWARDS**

- Doctorate Honoris Causa, Université de Bretagne Sud, Lorient, France, May 2008.
- Residential First-Year Experience Student Choice Award, Amherst, April 2013.
- Nominated for Distinguished Teaching Award, 2010, 2011, 2013.

**Ph.D. Thesis Advising (UMass):**
Advised over 60 graduate students and graduated 18 Ph.D. students during his 29-year tenure at UMass.