

Floorplans, Planar Graphs, and Layouts

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Abstract—The topics discussed in this paper are minimization of the area occupied by a layout and related results concerning networks flow and rectilinear representation of planar graphs, based on a graph model of floorplans and layouts. We do not restrict our analysis to sliced floorplans but allow arbitrary floorplans. Given an arbitrary floorplan and the areas of the embedded building blocks, we prove the existence and uniqueness of a zero wasted area layout, and characterize it by a necessary and sufficient condition. On the basis of this condition we develop a scheme to generate zero wasted area layouts. We prove that given a family of dual network pairs for which the product of dual arc lengths are invariant, the minimal product of their longest paths is not smaller than the maximal product of their shortest paths. We also show that the maximal product of the flows in such a family of dual network pairs is given by the total sum of the arc length product of each individual pair of dual arcs. Finally, based on the zero wasted area layout, we present an efficient procedure to derive a rectilinear representation for any planar graph.

Index Terms—Floorplan, optimization, layout, graph representation, planar graphs, network flow.

I. INTRODUCTION

THE objective of many engineering problems such as in VLSI design, building architecture and alike, happens to be a valid *layout* of some *building blocks* of a rectangular shape. The first step towards this goal is to obtain a *floorplan* which is a partitioning of the floor rectangle into smaller ones. In the design of such a floorplan the engineer takes into account all the information in his possession about the required or admissible mutual positions of the building blocks. Fig. 1 shows a floorplan in which the rectangle B_0 is partitioned into eight subrectangles B_1 through B_8 . In the second step a layout is derived from the floorplan by embedding the physical rectangular building blocks into the floorplan's sub-rectangles, such that blocks do not overlap, and their relative position in the floorplan is preserved. Fig. 2 illustrates a layout derived from the floorplan given in Fig. 1. We say that the floorplan determines the *topology* of the layout.

In many cases not all the geometrical dimensions of the building blocks are predetermined, and the layout designer can set their values arbitrarily. These values can therefore be determined so as to optimize some measure of the layout. For example, in VLSI chip design, B_0 can be a

CPU and the B_i 's are functional blocks like ALU, control unit, register file, etc.. The designer may have a good estimate of the functional blocks' expected areas at a very early stage of the design cycle, while their length and width can still be changed so as to minimize the chip area. In building architecture B_0 can be a house and the B_i 's are its rooms. If the cost of the house is dominated by the cost of its external walls and only the areas of its rooms are predetermined, we may set their dimensions such that the layout's perimeter is minimized.

Most floorplans that have been discussed in the literature are *sliced* floorplans, for which the partitioning begins with the entire rectangle B_0 which is sliced into several slices either horizontally or vertically. This procedure is then repeated for every resulting slice until the smallest sub-rectangles which represent building blocks are reached. This approach has been employed for example, in min-cut placements of VLSI designs [10], [11], [13]. The slicing procedure induces a very restrictive topology of the floorplan. However, there are other less restrictive methods to obtain a floorplan, for example, one can derive a floorplan of a VLSI chip from the adjacency graph of its constituting blocks. A simple non-sliced floorplan is discussed in [3]. Recently, a method for modifying a given initial floorplan, has been presented in [2]. There, the initial stiff floorplan is relaxed, thus enabling to consider an entire class of possible configurations, from which the most promising floorplan is selected. Even when the initial floorplan is sliced, the final "best" floorplan may be non-sliced. The resulting floorplan is then used to determine the topology of the layout, which can be further optimized, as discussed later in this paper. In most cases, the layout optimization algorithms that were proposed for sliced floorplan are not applicable for the general floorplan.

In this paper we study arbitrary floorplans which cannot be obtained by any slicing procedure (like the one in Fig. 1) and discuss the problem of minimizing the area of a general layout obtained from an arbitrary floorplan. The goal of area minimization is typical in VLSI design, where the cost of a chip is dominated by its area. The problem of minimizing the area in sliced floorplans has been discussed in [15]. There, the dimensions of the building blocks are fixed, but the blocks can be arbitrarily oriented in parallel to the xy orthogonal axes. A polynomial algorithm to determine the orientation of each block in the layout, such that minimal wasted area results in, is presented there. The algorithm applies a *divide and conquer* approach to the recursive structure of the *series-parallel* digraph [17] rep-

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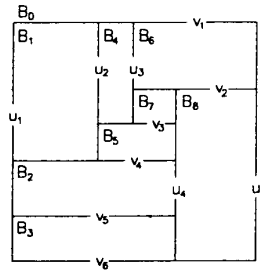


Fig. 1. Eight sub-rectangle floorplan.

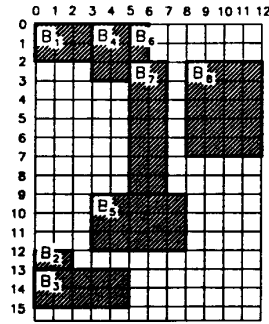


Fig. 2. A layout derived from the floorplan in Fig. 1

representing the sliced floorplan. It is also proved there that for general floorplans the problem of optimal orientation is NP-complete.

The rest of the paper is organized as follows. To study general floorplan we first present in Section II a graph model of floorplans and show how this model yields a layout. Using this graph model, we prove a theorem that separates the product of the longest paths from the product of the shortest paths in a family of dual network pairs. We then discuss the problem of obtaining a zero wasted area layout in Section III. We prove that there always exists a unique zero wasted area layout, and obtain a necessary and sufficient condition for its existence. We also present a flow interpretation of this condition which simplifies the problem of finding the zero wasted area layout. Section IV presents an algorithm to construct a rectilinear representation of any nonseparable planar graph, based on the graph model for floorplans and the theory presented in Section III. Conclusions and open questions for further research are presented in Section V.

II. FROM FLOORPLAN TO LAYOUT

A floorplan can be described by the vertical and horizontal line segments which determine the partitioning. In Fig. 1 there are five vertical line segments u_1 through u_5 and six horizontal line segments v_1 through v_6 . These line segments are not allowed to intersect each other. The floorplan's topology can be represented by two planar digraphs $G(U, E)$ and $H(V, F)$ constructed as follows. A vertex in $G(U, E)$ represents a vertical line segment of the floorplan. We order the vertices according to the distance of the corresponding line segments from the leftmost side

of the rectangle. Two vertices u_i and u_j in G are connected by an arc e directed from u_i to u_j if there is a sub-rectangle in the floorplan whose left and right edges lie on the corresponding vertical line segments, respectively. $G(U, E)$ is called the x -graph of the floorplan. Fig. 3(a) is the x -graph of the floorplan given in Fig. 1. It has one source and one sink corresponding to the leftmost and rightmost vertical line segments of the floorplan. Notice that $G(U, E)$ is an acyclic digraph, since closing a cycle would require the closing arc to be directed oppositely. The planar digraph $H(V, F)$ is defined similarly for the horizontal line segments and is called the y -graph of the floorplan. Fig. 3(b) depicts the y -graph of the floorplan given in Fig. 1. In Fig. 3(c) these graphs are drawn one above the other. We see that an arc of the x -graph intersects one and only one arc of the y -graph and vice versa. In addition, the direction of turning by an angle $\alpha < \pi$ an arc of the x -graph to its dual arc in the y -graph, so that their orientations coincide, is the same for all the dual arc pairs. Consequently, we may consider each graph to be the dual of the other. Notice that the source and the sink of G are both located in the infinite face of H and vice versa. In this representation, a pair of dual arcs (e, f) where $e \in E$ and $f \in F$, intersect each other if and only if they correspond to the same sub-rectangle in the floorplan. This graph model was used in [1] to represent the dissection of a rectangle into squares, and the above graphs were called *polar dual*. We shall use also the notion *dual networks*.

A sub-rectangle of the floorplan is occupied in the actual layout by some physical block which has a width x and a height y . These dimensions are introduced into G and H by assigning them as weights to the corresponding arcs. The weighted x -graph and y -graph are denoted by $G(U, E, \bar{x})$ and $H(V, F, \bar{y})$, respectively, where $\bar{x} = (x_1, \dots, x_b)$ and $\bar{y} = (y_1, \dots, y_b)$ are the weights. The actual layout can now be derived from G and H as follows. Assign a zero x -coordinate to the leftmost vertical line segment (represented by the source of G) and zero y -coordinate to the uppermost horizontal line segment (represented by the source of H). The position of every block in the layout is then determined by the coordinates of its upper left corner which can be calculated by computing the length of the longest paths in G and H starting at the sources and ending at the corresponding vertices of G and H . An overview of using this model in various design systems is found in [2].

Example 1: Let the dimensions of the blocks to be placed in the floorplan shown in Fig. 1, be

$$\begin{aligned} x_1 &= 3, x_2 = 2, x_3 = 5, x_4 = 2, \\ x_5 &= 5, x_6 = 1, x_7 = 2, x_8 = 4, \\ y_1 &= 2, y_2 = 1, y_3 = 2, y_4 = 3, \\ y_5 &= 3, y_6 = 2, y_7 = 7, y_8 = 5. \end{aligned}$$

Assigning the above weights to the corresponding arcs in G and H and then computing the length of the longest path from the source to each node in G and H results in the layout drawn in Fig. 2. ■

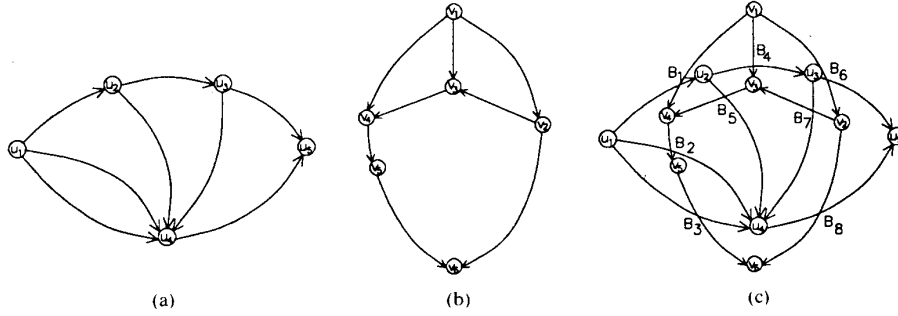


Fig. 3. The graph representation of the floorplan in Fig. 1.

Unless otherwise stated, we use the notion path for a directed path starting at the source and ending at the sink. Such paths of maximal length will be called critical paths. The width w and the height h of the layout equal to the length of the critical paths in G and H , respectively. Once w and h are known, we can calculate the area A of the layout. In Fig. 2 we see that not all the area is occupied by blocks. The unutilized area is considered to be wasted and should be minimized.

Before proceeding to Section III, we prove a separation theorem, based on the graph representation of floorplans and layouts. This theorem states that given a family $\Phi = \{(G, H)\}$ of dual network pairs for which the product of dual arcs' length is invariant, there exists a constant which separates the product of their shortest paths from the product of their longest paths.

Theorem 1: Consider an arbitrary assignment of weights $\bar{x} = (x_1, \dots, x_b)$ and $\bar{y} = (y_1, \dots, y_b)$ to the arcs of G and H , respectively, where $(G, H) \in \Phi$, such that for any two dual arcs, the product of their weights satisfies

$$x_j y_j = a_j, \quad 1 \leq j \leq b. \quad (2.1)$$

Let w and h be the length of the longest paths in G and H , respectively, and let z and g be the length of the shortest paths in G and H , respectively. Then, the minimal product of the longest paths length is separated from the maximal product of the shortest paths length as follows:

$$\min_{(G, H) \in \Phi} w(\bar{x})h(\bar{y}) \geq \sum_{j=1}^b a_j \geq \max_{(G, H) \in \Phi} z(\bar{x})g(\bar{y}). \quad (2.2)$$

Proof: Interpreting x_j as the width of a building block B_j , y_j as its height and a_j as its area, we can derive a layout from G and H . Since in a valid layout no two blocks overlap, and since $w(\bar{x})$ and $h(\bar{y})$ are the width and the height of the layout, we conclude that for every arc length assignment satisfying (2.1), there exists:

$$w(\bar{x})h(\bar{y}) \geq \sum_{j=1}^b x_j y_j = \sum_{j=1}^b a_j. \quad (2.3)$$

To prove the lower bound we generate an invalid layout as follows. Rather than determine the coordinates of the upper left corner of a block by the length of the longest paths from the sources to the corresponding vertices in G and H , we determine them by the length of the shortest paths from the sources to the corresponding vertices. We

then define the width $z(\bar{x})$ and the height $g(\bar{y})$ of the resulting invalid layout as the length of the shortest paths in G and H , respectively. In the invalid layout thus created, there is no vacant area, some blocks may overlap, and some may extend beyond the right and bottom edges of the layout. Therefore,

$$z(\bar{x})g(\bar{y}) \leq \sum_{j=1}^b x_j y_j = \sum_{j=1}^b a_j. \quad (2.4)$$

Equations (2.3) and (2.4) hold for every $\bar{x}$ and $\bar{y}$ satisfying (2.1), which proves (2.2). ■

We may ask whether the separator $\sum_{j=1}^b a_j$ is achievable, that is, whether there exists an assignment of arc lengths satisfying (2.1) for which the inequalities of (2.2) become equalities. Obviously, in such a case, all the critical paths in G and all the critical paths in H are equally long. In Section III it is proved that the equalities in (2.2) are achievable, and the resulting layout has therefore a zero wasted area.

III. MINIMIZING THE AREA OF A LAYOUT

In this section we discuss the problem of minimizing the area of a layout when the areas of its building blocks are predetermined but not their dimensions. Let x_j and y_j denote the length of the arcs e_j and f_j , respectively. The dimensions x_j and y_j of the building block B_j , $1 \leq j \leq b$, will be determined as to minimize the area of the layout.

The area A of the layout depends upon the length of the paths from source-to-sink in G and H . Let Γ_i , $1 \leq i \leq k$, and Δ_i , $1 \leq i \leq l$, denote the paths from source to sink in G and H , respectively. Each path Γ_i in G consists of several arcs e_j and we define a $k \times b$ zero-one matrix K as follows:

$$K_{ij} = \begin{cases} 1, & e_j \in \Gamma_i \\ 0, & \text{otherwise.} \end{cases} \quad (3.1)$$

L is a $l \times b$ zero-one matrix defined similarly for H . Let w be the length of a critical path in G and let h be the length of a critical path in H (notice that G and H may possess several critical paths). Then, by definition

$$\sum_{j=1}^b K_{ij} x_j - w \leq 0, \quad 1 \leq i \leq k \quad (3.2)$$

$$\sum_{j=1}^b L_{ij} y_j - h \leq 0, \quad 1 \leq i \leq l \quad (3.3)$$

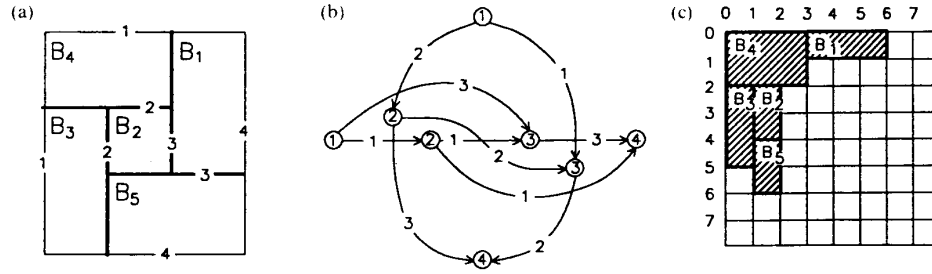


Fig. 4. Five block floorplan and the implied layout.

where x_j , y_j , w , and h are all unknown. The dimensions x_j and y_j of the block B_j have to be set so that the area a_j of B_j is preserved, i.e.,

$$x_j y_j = a_j, \quad 1 \leq j \leq b. \quad (3.4)$$

If in addition to (3.4), the *aspect ratios* of the building blocks, defined by y_j/x_j , are constrained to some range, then this can be expressed by the following inequality:

$$x_j^l \leq x_j \leq x_j^h, \quad 1 \leq j \leq b. \quad (3.5)$$

The corresponding constraints imposed on y_j are obtained from (3.4) and (3.5). Our objective is, therefore, to find weights x_j , y_j , $1 \leq j \leq b$, so that the area

$$A = wh \quad (3.6)$$

is minimized and the constraints (3.2)–(3.5) are satisfied.

Equations (3.2)–(3.6) constitute a nonlinear mathematical program, which can be solved by using appropriate mathematical programming algorithms [8], but its solution is very difficult. In the following we show that a closed form solution can be obtained by employing the x -graph and the y -graph corresponding to the floorplan.

3.1. Necessary and Sufficient Conditions for Minimal Area

Let us first relax the restrictions concerning the aspect ratios of the building blocks, given in (3.5). We show now that any given layout with area A , represents a whole family of layouts, each one of them with area A and an arbitrary aspect ratio h/w .

Lemma 1: Let $G(U, E, \bar{x})$ and $H(V, F, \bar{y})$ be the x -graph and the y -graph, respectively, of a given floorplan. Let a_j be the area of B_j , $1 \leq j \leq b$, that is, $a_j = x_j y_j$. Let w , h , and A be the width, height and area of the layout implied by G and H , respectively, and let $\mu = h/w$ denote its aspect ratio. Then, for every $\lambda > 0$ there is an assignment of arc lengths $\bar{x}(\lambda)$ and $\bar{y}(\lambda)$ such that the area of the resulting layout is A and its aspect ratio is λ .

Proof: The length of the critical paths in G and H , w , and h , respectively, satisfy $wh = A$. Create now new graphs $G'(U, E, \bar{x}')$ and $H'(V, F, \bar{y}')$ isomorphic to G and H , respectively, which satisfy

$$x'_j = x_j \sqrt{\mu/\lambda}, \quad y'_j = y_j \sqrt{\lambda/\mu}, \quad 1 \leq j \leq b.$$

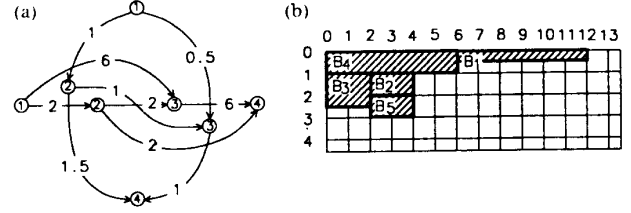


Fig. 5. Transformation of the layout in Fig. 4.

The following is true:

- 1) Every pair (e_j, f_j) of dual arcs in G' and H' represents a building block whose area is a_j , since

$$x'_j y'_j = x_j \sqrt{\mu/\lambda} y_j \sqrt{\lambda/\mu} = x_j y_j = a_j.$$

- 2) The longest paths of G' and H' , whose lengths are w' and h' , respectively, are isomorphic to those of G and H . In addition, the above transformation multiplies by $\sqrt{\mu/\lambda}$ the length of every path in G and by $\sqrt{\lambda/\mu}$ the length of every path in H .

Consequently,

$$w' h' = w \sqrt{\mu/\lambda} h \sqrt{\lambda/\mu} = wh = A$$

and

$$\frac{h'}{w'} = \frac{h \sqrt{\lambda/\mu}}{w \sqrt{\mu/\lambda}} = \frac{h}{w} \frac{\lambda}{\mu} = \lambda.$$

Example 2: Fig. 4(a) shows a five block floorplan whose x -graph and y -graph are given in Fig. 4(b) and the actual layout is shown in Fig. 4(c). The aspect ratio of the above assembly is 1. Fig. 5(a) shows the transformed graphs obtained by multiplying each arc of G by 2 and each arc of H by $1/2$. The layout corresponding to G' and H' is shown in Fig. 5(b) with aspect ratio $1/4$.

The area of a layout consists of areas occupied by blocks and unoccupied areas between them. The latter is considered as wasted and we wish to reduce it as much as possible.¹ We may ask whether under the assumption of nonrestricted aspect ratio of building blocks, there exists an assignment of lengths to the arcs of G and H such that

¹A typical layout algorithm of VLSI chips requires some area between blocks for the inter-block connections. If this area is estimated and then added to the block area, the remaining unoccupied area can be considered wasted.

a zero wasted area layout is obtained. Notice that if such a layout exists, then according to Lemma 1, a whole family of layouts can be obtained by applying a uniform stretch transformation to all building blocks (the term uniform stretch means that one dimension is stretched while the other is contracted by a reciprocal magnitude).

We attempt to characterize the zero wasted area layout by proving necessary and sufficient conditions on G and H to represent such optimal layouts. We begin by proving some properties of the paths in G .

Lemma 2: Let $G(U, E, \bar{x})$ be an acyclic directed graph with a single source, a single sink, and arc lengths $\bar{x}$. Then,

- 1) each arc belongs to some path from source to sink, and
- 2) if every $e \in E$ belongs to some critical path, then all the paths from source to sink are critical.

Proof: Let u_1 and u_m denote the source and the sink, respectively. Consider an arc (u_i, u_j) , $i \neq 1$, $j \neq m$. Since u_1 is the only source of G , there exists an arc (u_k, u_i) incident into u_i , and since G is acyclic, the vertices u_k , u_i , and u_m are distinct. If $u_k = u_1$ then u_i is reachable from the source, otherwise the process is repeated. Since G is a finite graph, after a finite number of such steps we establish a path from u_1 to u_i . Similarly, we can establish a path from u_j to u_m , which proves the first claim.

To prove the second claim, assume to the contrary that there exist a path Ω from source to sink which is not critical. Let $u_1, \dots, u_i, u_j, \dots, u_m$ denote the vertices along Ω . Let u_i be the last vertex on Ω such that the portion of Ω from u_1 to u_i is a path of maximal length connecting u_1 to u_i . Obviously $u_i \neq u_m$, otherwise Ω is critical. Therefore, the arc connecting u_i with u_j is not the longest path between these two vertices and a longer path between them must exist. This means that the arc from u_i to u_j cannot participate in any critical path, thus establishing a contradiction. ■

Lemma 3 (necessary condition): Let $G(U, E, \bar{x})$ and $H(V, F, \bar{y})$ be the x -graph and y -graph of some zero wasted area layout whose area is A . Let a_j be the area of the j th building block, $1 \leq j \leq b$, that is,

$$A = \sum_{j=1}^b x_j y_j = \sum_{j=1}^b a_j.$$

Then all the paths of G and H are critical.

Proof: Let Γ be a critical path of G and let w denote its length. Assume to the contrary that G contains a path Ω which is not critical. Then according to Lemma 2, there exists an arc $e \in E$ whose length is x which does not belong to any critical path of G . Let Γ_e be a path of maximal length from source to sink containing e and let w_e be its length. Then $w - w_e = \epsilon > 0$. We transform G and H into G' and H' as follows. G' is identical to G except that e is replaced by two consecutive arcs e' and e'' whose lengths are x and ϵ , respectively, as illustrated in Fig. 6. H' is identical to H , except that $f \in F$ (the dual of e) whose length is y , is replaced by two parallel arcs f' and

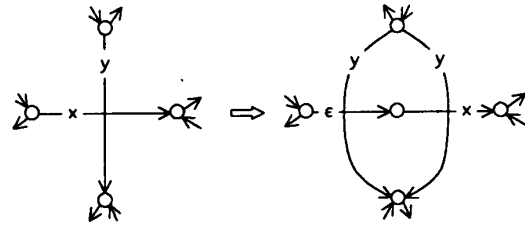


Fig. 6. Proof of Lemma 3.

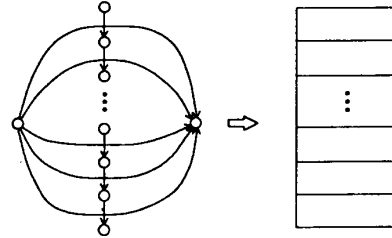


Fig. 7. Proof of Lemma 4. Maximum cardinality of a path in G equals 1.

f'' of length y each. Considering (e', f') and (e'', f'') as pairs of dual arcs, we ensure that G' and H' are dual graphs corresponding to a floorplan. The length of the critical paths in G' and H' are the same as that of G and H . Hence they impose a layout whose area is A with $b+1$ blocks, where (e'', f'') is a pair of dual arcs corresponding to the additional block. Consequently,

$$A \geq \sum_{j=1}^{b+1} x_j y_j = \sum_{j=1}^b x_j y_j + \epsilon y > \sum_{j=1}^b a_j = A$$

which is a contradiction. Therefore, all the paths in G and H are critical. ■

The following lemma proves that the equality of the length of all paths in G and similarly for H is sufficient to obtain a zero wasted area layout.

Lemma 4 (sufficient condition): Let $G(U, E, \bar{x})$ and $H(V, F, \bar{y})$ be the x -graph and y -graph corresponding to some floorplan implying a layout whose area is A , and let a_j be the area of B_j , $1 \leq j \leq b$. If all the paths from source to sink in G and H are critical, the layout has zero wasted area, i.e.,

$$A = \sum_{j=1}^b a_j.$$

Proof: The proof proceeds inductively on the maximal cardinality of a path in G (the cardinality of a path is the number of arcs along it). When the maximum cardinality is 1, the condition is trivially sufficient, as shown in Fig. 7. Here all the paths are of cardinality 1, and since they are all critical, all the arcs of G are equally long. In H there is a single path which is obviously critical. Therefore,

$$A = wh = w \sum_{j=1}^b y_j = \sum_{j=1}^b x_j y_j = \sum_{j=1}^b a_j$$

which means that there is no wasted area.

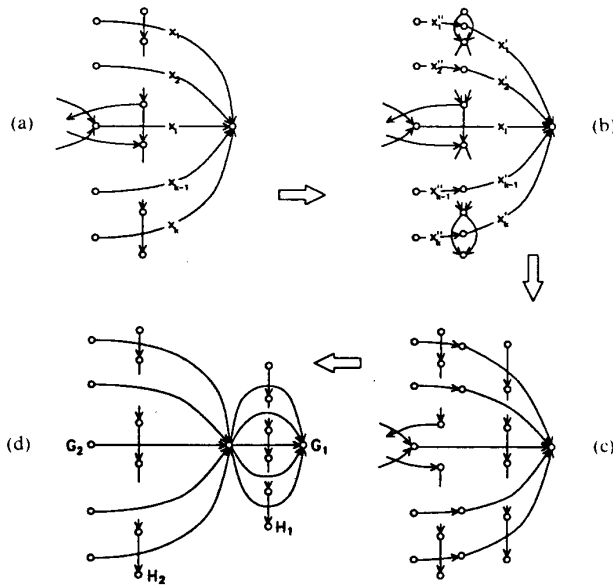


Fig. 8. Proof of Lemma 4. Reducing the maximum cardinality of a path in G .

Assume that the lemma holds for maximal cardinality not greater than $n-1$, and let G have some paths with maximal cardinality n . We show that the cardinality of any path consisting of n arcs can be reduced to $n-1$ by applying a finite series of transformations to G and H preserving the layout area. Assume that k arcs e_j whose length are x_j , $1 \leq j \leq k$, are connected to the sink of G as illustrated in Fig. 8(a). Let $x_l = \min_{1 \leq j \leq k} x_j$. Every arc e_j for which $x_j > x_l$ is replaced by two consecutive arcs e'_j and e''_j whose lengths are $x'_j = x_l$ and $x''_j = x_j - x_l$, respectively. The corresponding dual arcs in H are replaced by two parallel arcs having the same length, as shown in Fig. 8(b). The layout implied by the new dual digraphs has the following properties:

- 1) The lengths of the critical paths in the new G and H are the same as that of the critical paths in the original G and H .
- 2) The total sum of block areas in the new G and H equals to that of the original G and H .

The new graphs are further transformed as follows. The tail and the head vertices of the parallel arcs in H are each replaced by two vertices as illustrated in Fig. 8(c). The two resulting paths in H are disjoint and equally long. Finally, the new vertices which have been introduced into G , and the tail vertex of e_j are all combined into a single vertex, thus resulting in a separable x -graph with components G_1 and G_2 as shown in Fig. 8(d). Let H_1 and H_2 denote the corresponding y -graphs. The layout imposed by (G_1, H_1) has zero wasted area as proved formerly. Furthermore, the two resulting layouts have the same height since the critical paths of H_1 and H_2 have the same length and they can be matched without wasting area. Therefore, if (G_2, H_2) imposes a zero wasted area layout the lemma is proved. At

least one path in G_2 has a cardinality lower than that of the corresponding path in G . If we employ the above series of transformations repetitively to (G_2, H_2) , then after a finite number of steps the maximal cardinality of any path in G must be reduced to $n-1$ (or lower), resulting in a pair of dual graphs (G, H) that satisfy the induction hypothesis. ■

Lemm 3 and 4 are summarized in the following theorem.

Theorem 2: The layout implied by two dual x -graph and y -graph has zero wasted area if and only if every path in these graphs is critical. ■

The above necessary and sufficient condition for zero wasted area layout provides a basis for a scheme to find this layout when the areas of the building blocks are given. Using the path matrices K and L defined in (3.1), a solution of the system

$$\sum_{j=1}^b K_{ij} x_j - w = 0, \quad 1 \leq i \leq k \quad (3.7)$$

$$\sum_{j=1}^b L_{ij} y_j - h = 0, \quad 1 \leq i \leq l \quad (3.8)$$

$$x_j y_j = a_j, \quad 1 \leq j \leq b \quad (3.9)$$

$$wh = \sum_{j=1}^b a_j = A \quad (3.10)$$

that satisfies $x_j > 0$, $y_j > 0$, $w > 0$, and $h > 0$, yields the desired layout.

Notice that according to Lemma 4, an arbitrary feasible solution of (3.7) and (3.8) provides a zero wasted area layout. Then, (3.10) is automatically satisfied. In addition, since

$$\sum_{j=1}^b x_j y_j = \sum_{j=1}^b a_j = wh = A$$

an arbitrary equation from the set (3.9), e.g., for $j = b$, may be omitted. The $b-1$ remaining equations imply that

$$x_b y_b = A - \sum_{j=1}^{b-1} x_j y_j = A - \sum_{j=1}^{b-1} a_j = a_b.$$

With respect to the linear part (3.7) and (3.8) of the system, the number of independent equations is defined in the following.

Lemma 5: Let Q be a $(k+l) \times 2b$ matrix defined as follows:

$$Q = \begin{pmatrix} K & 0 \\ 0 & L \end{pmatrix} \quad (3.11)$$

where K and L are defined in (3.1). Then, the rank of Q equals $b+1$.

Proof: Assume that G and H contain m and n vertices, respectively. Let us augment G and H by adding to each of them a $(b+1)$ th arc directed from the sink to the source. The path matrices K and L defined in (3.1) are thus modified to circuit matrices $\bar{K}$ and $\bar{L}$ corresponding to the extended graphs $\bar{G}$ and $\bar{H}$, respectively, by adding a $(b+1)$ th column of -1 's to each of them.

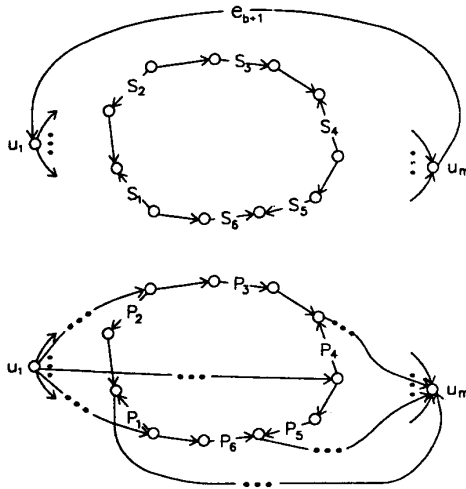


Fig. 9. Proof of Lemma 5.

Consider first $\bar{G}$ and the corresponding circuit matrix $\bar{K}$. Let u_1 and u_m denote its source and sink, respectively, and $C_{\bar{G}}$ denote the full circuit matrix corresponding to the set of all $\bar{G}$'s circuits.² As is well known [14], there exists

$$\begin{aligned} \text{rank } C_{\bar{G}} &= \# \text{ arcs} - \# \text{ vertices} + 1 = (b+1) - m + 1 \\ &= b - m + 2. \end{aligned} \quad (3.12)$$

$\bar{K}$ is a submatrix of $C_{\bar{G}}$, and, therefore,

$$\text{rank } \bar{K} \leq b - m + 2. \quad (3.13)$$

Take now an arbitrary row c_q of $C_{\bar{G}}$ and let S be its corresponding circuit in $\bar{G}$. It may happen that S contains the additional arc (u_m, u_1) . In such a case, the rest of S presents a path from u_1 to u_m , and c_q is up to a sign identical with some row of the matrix $\bar{K}$. If however, the arc (u_m, u_1) does not belong to S , we partition S into a sequence of sections $S = (S_1, S_2, \dots, S_r)$, such that the direction of the arcs along each section is preserved, and the directions of every two consecutive sections alternate, as illustrated in Fig. 9(a). It can be readily verified that r must be an even number (see Lemma 6 in Section IV). Without loss of generality we may assume that the odd sections S_{2i-1} , $1 \leq i \leq r/2$ are clockwise directed, while the even sections S_{2i} , $1 \leq i \leq r/2$ are counterclockwise directed. Applying the same technique as in Lemma 1, we may extend each of the above sections to a path starting at u_1 and ending at u_m . In case of a vertex common to two leaving consecutive sections, the extending path connects the source to this vertex, while in the case of two entering consecutive sections, the common vertex is connected to the sink, as illustrated in Fig. 9(b). Let P_j , $1 \leq j \leq r$ denote the paths corresponding to the sections of S . To each of these paths augmented by the additional arc (u_m, u_1) there

is a corresponding row $\bar{k}_{P_j}$ in the circuit matrix $\bar{K}$ satisfying

$$c_q = \sum_{i=1}^{r/2} \bar{k}_{P_{2i-1}} - \sum_{i=1}^{r/2} \bar{k}_{P_{2i}} \quad (3.14)$$

since each of the terms corresponding to an extension of a section appears in (3.14) twice, once with a plus sign and once with a minus sign, as can be seen from Fig. 9(b). Consequently, all the terms corresponding to the extensions will cancel out.

Equation (3.14) proves that the rows of $\bar{K}$ are a basis of $C_{\bar{G}}$, and, therefore,

$$\text{rank } \bar{K} = b - m + 2. \quad (3.15)$$

We show now that the $(b+1)$ th column of $\bar{K}$ (consisting of -1 's) is linearly dependent on the first b columns. Let $\bar{x} = (x_1, \dots, x_b)$ be a real vector satisfying (3.7),³ and let $\bar{1}_k$ be a k -vector of 1 's. Then, (3.7) can be rewritten as

$$\frac{1}{w} K \bar{x} = \bar{1}_k \quad (3.16)$$

thus proving the linear dependency. Consequently,

$$\text{rank } K = \text{rank } \bar{K} = b - m + 2. \quad (3.17)$$

Similarly, we can prove that the matrix L satisfies

$$\text{rank } L = b - n + 2. \quad (3.18)$$

Recall that the vertices of G and H correspond to the vertical and the horizontal line segments of the floorplan, respectively. We claim that the total number of line segments in a floorplan equals $b+3$. This can be shown by applying the Euler theorem of planar graphs, which says that if G has m vertices, f faces, and b arcs, then $m + f = b + 2$ (the outer face is included) [4]. Let n be the number of vertices in H . Then $n = f + 1$ since the outer face of G contains two vertices of H . Combining these two equalities, we conclude that $m + n = b + 3$, where by definition, $m + n$ is the total number of segments in the floorplan. Now, from (3.11), (3.17), and (3.18) we conclude that

$$\text{rank } Q = \text{rank } K + \text{rank } L = 2b - (m + n) + 4 = b + 1 \quad (3.19)$$

which proves the lemma. ■

Summarizing the above discussion, we notice that for a given w and h , such that

$$wh = \sum_{j=1}^b a_j = A$$

the number of unknowns and the number of independent equations are both equal to $2b$. There remain the questions whether there exists always a feasible solution of the system (3.7)–(3.9), and (if the answer to the first question is affirmative) whether the solution is unique (up to the

²In the full circuit matrix of a digraph the rows correspond to oriented circuits and the columns correspond to arcs. The (i, j) element equals 1 if circuit i contains arc j and their directions coincide. It equals -1 if circuit i contains arc j and they have opposite directions and it equals 0 if circuit i does not include arc j .

³It is shown in Section IV that it is always possible to assign lengths to the arcs of G such that all its paths are critical.

transformation discussed in Lemma 1). The following theorem answers these questions.

Theorem 3 (existence and uniqueness): A solution corresponding to a zero wasted area always exists, and it is unique up to a uniform stretch transformation.

Proof: Without loss of generality we may assume that $w = h = \sqrt{A} = z$, since according to Lemma 1, if a solution exists, we can get any w and h satisfying $wh = A$ by applying a uniform stretch transformation. Let us define the following two sets in $\mathbb{R}^{2b}$:

$$S_z = \left\{ (\bar{x}, \bar{y}) \mid \sum_{j=1}^b K_{ij} x_j - z = 0, \quad 1 \leq i \leq k; \right. \\ \left. \sum_{j=1}^b L_{ij} y_j - z = 0, \quad 1 \leq i \leq l \right\} \quad (3.20)$$

$$T = \{ (\bar{x}, \bar{y}) \mid x_j y_j \geq a_j, x_j > 0, y_j > 0, \quad 1 \leq j \leq b \}. \quad (3.21)$$

The set S_z defined in (3.20) is a subspace in $\mathbb{R}^{2b}$ (whose dimension equals $b-1$ since according to Lemma 5 the rank of Q in (3.11) equals $b+1$). The set T defined in (3.21) is convex and closed since it is an intersection of b convex closed sets. It is not difficult to see that $(\bar{x}, \bar{y}) \in T$ is an extremal point⁴ if and only if it satisfies $x_j y_j = a_j$, $1 \leq j \leq b$. S_z and T must satisfy one and only one of the following possibilities:

- 1) S_z supports T ,
- 2) $S_z \cap T \neq \emptyset$, and the intersection contains an internal point of T ,
- 3) $S_z \cap T = \emptyset$.

Fig. 10 provides a simplified illustration of these possibilities. Let us examine each one of them. In the first one, the points common to S_z and T are boundary points of T . It is well known that a subspace supporting a convex set must contain at least one of its extremal points [5]. Let $(\bar{x}^*, \bar{y}^*)$ be that point. Therefore, (3.7)–(3.9) are satisfied and $(\bar{x}^*, \bar{y}^*)$ provides a zero wasted area layout.

We show now that the other two cases are impossible. Let $(\bar{x}^*, \bar{y}^*) \in S_z \cap T$ be an internal point of T . Then, there exists some r for which $x_r^* y_r^* > a_r$. Assign x_j^* and y_j^* , $1 \leq j \leq b$, to the appropriate arcs and construct a layout. This layout satisfies (3.7) and (3.8) with $w = h = z$, implying a zero wasted area. Therefore,

$$A = z^2 = \sum_{j=1}^b x_j^* y_j^* + x_r^* y_r^* > \sum_{j=1}^b a_j = A \quad (3.22)$$

which is impossible. For the third case, let us define z^* as follows

$$z^* = \sup \{ z \mid S_z \cap T = \emptyset \}. \quad (3.23)$$

Then, $z^* > z$ and S_{z^*} supports T at an extremal point

⁴A point of a convex set is called extremal if it cannot be a midpoint of any other two different points belonging to the convex set.

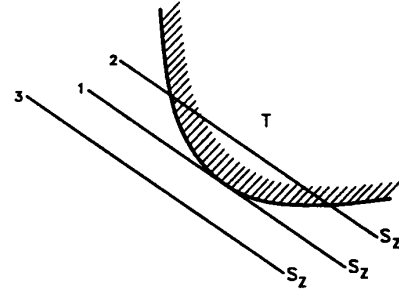


Fig. 10. Proof of Theorem 3.

$(\bar{x}^*, \bar{y}^*)$ satisfying $x_j^* y_j^* = a_j$, $1 \leq j \leq b$. Here again we assign x_j^* and y_j^* to the appropriate arcs and construct a layout which satisfies

$$A = \sum_{j=1}^b a_j = \sum_{j=1}^b x_j^* y_j^* = (z^*)^2 > z^2 = A \quad (3.24)$$

which is impossible. This completes the proof of existence.

To prove uniqueness, assume that $(\bar{x}^1, \bar{y}^1)$ and $(\bar{x}^2, \bar{y}^2)$ are two different real positive solutions of (3.7)–(3.9) (they are necessarily extremal points of T). Define $(\bar{x}^3, \bar{y}^3)$ to be the mid point of $(\bar{x}^1, \bar{y}^1)$ and $(\bar{x}^2, \bar{y}^2)$. Since S_z is a subspace, $(\bar{x}^3, \bar{y}^3)$ satisfies (3.7) and (3.8). By definition, $(\bar{x}^3, \bar{y}^3)$ is not an extremal point of S_z , and, therefore, there exists some r for which $x_r^3 y_r^3 > a_r$. Let us build a layout whose block dimensions are (x_j^3, y_j^3) , $1 \leq j \leq b$. Following the same arguments as in the proof of the existence, we obtain the following contradiction:

$$A = z^2 \geq \sum_{j=1}^b x_j^3 y_j^3 + x_r^3 y_r^3 > \sum_{j=1}^b a_j = A. \quad (3.25)$$

Therefore, (3.7)–(3.10) have a unique real positive solution. ■

Example 3: We wish to find a zero wasted area floorplan corresponding to the graphs given in Fig. 4(b). The areas of the building blocks are given as follows: $a_1 = 15$, $a_2 = 6$, $a_3 = 28$, $a_4 = 21$, $a_5 = 30$. The total area of the layout is $A = \sum_{j=1}^5 a_j = 100$. According to Lemma 1, $w = h = 10$ are determined arbitrarily to satisfy (3.10). Equations (3.7)–(3.9) have the following solutions:

$$x_1' = 3, x_2' = 3, x_3' = 4, x_4' = 7, x_5' = 6$$

which is feasible, and

$$x_1'' = \frac{85}{14}, x_2'' = 10 - \frac{385}{64} - \frac{85}{14}, x_3'' = \frac{385}{64},$$

$$x_4'' = \frac{55}{14}, x_5'' = \frac{255}{64}$$

which are not feasible since $x_2'' < 0$. Recall that a feasible solution implies a family of layouts whose aspect ratios are determined arbitrarily. ■

Example 4: Fig. 11(a) depicts a 20-block floorplan where the desired area of each block appears at the center of the appropriate region. The corresponding G and H were

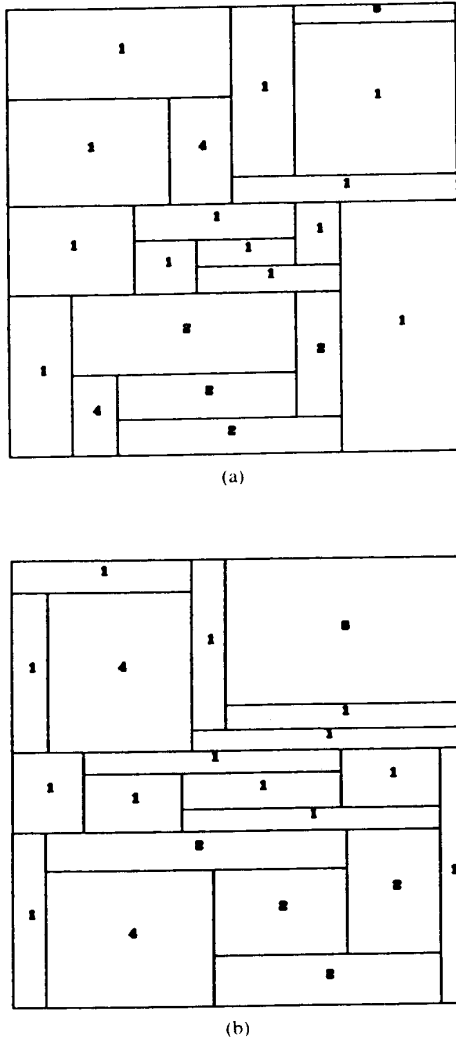


Fig. 11. 20-block floorplan and the implied zero wasted area layout.

derived by a computer program. Equations (3.7)–(3.10) were then solved and the resulting layout is shown in Fig. 11(b). We can see that all the blocks' dimensions match, yielding a zero wasted area layout. ■

3.2. Constrained Aspect Ratios

A more realistic situation is of constrained aspect ratios of the building blocks. For example, a block in VLSI may have an aspect ratio from some restricted interval determined by the various possibilities of implementation. In architecture, the aspect ratio of a room cannot assume any arbitrary value but must be such that the functionality of the room is retained. In the unconstrained case we have determined necessary and sufficient conditions for zero wasted area layouts. The existence of this optimal situation in the constrained case is discussed in the following corollary.

Corollary 2.1: Let the aspect ratio y_j/x_j of B_j be constrained in a given interval $[\alpha_j, \beta_j]$, $1 \leq j \leq b$. A zero wasted

area layout exists if the aspect ratios $\bar{\lambda} = (\lambda_1, \dots, \lambda_b)$ of the corresponding unconstrained case satisfy

$$\bigcap_{j=1}^b \left[\frac{\alpha_j}{\lambda_j}, \frac{\beta_j}{\lambda_j} \right] \neq \emptyset.$$

Proof: According to Lemma 1 and Theorem 3, $\bar{\lambda}$ is uniquely determined up to a real positive multiplying factor. Let $\kappa \in \bigcap_{j=1}^b [\alpha_j/\lambda_j, \beta_j/\lambda_j]$. Lemma 1 shows that if the aspect ratio of each block is multiplied by κ , the area of the layout whose building blocks' aspect ratios are $\lambda_1, \dots, \lambda_b$ is preserved. Since $\alpha_j \leq \kappa \lambda_j \leq \beta_j$, $1 \leq j \leq b$, a zero wasted area layout for the constrained case does exist. ■

Corollary 2.1 characterizes the situation of zero wasted area for the case of aspect ratios constrained in finite intervals. However, it may happen that the condition in corollary 2.1 is not satisfied and some optimization algorithm must be employed to minimize the wasted area. A practical way to find a layout of minimum area is to approximate the aspect ratios, which in this discussion are continuous functions defined on some intervals, by a finite set of possible aspect ratios for each block, or by piecewise linear function. Under these approximations the problem of minimizing the layout area in slicing floorplans was solved by polynomial algorithms [12]–[15]. For general floorplans the problem is NP-complete [15] and an efficient *branch and bound* algorithm was presented in [18].

3.3. Flow Conditions for Zero Wasted Area Layout

The number of rows in K and L , k and l , respectively, may grow exponentially with the number of arcs in G and H (which equals the number of blocks). Therefore, solving (3.7)–(3.10) may be very tedious. We show in what follows that the $k + l$ path equations in (3.7)–(3.8) can be replaced by $b + 3$ flow equations. To this end, we first define two new graphs $G'(U, E, \bar{y})$ and $H'(V, F, \bar{x})$, which are isomorphic to G and H except their arc lengths which are obtained by interchanging the lengths of the arcs in each dual pair of G and H . Recall that there is one to one correspondence between paths in G and cutsets in H and vice versa [9], and similarly for G' and H' . Therefore, in case of a zero wasted area layout, the total weights of arcs in all the cutsets of G' and H' equal to h and w , respectively. This shows that we can interpret the arc weights as flows with the same flow passing through each cut.

Considering vertices, the above interpretation means that the out-flow of the source equals the in-flow of the sink (h in G' and w in H'), and for any other vertex, the in-flow equals the out-flow. Let m and n be the number of vertices in G' and H' , respectively. Let M be the $m \times b$ vertex-arc incidence matrix of G' , defined as follows:

$$M_{ij} = \begin{cases} 1, & \text{if } e_j \text{ leaves } u_i, \\ -1, & \text{if } e_j \text{ enters } u_i, \\ 0, & \text{otherwise.} \end{cases} \quad (3.26)$$

N is an $n \times b$ vertex-arc incidence matrix defined similarly for H' . The $k + l$ path equations in (3.7) and (3.8) can now

be replaced by the following $m + n$ flow equations of G' and H'

$$\sum_{j=1}^b M_{ij} y_j = 0, u_i \text{ is neither a source nor a sink} \quad (3.27a)$$

$$\sum_{j=1}^b M_{ij} y_j - h = 0, u_i \text{ is the source} \quad (3.27b)$$

$$\sum_{j=1}^b M_{ij} y_j + h = 0, u_i \text{ is the sink} \quad (3.27c)$$

$$\sum_{j=1}^b N_{ij} x_j = 0, v_i \text{ is neither a source nor a sink} \quad (3.28a)$$

$$\sum_{j=1}^b N_{ij} x_j - w = 0, v_i \text{ is the source} \quad (3.28b)$$

$$\sum_{j=1}^b N_{ij} x_j + w = 0, v_i \text{ is the sink.} \quad (3.28c)$$

Consequently, instead of $k + l$ path equations we have now only $m + n$ flow equations, and as was proved in Lemma 5, $m + n = b + 3$. We have thus reduced significantly the number of equations to be solved.

It is well known that the minimal cut in a planar network is equivalent to the shortest path in the dual network, where each dual arc is assigned the weight of its corresponding primal [9]. Equation (2.4) in Theorem 1 proves that given dual parametric networks whose arc lengths satisfy (2.1), the product of their shortest paths is bounded by $\sum_{j=1}^b x_j y_j$. Theorem 2 proves that this bound is achieved when all the paths in each graph are equally long. These results can now be applied to bound the product of the maximal flows in such networks.

Corollary 2.2: Let G and H be two dual networks, whose arc capacitance satisfy (2.1). Then, the product of their maximal flows is bounded by $\sum_{j=1}^b x_j y_j$, and this bound is achieved when all the cuts in each network pass the same flow. ■

IV. RECTILINEAR REPRESENTATION OF PLANAR GRAPHS

In Section II we saw how a floorplan can be represented by planar graphs. The floorplan is actually some rectilinear representation of these graphs. An interesting question is whether the converse exists, i.e., whether for any given planar graph there exists such a rectilinear representation. This question has also practical implications and the use of the rectilinear representation of a planar graph in the layout of MOS circuits is now under investigation. The existence question was studied in [16], where the following theorem is proved.

Theorem 4 (Thomassen [16]): If G is a 3-connected planar graph, then G has a representation in the plane such that the vertices of G correspond to vertical line segments and two vertices of G are adjacent if and only if the corresponding segments can be connected by an hori-

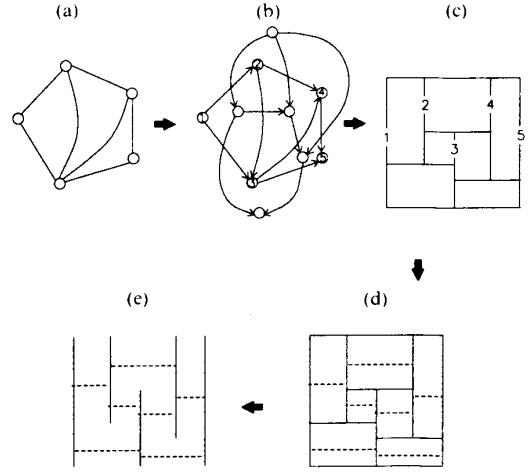


Fig. 12. Rectilinear representation of planar graphs.

zontal line segment not intersecting any other vertical line segment. ■

The proof of the above theorem in [16] is inductive and does not provide an efficient procedure to generate the rectilinear representation.

In what follows we obtain the above rectilinear representation by using the dual digraphs corresponding to a floorplan, and the layout they imply. The procedure is based on the observation that if the implied layout has zero wasted area, then the layout and the floorplan are identified. The steps of the procedure are outlined in the following:

- 1) Modify the given planar graph into an acyclic digraph having unique source and sink.
- 2) Obtain its dual, which is also an acyclic digraph having unique source and sink.
- 3) Assign lengths to the arcs of the dual graphs such that all their paths are critical.
- 4) Derive a zero wasted area layout (floorplan) from the above x -graph and y -graph.
- 5) The resulting floorplan is transformed to obtain the rectilinear presentation.

We next describe in detail the five steps of the procedure which are also illustrated in Fig. 12 which follows the above steps. In step (1) directions are assigned to the edges of the planar graph G , employing the *st-numbering* procedure [6]. Given any two vertices s and t of a nonseparable graph $G(U, E)$, this procedure generates a one to one function, $g: U \rightarrow \{1, 2, \dots, |U|\}$ satisfying:

- 1) $g(s) = 1$,
- 2) $g(t) = |U|$,
- 3) for every $u \in U - \{s, t\}$ there are adjacent vertices p and q such that $g(p) < g(u) < g(q)$.

In [6] an algorithm that produces an *st-numbering* in $O(|E|)$ time units is presented. We can choose any two vertices on the external face of our planar graph and designate them as s and t . Applying the *st-numbering*

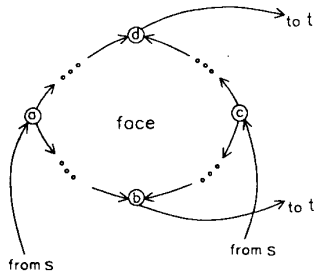


Fig. 13. Proof of Lemma 6.

procedure, a digraph is obtained in which s and t are the source and the sink, respectively.

In the second step we first construct the undirected dual of G , denoted by H . Then, directions are assigned to the arcs of H such that the orientation when going from the head of an arc in G to the head of its dual arc in H (clockwise or counterclockwise) is preserved. We have to prove that the resulting digraph is acyclic, with unique source and sink (i.e., H is st -numbered). Otherwise, it cannot yield a layout. This is proved through the following two lemmas.

Lemma 6: Let G be a nonseparable planar acyclic digraph with unique source and sink. Then, the direction of the arcs along any face is changed exactly twice.

Proof: Let s and t denote the source and sink, respectively. Obviously, the direction must be changed since G is acyclic. Also, the number of changes must be even. To prove it observe that any direction of the arcs along a face can be obtained by starting from a cycle where there are no changes in the direction. Then, reversing the direction of an arcs either adds two changes in the direction, or it does not add any change.

Assume to the contrary that the direction is changed more than twice. Consider first a face containing neither s nor t . There must be at least four vertices along the face such that two of them have only incoming arcs and two of them having only outgoing arcs, ordered as illustrated in Fig. 13. Since G is st -numbered, there exist paths connecting vertices a and c with s , and paths connecting vertices b and d with t . Since G is acyclic, the circuits $a - d - c - s - a$ and $b - c - d - t - b$ cannot have a common vertex which is not a part of the face, otherwise the planarity of G is contradicted. Similar considerations can be applied to the faces containing the source or the sink. ■

Lemma 6 proves that the external face of the x -graph is composed of two paths connecting the source to the sink, that is, an upper one and a lower one. Consider the vertex of H which is above the upper path of G . We may direct all the edges connected to this vertex of H and which cross the corresponding arcs on the upper path of G , in such a way that the direction of turning by an angle $\alpha < \pi$ an arc of G to its dual arc in H , so that their orientations coincide, is the same for all the dual arc pairs. Since all the arcs along the upper path of G have the same direction, directing the dual arcs of H results in a source. The sink of H is obtained similarly by the dual arcs of the lower path

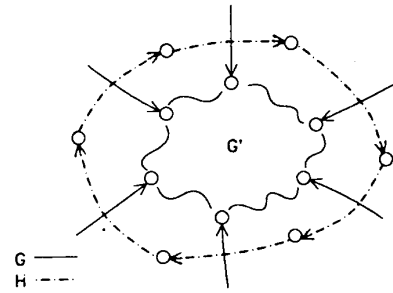


Fig. 14. Proof of Lemma 7.

of G . The above source and sink of H are unique since any other source or sink in H implies a cycle in G , which is impossible. We still have to show that H is acyclic.

Lemma 7: Let G be an acyclic planar digraph having unique source and sink. Then its dual is acyclic too.

Proof: Assume to the contrary that its dual H contains a cycle C . Then all the dual arcs of G are directed inwards (outwards), as illustrated in Fig. 14. Let G' denote the portion of G enclosed in C . Since G' has no cycles, it must have a source (and a sink). But this contradicts the fact that s is the only source of G . An alternative proof is to look at some vertex of G' . There is a path connecting this vertex to the sink. This path must have an edge going outward C , which again results in a contradiction. ■

In step (3) of the procedure we assign nonnegative real numbers to the arcs of G and H such that all their paths are critical. The assignment proceeds as follows. The directing of the arcs which follows the st -numbering process yields a graph in which an arc $u_j \rightarrow u_i$ is always directed from a vertex with a lower number to a vertex with a higher number. Initially the source (u_1) is labeled with zero, that is $l(u_1) = 0$, and all the other vertices are unlabeled. Let U_i be the set of all the vertices having an arc directed to u_i . Then, the label of u_i is defined by

$$l(u_i) = \max_{u_j \in U_i} \{l(u_j) + 1\}.$$

Let $u_k \in U_i$ be a vertex satisfying $l(u_k) = \max_{u_j \in U_i} l(u_j)$. Then the arc $u_k \rightarrow u_i$ is assigned the length 1. For the remaining vertices $u_m \in U_i$ the arc $u_m \rightarrow u_i$ is assigned the length $l(u_i) - l(u_m)$. The paths in the resulting graph are all critical.

In step (4) we construct a layout from $G(U, E, \bar{x})$ and $H(V, F, \bar{y})$. The resulting layout has zero wasted area since Theorem 2 states that the criticality of all the paths in the x -graph and y -graph is necessary and sufficient for a zero wasted area layout. The resulting layout can be treated as if it was a floorplan since they are now identified.

Finally, the floorplan constructed in the fourth step is trivially transformed to obtain the desired rectilinear representation. The floorplan is in one to one correspondence with the original planar graph, where a vertex corresponds to a vertical line segment, and an edge connecting two vertices corresponds to the sub-rectangle supported by the two corresponding vertical line segments. In each sub-rect-

angle we draw now a horizontal line segment passing through its center and extending up to its left and right edges. We then drop all the former horizontal line segments of the floorplan, yielding a representation that satisfies the conditions of Theorem 4. Fig. 12(e) illustrates the final result of the construction.

V. CONCLUSIONS

We have discussed in this paper the problem of minimizing the area of a layout, given its floorplan and the areas of its building blocks, by allowing the dimensions of these blocks to be determined arbitrarily. The floorplans considered are general ones and are not restricted to sliced floorplans. A necessary and sufficient condition for the existence of a zero wasted area layout was derived and its uniqueness was proved. Then, a closed form solution to generate it was presented. It was also proved that for a family of dual network pairs for which the product of dual arc length is invariant, the minimal product of their longest paths is not smaller than the maximal product of their shortest paths. Based on the zero wasted area layout analysis, we proved that the maximal product of the flows in such dual parametric networks is given by the total sum of the capacitance product of each individual pair of dual arcs. Finally, an efficient procedure to derive a rectilinear representation for any planar graph, based on the layout and floorplan graph model, was presented. There are other engineering applications where different geometric measures could be optimized and other constraints are imposed on the building blocks (like perimeter and diagonal). This suggests a class of optimization problems. It is an interesting question whether efficient solutions can be derived by taking advantage of the graph model, rather than applying some mathematical programming procedures which are in most cases time consuming.

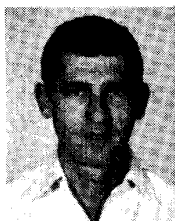
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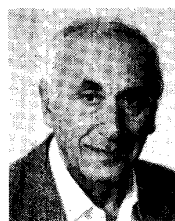
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