Impact of Nanomanufacturing Flow on Systematic Yield Losses in Nanoscale Fabrics

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***Abstract*—Reliable and scalable manufacturing of nanofabrics entails significant challenges. Scalable nanomanufacturing approaches that employ the use of lithographic masks in conjunction with nanofabrication based on self-assembly have been proposed. A bottom-up fabrication of nanoelectronic circuits is expected to be subject to various defects and identifying the types of defects that may occur during each step of a manufacturing pathway is essential in any attempt to achieve reliable manufacturing. The paper proposes a methodology for analyzing the sources of defects in a nano-manufacturing flow and estimating the resulting systematic yield loss. This methodology allows analyzing the impact of the fabrication process on the systematic yield. It integrates physical fabric considerations, manufacturing sequences and the resulting defect scenarios. This is in contrast to most current approaches that use conventional defect models and assume constant defect rates without analyzing the manufacturing pathway to determine the sources of defects and their probabilities (or rates). While the focus of the paper is on estimating the mask overlay-limited yield for the NASIC nano-fabric, the proposed approach can be easily adapted to suit other structured nano-fabrics.**

Keywords- mask alignment, overlay, nanowires, yield, mask offset

I. INTRODUCTION

Reliable manufacturing of integrated systems incorporating nanodevices such as semiconductor nanowires [1][2], spin waves [3], carbon nanotubes [4][5], and graphene [6] is still very challenging. Techniques such as reconfiguration and built-in fault tolerance have been studied for mitigation of permanent defects in nanoscale computing fabrics. Most of the prior publications have, however, focused on the impact of the assumed defects at device/circuit/architectural levels and have not analyzed the sources of the defects. For example, a modular approach is used by Patwardhan [7] to reprogram faulty 'nodes' (a functional block). Built-in defect tolerance for stuck-on or stuck-off devices (with up to 10% defect rates) has been considered for the NASIC fabric[8][9][10][11][12][13]. Switches that may not be programmable due to defects have been considered for the CMOL fabric [14], but mask overlay aspects were not discussed in detail. Mask overall/registration is likely to be the critical source of defects at the nanoscale.

Our goal in this paper is to analyze the sources of defects from a manufacturing perspective rather than assuming a fixed distribution and consider mask overlay introduced defect sources carefully. Identifying the defects that may occur during each step of the bottom-up fabrication of nanoelectronic circuits is important since it would enable a better estimate of the defect rates, thereby allowing a more accurate yield analysis and enable a better comparison of various manufacturing flows, and fabric directions.

Scalable nanofabric manufacturing techniques have been proposed which utilize lithography masks for functionalization and interfacing in conjunction with nanofabrication based on self-assembly based approaches [10][15]. Each step in the manufacturing process can be viewed as a combination of "alignment of a mask for pattern transfer" followed by a "processing step." Defects can be introduced during (a) the alignment of the mask, or (b) the processing step after the mask alignment, and can also be the result of (c) impurities during the manufacturing steps. Defects introduced during the mask alignment are commonly classified as systematic defects; whereas the defects introduced during the processing step can be either random or systematic. Impurity related defects are random in nature and are expected to result in a considerably smaller yield loss.

Mask-overlay-limited yield is a key contributor to yield loss even in CMOS. For example, yield loss of approximately 10% is attributed to mask overlay in fabrication of memory in sub-90nm CMOS technology [16]. A thorough analysis of the systematic yield loss due to mask overlay must therefore be carried out for nanofabrics. We propose in this paper a methodology for analyzing the yield implications of mask overlay on nanoscale designs. While, for concreteness, the methodology is presented in the context of NASICs [8][9][10][11][12][13], where a preliminary manufacturing flow has been established; the approach can be modified to model other structured nano-fabrics as well.

The yield evaluation has been carried out using a scalable manufacturing pathway that focuses on realizing the NASIC fabric with incorporated contacts, interconnects and devices [10], and using the overlay misalignment tolerance projected

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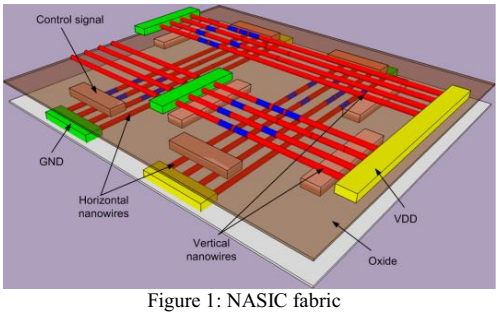

Figure 1: NASIC fabric

by ITRS [17]. Yield predictions obtained using the proposed methodology would be more realistic and help us gain a perspective on the adopted manufacturing flow through: (a) the yield implications of the nanowire alignment step, (b) yield loss associated with successive mask overlays, and (c) yield implications for different overlay requirements.

The key contributions of this paper are: (i) estimation of yield loss associated with successive mask overlays, (ii) analysis of the yield implications of different overlay requirements, (iii) sensitivity of the overall yield to the choice of physical fabric design parameters.

The rest of the paper is organized as follows: Section II describes the background work and motivation, Section III discusses alignment, mask offset, and overlay requirements, Section IV presents the modeling of mask overlay, Section V describes the experiments and results, and finally, Section VI concludes the paper.

II. Background Work And Motivation

Mask registration/mask offset may be defined as the difference $(\Delta x, \Delta y)$ between the actual position of a feature on a substrate and its intended position. Mask overlay error is defined as the displacement error of an exposed photo image (feature) relative to a previously exposed image (feature). It can hence be expressed as $(\Delta x_1 - \Delta x_2, \Delta y_1 - \Delta y_2)$ for any two successive masks in the manufacturing sequence. In order to achieve the required functionality, the lithographic masks in the fabrication must overlay each other to within acceptable tolerance. Mask overlay has been a key design issue even in CMOS. Critical layer mask pairs such as active-to-gate, gate-to-contact, and contact-to-metal have been traditionally analyzed for overlay related errors [16]. Active-to-gate mis-registration can result in gate leakage or reduced static noise margin. Gate-to-contact mis-registration can result in shorts and functional failures. Contact-to-metal mis-registration quite often results in resistive or open interconnect [16]. As the number of metal layers increases in CMOS, the probability of a metal-to-via overlay failure also increases.

To build a nanofabric in a scalable fashion, lithography needs to be used for functionalization (e.g., drain/source regions and locations of nanodevices) and for interfacing to

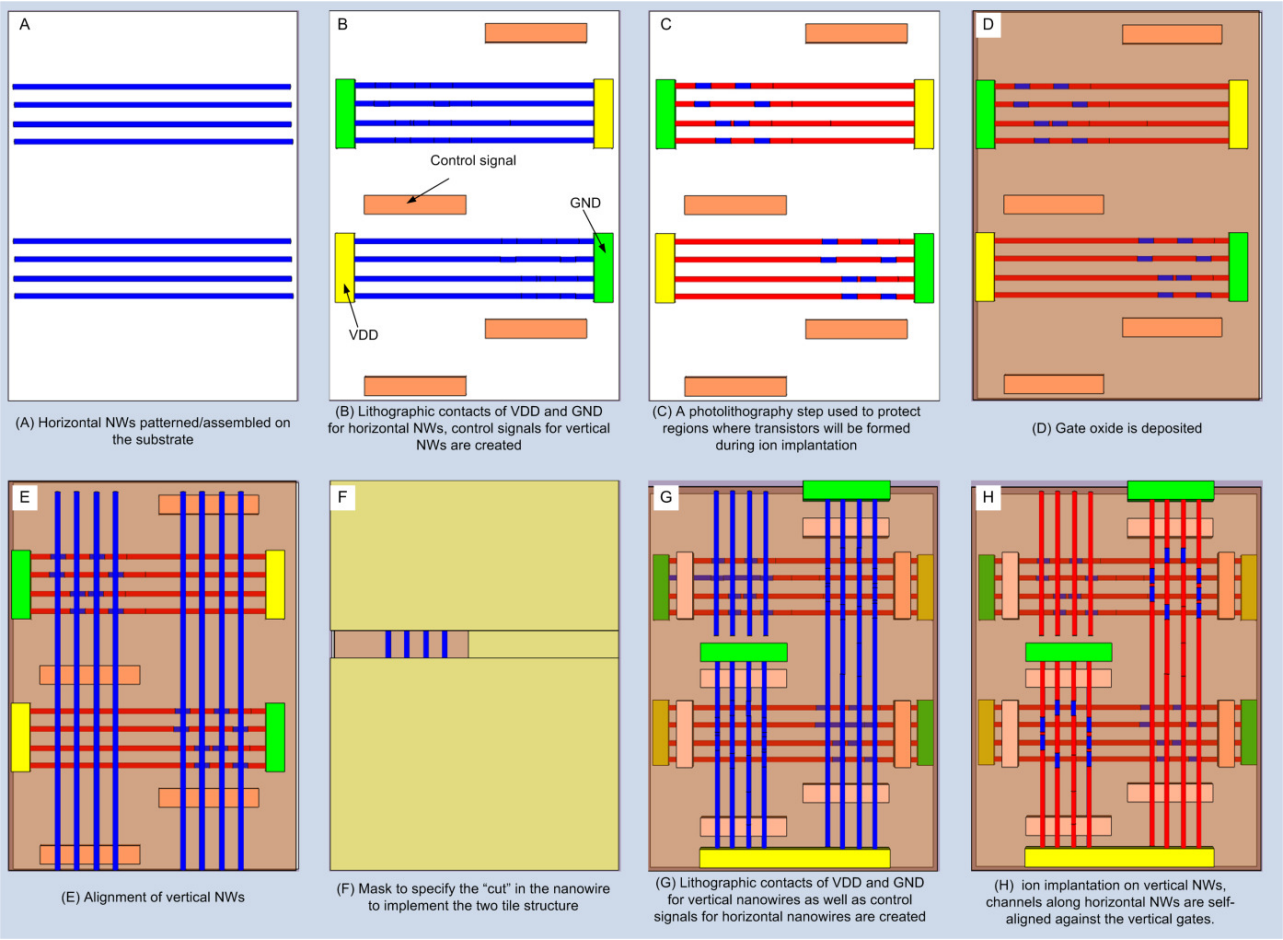

Figure 2: NASIC's manufacturing sequence using "two nanowire transfer"

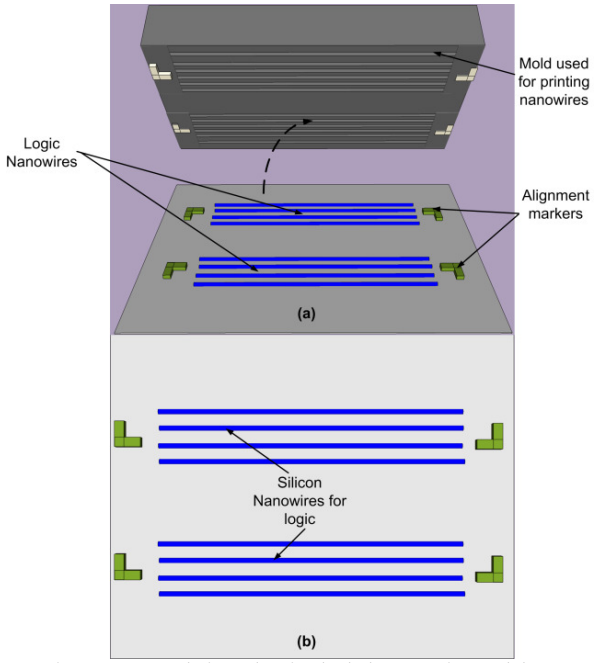

Figure 3: NIL technique showing both the nanowires and the alignment markers in the same mold

external CMOS. For example, Cerofolini *et al.* have described terascale integration and arrangement of Si-nanowires [15]. Narayanan *et al.* have proposed a manufacturing pathway and described the associated challenges for nanoscale systems [10] using a combination of unconventional and photolithographic manufacturing steps. This implies that mask overlay and registration requirements as well as the systematic yield implications for emerging nanofabrics need to be carefully examined. The questions that should be answered include: What kinds of defects are introduced due to mask overlays in the considered nanomanufacturing sequence? What is the yield loss associated with successive mask overlays? How do yield losses change for different overlay requirements? How sensitive is the overall yield to the choice of physical fabric design parameters (e.g., pitch/width of nanowires)?

We have carried out a detailed analysis of systematic sources of defects for the manufacturing pathway proposed in [10]. This pathway focuses on realizing the NASIC fabric (see Fig. 1) incorporating all the required contacts, interconnects and devices. Fig. 2 shows the manufacturing sequence. Horizontal NWs are grown and aligned on a substrate (Fig 2A); Lithographic contacts for VDD and GND for horizontal nanowires as well as control signals for vertical nanowires are then created (Fig. 2B). A photolithography step is used to protect regions where transistors will be formed while creating high conductivity regions (using ion implantation) elsewhere (Fig. 2C). Gate dielectric layer is then deposited (or oxide is grown) (Fig. 2D) followed by alignment of vertical NWs (Fig. 2E).The next mask is used to "cut" the nanowires using an etch-back process to implement the two tile structure (Fig. 2F) [8]. Lithographic contacts of VDD and GND for vertical nanowires as well as control signals for horizontal nanowires are created (Fig. 2G). During ion implantation on vertical NWs (Fig. 2H), channels along horizontal NWs are self-aligned against the vertical gates.

The following nano-manufacturing issues need to be considered in the proposed methodology:

1) The total number of masks required to realize the fabric is much less than that for a conventional CMOS design. This is intuitive because: a) NASIC circuits require very limited customization: only one type of FET [13] is used in the logic portions of the design and there is no requirement for arbitrary placement or sizing of devices; b) Devices and interconnects are achieved on the nanowire grid itself in a single functionalization step; interconnection of devices does not require a metal stack.

2) Lithographic masks are required at the following manufacturing steps: (a) Creation of VDD and GND contacts for horizontal nanowires along with control signals for vertical nanowires (Fig. 2B), (b) Functionalization of horizontal nanowires (Fig. 2C), (c) Mask used to specify the cut in the nanowires during etch-back process (Fig. 2F), (d) Creation of VDD and GND contacts for vertical nanowires along with control signals for horizontal nanowires (Fig. 2G), and (e) Functionalization of vertical nanowires (Fig. 2H). All masks except the one used to cut nanowires using an etch-back process will be considered in our systematic yield analysis. The mask used for etch-back has high tolerance for overlay imprecision (i.e., it does not introduce any defects when misaligned in the range specified by ITRS; lithographically defined regions to cut the nanowires are of dimensions larger than the minimum feature size and hence greater tolerance is achieved).

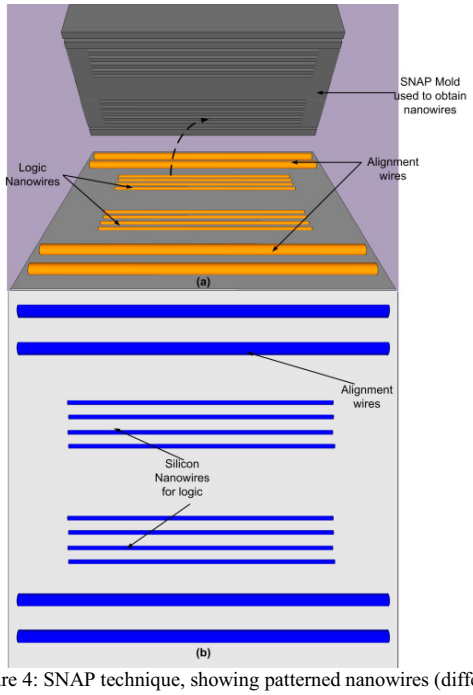

Figure 4: SNAP technique, showing patterned nanowires (different dimension than logic nanowires) which can be used as alignment markers for moire patterning

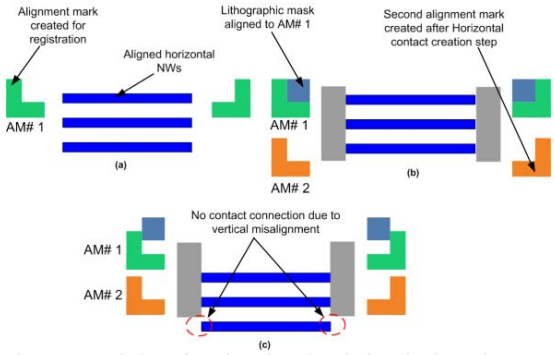

Figure 5: Depiction of mask registration during "horizontal contact creation" step

III. ALIGNMENT, MASK OFFSET AND OVERLAY

Several techniques have been proposed for nanowire alignment. *In-situ*, *ex-situ* and unconventional patterning approaches are being studied for formation of aligned nanowire arrays. Superlattice Nanowire Pattern Transfer (SNAP) has been demonstrated for silicon nanowire arrays at 13nm pitch and 8nm width [18]-[19]. *Ex-situ* processes employ techniques such as the Langmuir-Blodgett technique [20]-[21], fluidic-guided method [22], electric field guided assembly [23], or organic self-assembly [24]-[25], to align the semiconductor nanowires that are synthesized elsewhere (through techniques such as Vapor-Liquid-Solid (VLS) growth) to produce almost parallel nanowires array.

It should be noted that nanowire assembly is carried out prior to any lithographic step without any overlay requirement. In the case of techniques like NIL [26], alignment markers for registering against photolithographic steps are created in conjunction with the logic nanowire array using a single mold as shown in Fig. 3. For techniques like SNAP, patterned nanowires (of a different dimension than that of the logic nanowires) can be used as alignment markers (Fig. 4), since arbitrary alignment patterns may be difficult. The alignment nanowires would form Moire patterns/fringes [27]-[28] for alignment. The creation of markers for registration is accomplished in the same step using the same mold/superlattice as the logic nanowires and is therefore self-aligned.

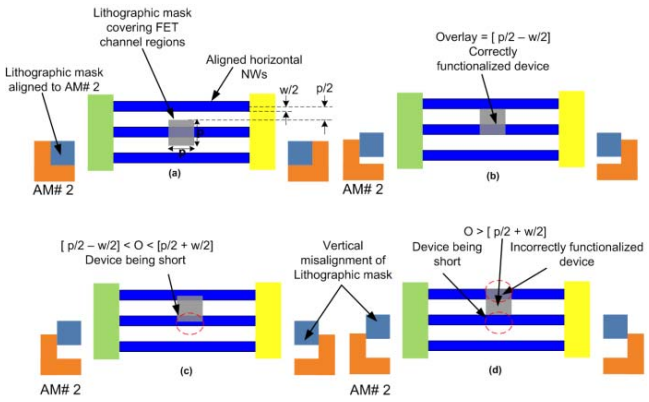

Figure 6: Depiction of the mask overlay effect during the "Horizontal Functionalization" step

The underlying arrangement of the uniform and regular nanowires allows the first lithographic mask to be "offset" horizontally with tolerance on the grid and still achieve correct functionality. The effect of mask offset (registration or alignment of the first lithographic mask) can be envisioned as shown in Fig. 5. A uniform parallel array of nanowires is first patterned (or assembled). The accompanying alignment marks (i.e., AM#1 in Fig. 5a) are also simultaneously created for registration purposes. During the alignment of the first mask (e.g., to create metal contacts, Fig. 2B), AM#1 will be used as the alignment target (Fig. 5b). An excessive offset in the y-direction can potentially result in defective chips (Fig. 5c), with some nanowires not being contacted to power rails. New alignment markers should also be created for subsequent steps. As shown in Fig. 5b,c new alignment patterns (AM#2), are defined on the photoresist in addition to contact patterns for the current step. After the development of the photoresist, the intended process is carried out. For example, metal deposition to create contacts and control may be carried out. Metal markers (AM#2) would then be created on the substrate itself and used as alignment targets for the subsequent step.

After creating the contacts, functionalization is done to define the positions of devices and interconnects on the horizontal nanowire array (Fig. 2C). Lithographically defined regions with a minimum size of (pitch × pitch) squares are blocked out, and ion-implantation/metallization is done elsewhere.

Fig. 6 shows transistor defects that arise from misalignment of this mask. Fig. 6a shows the correct alignment scenario. Pitch and width parameters are labeled as 'p' and 'w'. A vertical misalignment of up to (p – w)/2 may be tolerated without any defects in this step (Fig. 6b). A misalignment greater than this value would result in shorted channels across the horizontal nanowire array, leading to yield loss (Fig. 6c). While at this point the chip is already defective, for completeness, a case where both incorrectly shorted and incorrectly functionalized devices are created, is shown (see Fig. 6d) when the misalignment exceeds (p+w)/2. This cannot

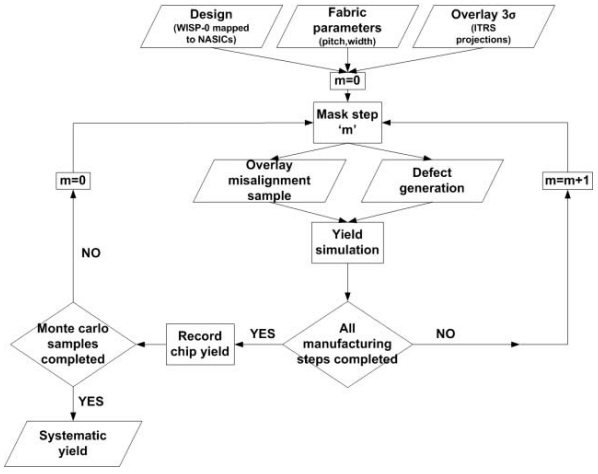

Figure 7: Proposed methodology for yield estimation to predict the systematic yield loss due to mask overlay

Year of Prod	mask overlay(nm)	MPU gate in resist (nm)
2009	10.3	47
2010	9	41
2011	8	35
2012	7.1	31
2013	6.4	28
2014	5.7	25
2015	5.1	22
2016	4.5	20
2017	4	18
2018	3.6	16
2019	3.2	14
2020	2.8	12
2021	2.5	11
2022	2.3	10
2023	2	9
2024	1.8	8

Figure 8. Overlay values as projected by ITRS

be envisioned as shifting the design 'up' by a nanowire pitch, since the contacts are already defined in a previous step. It must be noted that additional markers will also be created in this step similar to Fig. 5; however, these have not been shown for clarity.

IV. MODELING OF MASK OVERLAY

The effect of mask overlay misalignment for successive masks in the NASIC manufacturing sequence was studied through simulation. The overlay misalignment between successive masks was modeled as a Gaussian random variable. As discussed in the previous section, all possible defect scenarios for a given manufacturing step and a sampled value of overlay misalignment were carefully modeled using a custom simulator.

The overall methodology for yield estimation is shown in Fig. 7. Inputs to the simulation include fabric parameters such as width/pitch, the given design and the overlay standard deviation. For every manufacturing step, an overlay misalignment value with respect to the previous marker is sampled. This is an input to the simulator with all possible defect scenarios; the simulator determines whether the chip is either defective or defect-free (for a chip without redundancy, these are the two outcomes of systematic effects). After all mask steps are completed, the chip is recorded to either pass or fail. After a specified number of Monte Carlo simulations are complete (in this case 5000), the overall yield is calculated.

This methodology provides a generic framework for analysis of systematic yield implications for nanofabrics. It

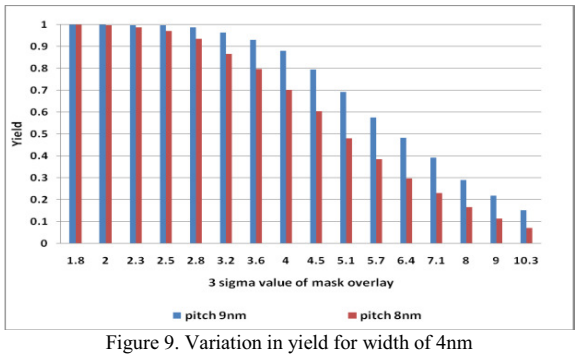

Figure 9. Variation in yield for width of 4nm

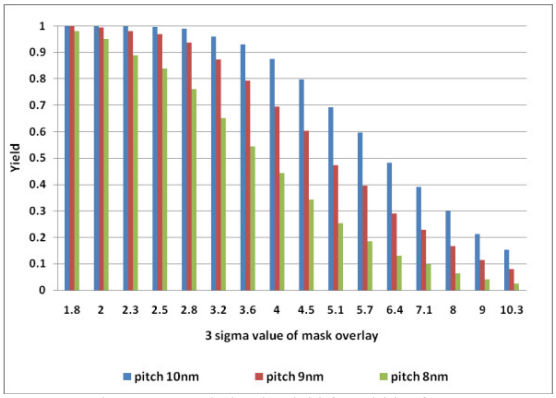

Figure 10. Variation in yield for width of 5nm

integrates physical fabric considerations (including geometric parameters such as pitch and width), manufacturing sequences and associated defect scenarios to estimate the yield. This is in contrast to prior approaches that used generic defect models that typically assume constant defect rates (or a range of constant defect rates) without considering the manufacturing pathway and the potential sources of defects. While the focus of this paper is the estimation of the mask overlay-limited yield for different fabric assumptions, this methodology can be easily extended to include 'processing-related' defects, like lateral diffusion during ion implantation leading to a shorted device, despite a correctly aligned mask.

This methodology enables addressing key overlay and registration requirements. For example, it is possible to estimate the overlay limited yield for a range of overlay projections. It is also possible to address sensitivity of the overlay-limited yield to key fabric parameters such as the width and pitch of nanowires. The next section describes our simulation results in more detail.

V. EXPERIMENTS AND RESULTS

Simulations were performed to check the impact of mask overlay and offset on the nano-manufacturing flow prescribed for NASIC fabric. The WISP-0 nanoscale processor design (mapped to the NASIC fabric), NASIC fabric assumptions, and overlay values were input to the simulator. The yield implications were studied for the various overlay values as shown in Fig. 8. Manufacturing solutions are known and are

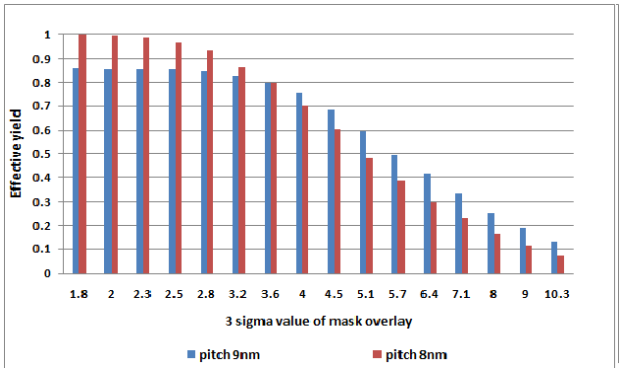

Figure 11. Variation in effective yield for width of 4nm

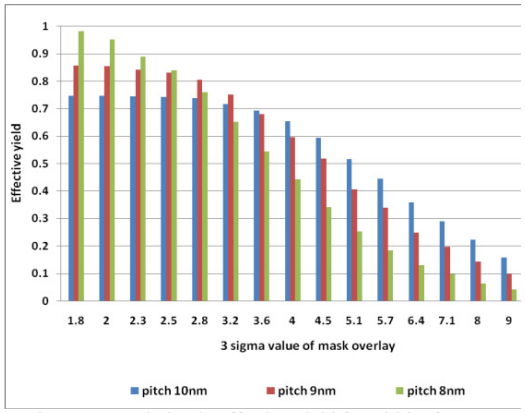

Figure 12. Variation in effective yield for width of 5nm

being optimized for the green (top) region; manufacturing solutions are known for the yellow (middle) region; and manufacturing solutions are as yet unknown for the red (bottom) region [17]. As mentioned in Section III, defect scenarios and consequently systematic yield loss are strongly dependent on the pitch and width parameters of the NASIC fabric.

A. *Sensitivity to pitch*

The impact of the nanowire pitch on the systematic yield loss due to mask overlay imprecison was evaluated. An xnwFET with a larger NW pitch is significantly easier to manufacture due to the increased minimum feature size on resist and also the increased spacing between adjacent nanowires. It is also expected to have better overlay imprecision tolerance. However, as expected, a larger NW pitch will result in a lower overall density, so it is important to understand its impact at the system level. WISP-0 consumes 0.839sq.um, 0.977sq.um, 1.125sq.um, 2.2394sq.um when mapped to 8nm, 9nm, 10nm and 16nm pitch NW, respectively. Fig. 9 shows the value of the systematic yield at various overlay values for a nanowire width of 4nm and varying pitch. At an overlay of 5.7nm, 57.48% yield was observed at 9nm pitch and 38.46% yield was observed for 8nm pitch. At a cost of 16.5% area increase, the yield can be increased by 45%. Fig. 10 shows the results for 5nm width nanowires. This

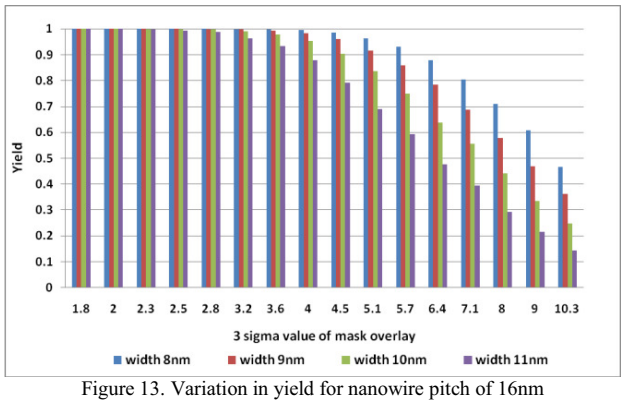

Figure 13. Variation in yield for nanowire pitch of 16nm

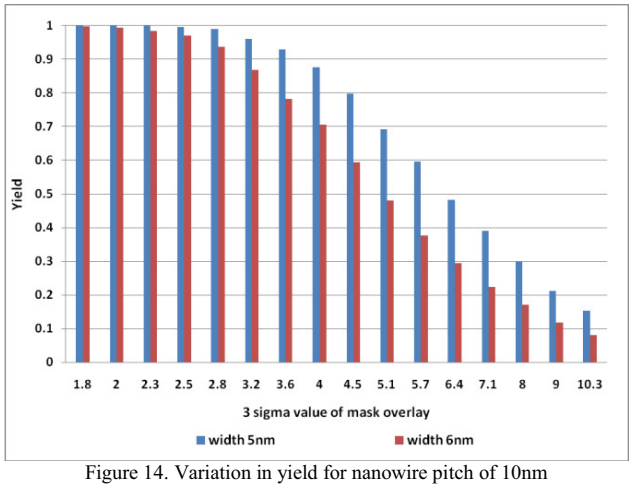

Figure 14. Variation in yield for nanowire pitch of 10nm

implies different design choices; for example, for a design with a larger pitch it may be feasible to give up some yield for better devices.

We use the metric "Effective Yield" which takes into account the tradeoff between yield and area overhead and represents the number of functional chips obtained from a given area. Effective yield is defined as (Overall Yield)*(Area of design with smaller pitch/Area of design with increased pitch). Fig. 11 shows the effective yield for 4nm width nanowires and varying pitch. It can be seen that up to overlay imprecision of 3.2nm, a design with an 8nm pitch gives a higher effective yield. For overlay imprecisions greater than 3.2nm, a 9nm pitch design has a better yield. This result suggests to start manufacturing at a relatively lower density and gradually scale down the pitch with improvements in manufacturing alignment. An effective yield plot for 5nm nanowire width (Fig. 12) for varying overlay values shows a similar trend for pitch 8, 9 and 10nm. While at high overlay imprecision, a low density fabric offers a better effective yield, with improvement in alignment precision a more denser fabric can be obtained. It can be seen that the crossover point from the region favoring 9nm pitch to the region favoring 8nm pitch requires a greater overlay precision at increased width (the crossover occurs at 3.6nm overlay imprecision for 4nm width when compared to 2.5nm imprecision for 5nm width).

B. *Sensitivity to width*

The sensitivity of overlay-limited yield to nanowire width was also evaluated. For a given pitch, the area of a NASIC design is constant irrespective of the width. Evaluation was carried out for varying mask overlay for a WISP design mapped to 16nm pitch and four different nanowire widths as shown in Fig. 13. At a constant pitch, an increase in the width of the nanowires would imply an increased channel cross-section for devices and hence a greater Ion current for devices, leading to performance improvements. On the other hand, yield loss due to overlay imprecision increases due to decreasing spacing between the adjacent wires. For example, in Fig. 6, the margin for functionalization mask misalignment was shown to be (p-w)/2, which implies that the misalignment margin is

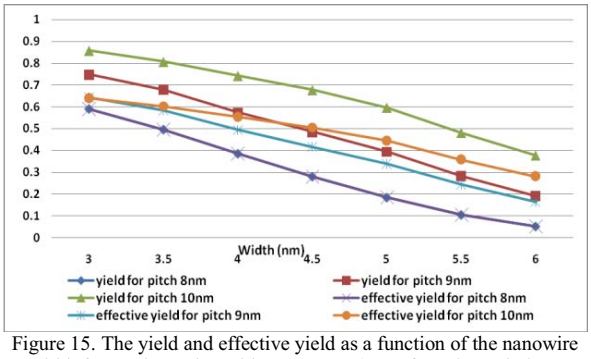

Figure 15. The yield and effective yield as a function of the nanowire width for mask overlay with 3σ=5.7nm (manufacturing solutions known)

reduced with increasing widths, leading to yield loss. Similar trends were observed for other process steps.

For a 16nm pitch nanowire, at 5.7nm mask overlay (manufacturing solutions known), a 93% yield was estimated at 8nm width with no fault tolerance incorporated. A yield of 85.96% was estimated for a 9nm width, and an yield of 75% and 59.36% was projected for a 10nm and 11nm width, respectively. The trends for a pitch of 10nm are shown in Fig. 14. As expected, for the same 3-sigma overlay imprecision, the yield is lower since less misalignment tolerance is available. Furthermore, a similar percentage increase in the width leads to a much higher decrease in yield for the 10nm design. For example, at 5.7nm overlay, a 20% (25%) increase in width leads to 36% (20%) decrease in yield for 10nm (16nm) pitch. Fig. 15 shows yield variation for seven different values of width for pitch of 8nm, 9nm and 10nm at 3σ=5.7nm (manufacturing solutions known). It can be seen that in the currently available manufacturing solutions, a larger pitch would provide a better yield margins. Fig. 16 is a similar plot for 3σ=5.1nm (manufacturing solutions unknown). The following observations were made during the evaluation: a) the impact of the nanowire width on the yield increases with increasing overlay imprecision, b) the *rate of decrease in yield* with increasing width, is faster at lower pitches as expected, c) the 'sensitivity of yield to width' analysis aids in achieving an

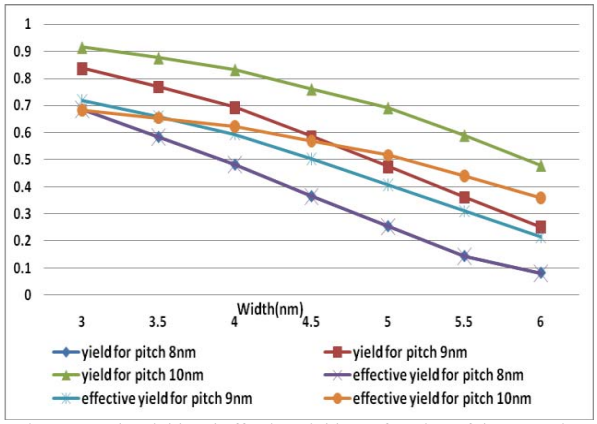

Figure 16. The yield and effective yield as a function of the nanowire width for mask overlay with 3σ=5.1nm (manufacturing solutions unknown)

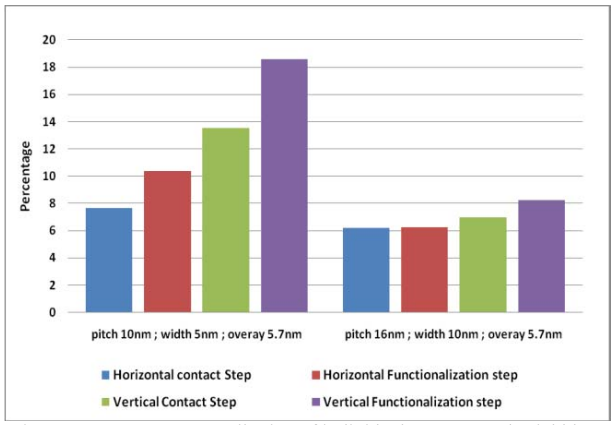

Figure 17. Percentage contribution of individual steps towards yield loss

efficient yield-performance tradeoff during the design phase.

C. *Contribution of each step*

An analysis of the contribution of each manufacturing step towards the yield loss was also carried out. This can be used to bring about improvements in manufacutring flow. The results in Fig. 17 show that the vertical functionalization step (Fig. 2H) is the most sensitive to mask overlay effects. Additional alignment markers may be used to allievate overlay imprecision for this step. It can also be observed that the horizontal contact creation step (Fig. 2B) is the least contributor towards yield loss, implying that nanofabrication techniques (based on contact patterning or self-assembly based approaches) tend to favor the formation of regular periodic structures such as grids as the bottom most layer. Registration requirements in such regular structures are alleviated since an initial lithography mask may be 'offset' with no loss of functionality. In CMOL [14] and HP's FPNI [29], nanofabric unconventional techniques such as nanoimprint are necessary after the fabrication of CMOS layers. This results in overlay alignment for imprint lithography with 3σ=±105nm [30], which implies significant challenges in alignment against previously formed features. Such a large overlay misalignment can contribute to significant yield losses (or conversely trade-off much of the density benefit for acceptable yield) and is not ideal. Furthermore, if an unconventional manufacturing step is performed before any lithographic masking, it is not affected by any overlay requirement. Thus, the result motivates us to utilize the uniform nanowire grid as the bottom most layer in the manufacturing pathway.

VI. CONCLUSION

To understand and deal with the challenges associated with a bottom-up fabrication of nanoelectronic circuits, identification of defects introduced during each step of the manufacturing pathway is essential. A study of the yield implications of the manufacturing sequence proposed for NASIC [8][9][12] , has been presented. The proposed methodology provides a framework for analyzing systematic yield loss. The sensitivity of the projected yield to physical fabric parameters has been

presented. At constant width, an increase in pitch increases the tolerance to mask overlay imprecision and hence achieves higher yield. At an overlay of 5.7nm, a 57.48% yield was projected for a 9nm pitch while a 38.46% yield was estimated for a 8nm pitch. An area increase of 16.5% was observed to bring about an almost 45% gain in yield. At constant pitch, the increase in width resulted in a lower yield due to the reduced overlay tolerances. The yield analysis can hence be used to identify effective design choices in fabric manufacturing. The pitch and width of the nanowire can be chosen in accordance with the lithographic alignment precision available to achieve an intended chip yield. Analysis of the yield loss due to individual steps emphasizes that the unconventional manufacturing step can be performed before any lithographic masking, so that it is not affected by any overlay requirement.

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