# Trade-Offs between Yield and Reliability Enhancement *

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**Abstract**

*Deep sub-micron VLSI technologies have led to a large increase in the number of devices per die as well as the switching speeds. These advances have been accompanied by increased design complexity and decreasing reliability. Scaling of the device dimensions has introduced "analog" effects on-chip that are causing signal integrity and delay problems. These problems are not easy to estimate and reduce after the VLSI layout has been finalized for fabrication and hence new CAD techniques are being proposed to tackle this problem up-front. Similarly, vastly increased manufacturing complexities have made manufacturing costs soar, and therefore chip yields need to be increased to cut losses due to manufacturing flaws. Extensive research has been done to suggest CAD solutions for reliability and yield enhancement, but these have treated the two as disjoint issues, and raised the thought-provoking question [1] about their relationship. In this paper, we attempt to answer this question using crosstalk minimization and yield enhancement techniques, as applied to the VLSI layout as a case study. We study the trade-offs between yield and reliability enhancement by using a weighted average of both objectives as the cost function.*

## 1: Introduction

While emphasis is still needed on VLSI CAD techniques for tackling conventional problems of floor-planning, placement and routing, it is becoming evident that deep sub-micron technology has brought with it newer problems. These are - yield reduction because of increased manufacturing complexity, and reliability reduction because of dominant "analog" effects like cross-coupled delays, electron-migration, hot-carrier effect and noise. A number of sources of noise exist [2, 3]. Ringing noise results from unmatched terminations if the interconnect is acting as a transmission line or from resonance if the line is acting as a RLC line. Crosstalk noise results from neighboring lines inducing signals on each other. Simultaneous switching noise occurs on power and ground lines as a result of drivers switching simultaneously.

Similarly, the cost of building sub-micron fabs coupled with the increase in the complexity of the mask process have meant that increased yields are required to offset the overheads incurred in manufacturing. The small feature sizes and the millions of devices on a chip rule out a solution to enhance yield by tuning the manufacturing process alone. The new approach has been to integrate the solutions into VLSI CAD tools so that the process is automated. Also, the integration should not violate earlier design constraints and must use an approach which ensures that there is no creation of new critical paths or drastic changes to the electrical characteristics. These methods are usually post-processing steps and have little overhead in terms of design turn-around-time, since they are applied to the

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last iteration step of the design just before the layout is ready for fabrication.
The approaches suggested so far treat yield enhancement and reliability enhancement as disjoint issues. Although the objective functions are different, there is a strong similarity between the methods used to achieve these objectives. This prompts the question about the inter-relationship between yield and reliability. It is important to address this question as it would be a waste of effort to develop techniques for either one of these issues which would result in a degradation of the other. Therefore, we need to develop techniques that take both yield and reliability into account and prevent a conflict of interest. The focus of this paper will be to analyze the effects of considering both issues simultaneously.

## 2: Yield enhancement techniques

Initial work on yield focused on developing yield models and estimation techniques [4, 5, 6]. The yield estimation tools were useful in providing the designer with information about the sensitivity of the design to defects and manufacturing flaws [7]. The application of this information to the development of yield enhancement techniques is very important since this means that modifications for yield enhancement done based on the knowledge of the defect sensitive regions of the design help increase yields by bigger margins. In addition, the overheads are minimal with respect to design turn-around-time, and hence cost effective to be included as a part of the design flow. Yield enhancement using layout synthesis techniques has been suggested in [8, 9, 10]. The underlying idea is that defect sensitivities of the design to random point defects can at times be reduced by modifications of the physical/symbolic layout without additional area overheads. The defect sensitivities minimization is effected as a measure of the critical areas that have been reduced by spacing out interacting nets. More recent techniques suggest that the critical nets of the design should not be disturbed and the layout modifications for yield will be done on the non-critical elements i.e., elements not on the critical path [10]. This is to ensure that the critical path is not affected by the yield modifications and the timings are consistent with what the designer intended.

## 3: Reliability enhancement techniques

The issue of designing reliable circuits and systems has attracted more attention [2, 3] in the past few years because of aggressive scaling of device sizes and increased clock-speeds of the VLSI chips. These factors, while leading to the performance leaps of present day VLSI chips, have also led to problems that have manifested themselves in a more severe way which can at times cause permanent chip damage. For example, the problem of impedance mismatch at the output pin may lead to a ground bounce of sufficient magnitude to cause a transistor on the path to latch-up and hence possibly destroy the chip through a short-circuit. Some extraneous signal effects can cause the chip to malfunction. For example, if two long wires run in parallel have a strong crosstalk interference, it is possible for a signal bit to get inverted and cause a logic malfunction. If one of the lines carried the clock, then the entire functionality of the system can become unpredictable if a stray pulse is introduced into the clock. Therefore, techniques that can tackle these problems as a part of the design flow are being developed [11]. These include physical/symbolic layout modifications and also efforts to reduce the effects through additional special structures like shields, matching and symmetric routing strategies [12]. The use of special structures requires considerable analysis and careful design as it might vary some other parts of the



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design and introduce the need to iterate some design flow steps to correct the discrepancy. This can lead to increased design turn-around-times. Crosstalk minimization is usually performed by spacing out nets that have a large cross-coupling capacitance. Also, if the net is on the critical path, then the changes are applied to the adjacent nets with a view to achieve a reliable design with minimal re-work of the layout.

## 4: Need for Trade-Offs

The reliability enhancement techniques proposed so far, and crosstalk minimizing channel-routers in particular, have failed to study the effect of their solution on yields. They are localized to nets with most severe cross-coupling and therefore might offer a solution in which the number of interacting nets increases leading to increase in critical areas. Similarly, yield enhancement techniques, while focusing on solutions that do not increase overall area, have not addressed the impact on crosstalk and other delays introduced as a result of the modifications. This has been partly due to the fact that both objective functions can be minimized by decreasing the "region of interaction" between adjacent nets. When a net on the critical path is used as a reference point for moving non-critical elements away, it is possible that a non-critical net becomes critical by virtue of the cross-coupling capacitance introduced. So it is not always true that a yield enhancement step leads to optimal reliability enhancement. Hence, there is a need to trade-off the two objective functions using a weighted cost function so as to arrive at a result that does not disregard either of them.

## 5: Analysis of Trade-offs

The chip yield is affected by various defect mechanisms and the defect size distribution. The defect mechanisms include open-circuit and short-circuit causing defects. The defect-size density function used is proportional to $1/x^3$, where $x$ is the defect-size [13]. Let $A_{sh}(z)$ and $A_{op}(z)$ represent the average critical area of short-circuit and open-circuit faults respectively, $D_{sh}$ and $D_{op}$ be the defect density of the short-circuit and open-circuit faults respectively, $z$ the width of the element and $\lambda_z$ represent the number of defects which can affect the functionality of the element. Therefore, the optimal location for the element [10] for decreased defect sensitivity, is calculated by minimizing the function

$$\lambda_z = A_{sh}(z) \cdot D_{sh} + A_{op}(z) \cdot D_{op} \quad (1)$$

We will consider only short-circuit causing defects for our case study. Therefore, the optimal location for decreased defect sensitivity can be calculated by minimizing

$$\lambda_z = A_{sh}(z) \cdot D_{sh} \quad (2)$$

The objective function for yield enhancement for the 2-layer channel routing case is defined as

$$Minimize\ Y\_Cost = \{ \lambda_{layer1} + \lambda_{layer2} \} \quad (3)$$

where $Y\_Cost$ is the Yield Cost and $\lambda_{layer1}$ and $\lambda_{layer2}$ represent the number of defects that can affect the functionality of $layer1$ and $layer2$ respectively. The reduction in critical area is used as a measure of the enhanced yield, since the other parameters that contribute to yield remain unchanged in this case. Since the track permutations are not allowed, $layer2$ critical areas do not change.



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Given a wire, the total capacitance is represented as a sum of three terms $C_p + C_f + C_{coup}$, where $C_p$ is the parallel plates capacitance, $C_f$ is the fringe capacitance and $C_{coup}$ is the line-to-line or coupling capacitance [2]. The reliability issue being considered is crosstalk minimization. This depends on the wire dimensions as well as spacings between adjacent interconnect lines. Hence $C_{coup}$ is the dominant factor. The cross-coupling capacitance per unit length is given by [14]

$$C_{coup} = \epsilon_{ox} \{ 1.93 (\frac{T}{H})^{1.1} + 1.14 (\frac{W}{H})^{0.31} \} (\frac{S}{H} + 0.51)^{-1.45} \quad (4)$$

where $\epsilon_{ox}$ is the dielectric constant of the oxide, $T$ is the thickness of the interconnect wire, $H$ is the thickness of the oxide, $W$ is the width of the wire and $S$ is the spacing between the two conducting wires. This model disregards the reliability issues caused due to partial shorts/opens since these are more difficult to model accurately. The crosstalk effect for a given net is computed [15] by considering the extent of overlap with nets that are adjacent to it. This overlap length determines the magnitude of crosstalk that is introduced into the other wire. The objective function to be minimized for reliability enhancement is defined as

$$Minimize \ \ R\_Cost = Maximum \{ C_{coup} \cdot L_{ol} \} \quad (5)$$

where $R\_Cost$ is the Reliability Cost for all nets, $C_{coup}$ is the cross-coupling capacitance per unit length and $L_{ol}$ is the overlap length of the wires.

Since cross-coupling capacitance plays a major part in the crosstalk effect, the objective in reliability enhancement is to minimize the maximum cross-coupling between the adjacent wires being considered. For crosstalk minimization, only the horizontal wires are considered since they are longer and hence more susceptible to the cross-coupling delays.

Therefore, a weighted cost function could serve as an objective function for achieving minimal total cost.

$$Total\_Cost = W_y \cdot Y\_Cost + (1 - W_y) \cdot R\_Cost \quad (6)$$

where $Total\_Cost$ is the cost required to take into account both the objective functions simultaneously, $W_y$ represents the weight for yield enhancement ($0 \leq W_y \leq 1$) and $(1 - W_y)$ represents the weight for reliability enhancement. Minimal total cost would by achieved by obtaining minimal critical area and also a reduction in cross-coupling capacitance.

In this paper, we present an algorithm which estimates the effect of the physical/symbolic layout modification on the yield enhancement and reliability enhancement objective functions and generates a solution which provides the best trade-off between yield and reliability based on the user inputs. The method ensures that no new critical paths are formed. The weighted cost function is applied only to non-critical nets which do not create or become critical nets when either yield or reliability enhancement is applied.

The proposed method assumes a best routing solution and a compact channel. It uses the inter-net space to move the nets to enhance yield by minimizing critical areas and also reduces the cross coupling between nets without violating the design rules specified. Track permutations are not permitted and varying the thickness of the net will be provided for in the next version of this CAD tool. We also assume that the user inputs include the critical path information in the form of slack information of each net. The slack on a net is defined as the difference between the critical net delay and the current net delay. Therefore, it follows that a critical net is a net having zero slack. To move the nets without violating design rules, the algorithm uses spacing rules, available to the algorithm in the form of a table. Also, a module that extracts the delay value given net dimensions is made available to the tool to obtain slack values.



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## 6: Algorithm

This algorithm is applied as a post-processing step to a 2-layer channel router to study the trade-offs in yield and reliability enhancement. The inputs to the algorithm include a routed 2-layer channel, information on the slacks of all the nets, defect-size distribution and weights for the yield and reliability enhancement objective functions and the design rules.

```
Begin
 Initialization:
      Create_constraint_graph (adjacency_info, spacing_slack_info);
 Main module:
  Iterate (till Total_Cost is minimized) {
     for each (net having spacing_slack and not on the critical path) {
         Calc_Crosstalk (Net,Slack_Info,Info_about_parasitics);
         Calc_Crit_Areas (Net, Defect_size_Distr, Fault_probs);
         if ((Net_Slack - Crosstalk_Delay) <= 0)  // new critical path
             Compute new net location which minimizes crosstalk;
             Update slack value on the net; // slack > 0
         else
         {
            Compute new Net location which enhances yield;
            Compute new Net location which minimizes crosstalk;
            Diff = Difference (as distance) in the computed net locations;
            Iterate (over Diff ensuring no new critical paths are formed)
            {
                Calc_Crit_Areas (Net, Defect_size_Distr, Fault_probs);
                Calc_Crosstalk (Net, Slack_Info, Info_about_parasitics);
            }
            end Iteration (when Cost is minimum);
            Update the slack value on the net;
         }
      Update the location of the net;
     }
  }
End;
```

Complexity Analysis : Let $n$ be the number of nets in the channel, and $\lambda$ the minimum unit of measure. Assume that the constraint graph is already available (since this is only a post-processing step) and that the operations required to embed the constraints of slack information take constant time. Therefore, the Initialization step is a constant time step. Since the algorithm has to check each net, it requires $n$ steps to complete the execution. For each of these $n$ nets, the algorithm requires $O(n)$ steps to evaluate the nets adjacent to it for both critical area and crosstalk estimation. After this calculation, the algorithm requires $O(log_2((x \cdot \lambda) - G))$ steps to compute the optimal location for the net, where $(x \cdot \lambda)$ is the distance between the adjacent nets being considered and $G$ is the distance as specified by the design rules.

The time complexity can be therefore specified as

$$Time\ \ taken = n. \cdot (O(n) \cdot O(log_2((x \cdot \lambda) - G))) + Const. \tag{7}$$



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## 7: Conclusion and Future Work

The above algorithm was incorporated into GLITTER [16], the gridless variable-width channel router, and was run on a few examples to validate the importance of the trade-offs required. These are shown in Fig. 1 and Fig. 2. In Fig. 1.a, the original channel router solution is shown with arbitrary slacks assigned to nets, and Net 2 is assumed to be critical. This net suffers additional delays on account of the crosstalk problem and therefore the algorithm moves nets to eliminate the additional delays due to cross-coupling. In practice the slack values will be fed from the timing analysis tool. The critical area is 36 sq. units and the total slack on the nets is 17 units. On minimizing crosstalk (Fig. 1.b), the critical area decreases to 32 sq. units and the total slack on the nets increases to 24 units. When yield enhancement is applied (Fig. 1.c), the critical area reduces to 26 sq. units and total slack is 26 units. But we find that net 8 becomes a critical net since the cross-coupling delays increase. This is undesirable since the succeeding stages of the design will be affected. Fig. 1.d shows the trade-off and ensures that no new critical paths are formed by moving non-critical elements. The critical area in this case increases to 28 sq. units and the total slack increases to 27 units. Fig. 2 illustrates another example where the existing techniques will be unable to come up with a good solution as there is very little spacing slack. Varying wire widths suitably helps keep the delays within predicted values. This example also illustrates the need to move critical elements to obtain the optimal solutions as long as the delays associated with it are not increased.

Future work includes taking into consideration other reliability issues and extending the optimization problem. In addition, we intend to study how detailed routers can use this information and come up with a optimal solution without violating the primary constraints of performance and area. The present implementation does not allow jogs in wires and varying the wire widths. These will be included in the future version of this algorithm. The algorithm will also be extended to deal with both layers rather than using the simplification that the vertical wires are not major contributors to cross-talk effects.

## 8: Acknowledgments

The first author wishes to gratefully acknowledge the guidance of Dr. H. Chen in incorporating the above algorithm into GLITTER, the gridless variable width channel router. Discussions with Dr. Chandramouli Visweswariah helped to fine-tune the algorithm. Both are with IBM Research Division, T.J. Watson Research Center, Yorktown Heights, NY.

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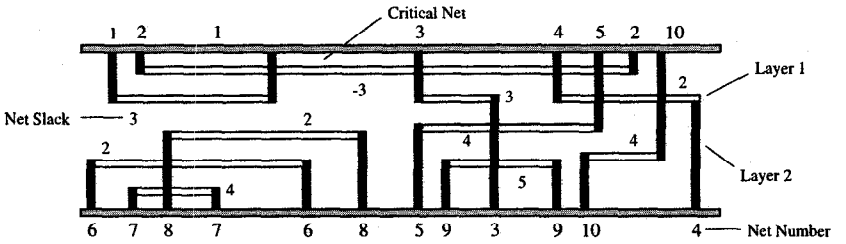


Fig. 1. a - Original Channel Router Solution (Slacks on nets are assigned arbitrarily)

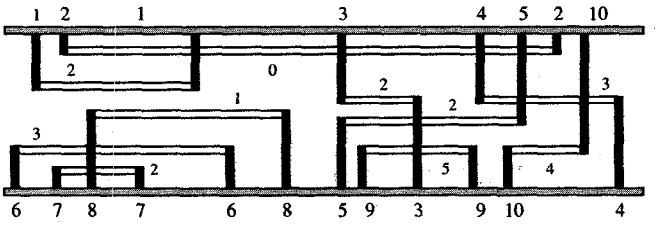

Fig. 1. b - Solution obtained after cross-talk minimization is applied

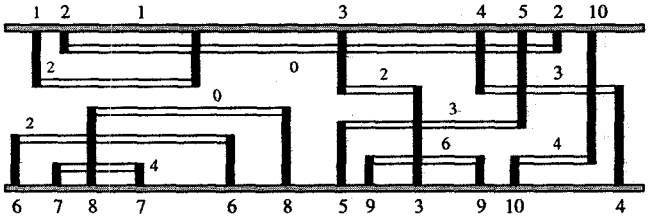

Fig. 1. c - Solution obtained after yield enhancement is applied

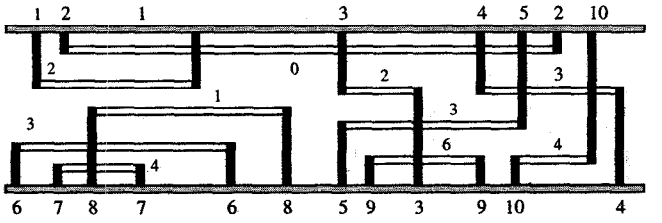

Fig. 1. d - Solution obtained by considering both yield and reliability simultaneously



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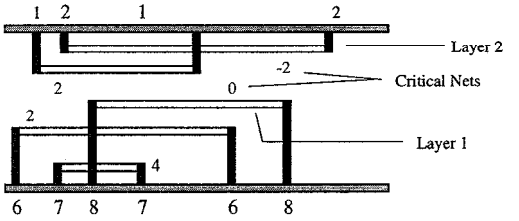


Fig. 2. a - Original Channel Router Solution (Slacks on nets are assigned arbitrarily)

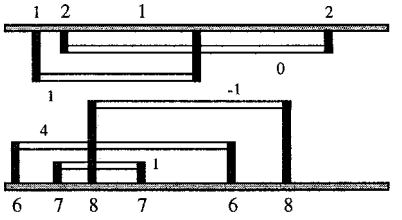


Fig. 2. b - Solution obtained after cross-talk minimization is applied

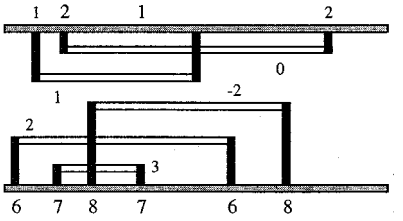


Fig. 2. c - Solution obtained after yield enhancement is applied

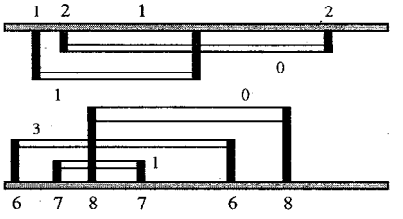


Fig. 2. d - Solution obtained by considering both yield and reliability simultaneously



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