Constructive floorplanning with a yield objective

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Abstract

The ability to improve the yield of integrated circuits through layout modification has been recognized, and several techniques for yield enhanced routing and compaction have been developed. Still, yield issues are rarely a factor in the choice of the floorplan mainly due to the tendency to focus on the more important timing and area objectives. Consequently, floorplanning tools have been developed with only these primary objectives in mind. We show in this paper that it is possible to generate a better floorplan with respect to yield, with very little penalty in the main objectives. We describe a constructive floorplanning approach which is based on analytical techniques and produces near optimal floorplans in terms of area utilization, wiring length and yield.

1. Introduction

Floorplanning is an essential design step when a hierarchical design methodology is used. Floorplanning is the placement of modules when the design of the modules has not yet been completed. As a result, the shape of the module (i.e., its aspect ratio) and the positions of the input and output pins have not yet been fixed. This flexibility presents the designer with the opportunity to choose among several implementations of the module in order to obtain a better floorplan. There are currently no universally accepted criteria for measuring the quality of a floorplan, but minimizing the chip area, wire length or delay are often used. Yield is normally not considered as an objective, although for today's ICs (with a total area of $2cm^2$ and up) it could become critical. Previous work [2] has shown a significant dependence of the yield on the floorplan for large chips, and the idea of a constructive floorplanning algorithm with a yield objective has been proposed. In this paper we extend these results and present a constructive floorplanning approach which combines heuristic and analytical schemes for generating yield enhanced floorplans. Section 2 describes the model and our new approach, and in Section 3 we present some of our numerical results. Section 4 concludes the paper.

2. The Floorplanning Algorithm

2.1. Model description

The floorplanning problem is that of placing in the chip area n rectangular modules with given area sizes $A_1, \ldots, A_n$. Although module i has a fixed area A_i, its height h_i and width w_i can be modified as long as $h_i \cdot w_i = A_i$. However, due to feasibility constraints, the aspect ratio of module i, h_i/w_i, must be limited to a range $r_i \leq \frac{h_i}{w_i} \leq s_i$ $(i = 1, \ldots, n)$.

The criteria for the quality of a floorplan dealt with in this paper are: a low chip area A (or equivalently, a high area utilization U), a low total wiring length L, and a high chip yield Y.

The chip area is measured by $A = H \cdot W$, where H and W are the height and the width of the chip, respectively. There is normally some flexibility in selecting H and W, as long as A covers all the modules and the chip aspect ratio is within a given range $p \leq \frac{H}{W} \leq q$. The area utilization U is defined by

$$U = \frac{\sum_{i=1}^{n} A_i}{A}$$

Since $\sum_{i=1}^{n} A_i$ is fixed, minimizing A is equivalent to maximizing U.

The wiring length is calculated using an interconnection matrix $C_{n \times n} = [c_{ij}]$, where c_{ij} indicates the number of wires connecting modules i and j $(i, j = 1, \ldots, n)$. The total wiring length for a given floorplan is defined as

$$L = \sum_{i<j} c_{ij} \cdot d_{ij} \qquad (1)$$

where d_{ij} is the Manhattan distance between the centers of modules i and j, which are denoted by (x_i, y_i) and (x_j, y_j),

respectively. Thus,

$$d_{ij} = |x_i - x_j| + |y_i - y_j| \quad (2)$$

Finally, for the purpose of estimating the yield of a given floorplan, a theoretical yield model is needed. We use the medium-size clustering negative binomial distribution presented in [4]. Under this yield model, which is suitable especially for large chips with clustered defects, the chip is divided into disjoint areas called "blocks", representing the areas on the chip in which the defect clusters are enclosed. The fit of the model to actual defect data has been demonstrated in [5]. To use this model, we need to know the fault density for each module i, denoted by λ_i and defined as the expected number of manufacturing defects per unit area which turn into actual faults. The exact fault density of a module depends upon its critical area (see for example, [3]) which in turn, depends upon its exact layout. At the floorplanning stage of the design process, the exact layout of the module is still unknown. A common practice is to estimate the fault densities based on transistor densities. These are usually known at this stage since reasonably good estimates of the area and number of transistors per module are available.

The purpose of floorplanning with yield as a secondary objective is to position all the modules in a bounding box with minimum total area A (or maximum area utilization U), minimum wiring length L, and as high as possible a yield Y. For given module areas $A_1, \ldots, A_n$, a feasible floorplan solution selects a $H \times W$ rectangle and places in it n non-overlapping rectangles, where rectangle i has dimensions $h_i \times w_i$ (with $h_i \cdot w_i = A_i$) and is centered around (x_i, y_i) ($i = 1, 2, \ldots, n$).

2.2. Yield enhancement

It is shown in [2] that for yield enhancement it is best to place modules with higher fault densities as close to the center of the chip as possible. To achieve this objective at the floorplanning stage, we assume that the chip is a square $S \times S$ ($S = \sqrt{\sum_{i=1}^{n} A_i}$) and divide the chip area into an $g \times g$ grid, so that the center of each grid cell is a possible location for the center of a module. g^2 is kept as close as possible to the number of modules, and to ensure symmetrical locations, g is restricted to odd numbers. For such a grid, the g^2 cells can be divided into $m = k(k+1)/2$ groups (where $k = (g+1)/2$), where the cells in the same group have an equal distance to the center of the chip. Each cell is then assigned a number from 1 to m. (See Figure 1 for the numbering of the cells in a 5×5 grid for which $g = 5$, $k = 3$ and $m = 6$.) A cell with a lower number is more suitable (from the point of view of yield) for a module with a lower fault density. Ideally, for yield maximization, the modules must now be ordered according to increasing fault densities: $\lambda_1 \leq \lambda_2 \leq \cdots \leq \lambda_n$, and placed in this order first in the cells numbered 1, then in the cells numbered 2, and so on. The module with the highest fault density (λ_n) should be placed in the center cell which is numbered m. Since our primary objective is not yield but wire length minimization, we use the placing scheme described above only as a tie breaker. We define for each cell a "yield fitness" value which is determined by the distance of the cell center (x, y) from the center of the chip $(S/2, S/2)$

$$F(x, y) = x(S - x) + y(S - y)$$

Cells with the same number have the same value of the fitness function, which results in m different fitness values $F_1, ..., F_m$.

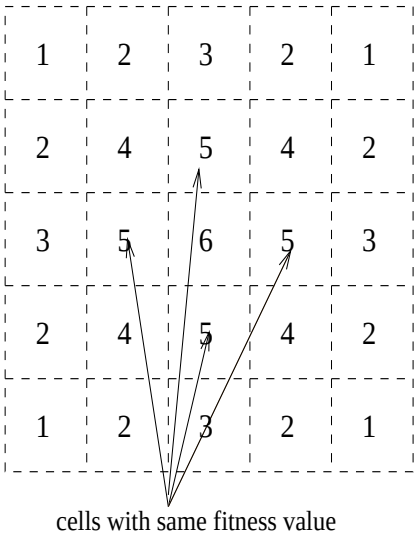
If, during the floorplanning process, a given module can be placed in several potential locations $(x^{(i)}, y^{(i)})$ which are equivalent with regard to wiring length, then we select the location for which $\mid F(x^{(i)}, y^{(i)}) - F_j \mid$ is minimized, where F_j is the fitness value of the ideal location for the given module.

2.3. Determining the relative locations of modules

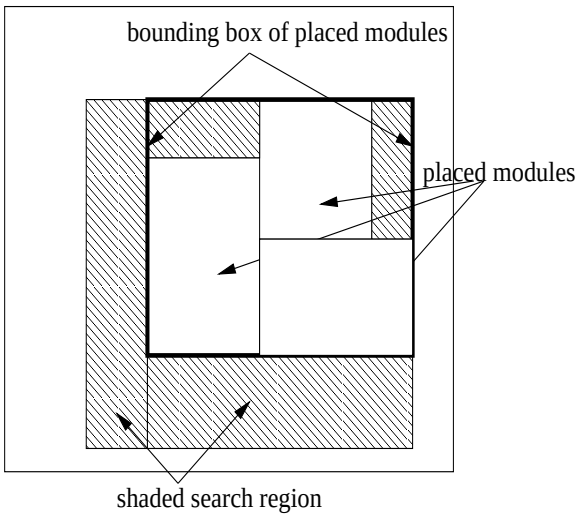
In constructive floorplanning, modules are selected and placed one at a time [1, 6]. The heuristic strategy which we follow here is to select a module which has the highest connectivity (i.e., number of wires) to the already placed modules and has the largest area. Once a module is selected, its location on the chip must be determined. Since the newly selected module is connected to the already placed ones, it will either be placed in the current bounding box containing all the placed modules or cause the bounding box to increase by no more than the width or height of the new block. All locations in this search space are evaluated so as to minimize the total wire length to already placed modules. If, however, multiple locations are available with similar wiring lengths, then the one which increases the yield is selected. The latter is the one with the minimum difference between the yield fitness of the candidate location and that assigned to the module by order of fault densities, as described in the previous sub-section. The first module to be selected according to this procedure is the one with the largest area, and it is placed in the location which is determined by its fault density. The "search space" for module locations is illustrated in Figure 1. Once an initial floorplan is obtained by the constructive algorithm, we modify the aspect ratios in order to achieve area minimization (and area utilization maximization). The next sub-section introduces the model used in this step.

2.4. Determining optimal shapes for modules

The floorplan construction step determines the relative positions of the modules. We then use a linear program-



5 X 5 Grid Cell has 6 unique fitness values.



Search space for locations of next module

Figure 1. Steps in the constructive floorplanning.

ming model to modify the shape of each module to achieve a better solution in terms of the chip area utilization.
The model variables are:
H, W - the height and width of the chip, h_i, w_i - the height and width of module i, x_i, y_i - the coordinates of the center of the location of module i ($i = 1, \ldots, n$).
Since the relative location of the modules is not changed in this step, we include in the model relative location constraints which are obtained from the horizontal adjacency graph (HAG) and the vertical adjacency graph (VAG) for the originally constructed floorplan. These graphs indicate which modules are placed to the right of other modules, or below other modules, respectively.
The linear programming model is:
select H, W, h_i, w_i, x_i and y_i ($i = 1, \cdots, n$)
so that the objective function

$$H + W \tag{3}$$

is minimized, subject to
Boundary constraints:

$$x_i \geq w_i/2 \quad (i = 1, \cdots, n) \tag{4}$$

$$x_i + w_i/2 \leq W \quad (i = 1, \cdots, n) \tag{5}$$

$$y_i \geq h_i/2 \quad (i = 1, \cdots, n) \tag{6}$$

$$y_i + h_i/2 \leq H \quad (i = 1, \cdots, n) \tag{7}$$

Non-overlapping constraints from HAG and VAG:

$$x_j \geq x_i + w_i/2 + w_j/2 \tag{8}$$

(j is to the right of i and non-overlapping)

$$y_j \geq y_i + h_i/2 + h_j/2 \tag{9}$$

(j is above i and non-overlapping)
Aspect ratio constraints:

$$h_i \cdot w_i = A_i \quad (i = 1, \cdots, n) \tag{10}$$

$$r_i \leq \frac{h_i}{w_i} \leq s_i \quad (i = 1, \cdots, n) \tag{11}$$

$$p \leq \frac{H}{W} \leq q \tag{12}$$

Non-negativity constraints:

$$\text{all variables} \geq 0 \tag{13}$$

If both w_i/h_i and h_i/w_i lie within the aspect ratio range then rotation is automatically performed. The objective for the linear programming model is to minimize the chip dimensions. We use the objective "minimize $H + W$" which results in an almost square floorplan. We can also have objectives like "minimize $2H + W$" or "minimize $H + 2W$", which will result in more rectangular floorplans.

Figure 2 shows an example of a floorplan before and after the area minimization step. We can see that for this example, not only did the area utilization increase, but the other two criteria improved as well.

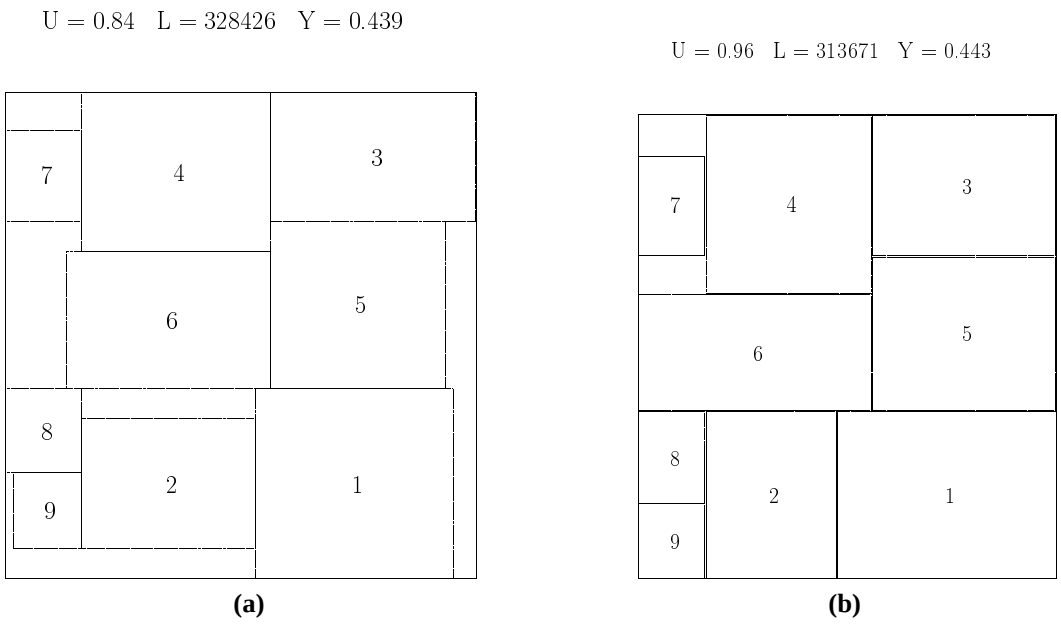


Figure 2. A floorplan (a) before and (b) after aspect ratio optimization.

3. Numerical Results

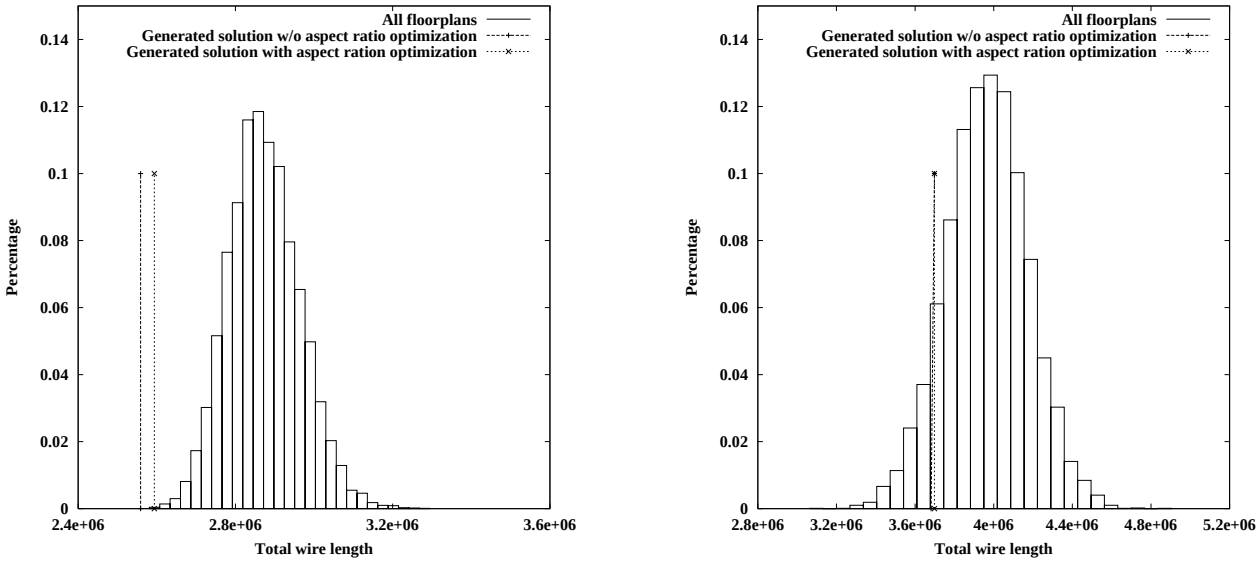
In order to measure the quality of the floorplans generated by our algorithm, we developed a random floorplan generator. In this random floorplan generator, a set of n modules with areas A_i is given. At each step, a module is selected at random from the list of yet unselected modules and its location is then determined randomly within the boundaries of the existing chip. If a suitable location cannot be found, the dimensions of the chip are increased. We performed multiple runs of random floorplan generation for a given set of modules, and recorded all the resulting non-isomorphic floorplans. Thus, for each floorplanning problem, we obtain the possible solution space and the probability distribution for quality measures like total wire length L, area utilization U and yield Y.

Clearly, the variation in the areas of the given modules has an impact on the quality of the floorplan. We therefore, experimented with two sample test cases: in case (a) we have modules of almost similar size and in case (b) we have few very big modules and the rest are small modules. The histograms illustrating the distributions of L, U and Y are shown below. Figure 3 illustrates the distribution of wire length for all non-isomorphic floorplans generated for case (b). As expected, it is similar to a normal distribution. The vertical line indicates the wiring length of the floorplan generated by our algorithm. Table 1 shows the percentile in which our solution is located compared to all floorplans, for the two cases of module size distribution. Our constructive floorplanning algorithm generates solutions with very good area utilization and wiring length. In case (a) the yield of the generated solution is also very good but in case (b) the greater emphasis on area utilization and wiring length did not allow a near optimal yield. In such a case further tradeoffs between yield and the other two objectives is possible.

	(a)	(b)
Module area range	1:2.37	1:7.80
Area utilization	5%	1%
Wire length	1%	8%
Yield	1%	35%
Run time	22 sec	30 sec

Table 1. Percentile of algorithm generated solution for the two types of floorplans.

Figures 4 and 5 illustrate the distribution of area utilization and yield, respectively, for all possible floorplans and for the best 20% floorplans with regard to wiring length. We observe in these two figures a shift towards higher area utilization and higher yield in the floorplans with low wiring length. We also see from the above figures that for these floorplans optimizing the shape of the modules has only a limited effect on the wiring length, but a bigger impact on area utilization and yield. Area utilization always improves with module shape optimization while the yield slightly reduces in the case of modules with a large variation in size.



(a) Modules with similar size

(b) Modules with varying size

Figure 3. Distribution of the total wire length of the floorplans.

4. Conclusions

A constructive heuristic approach combined with an analytical technique have been used in this paper to obtain floorplans with better yield. In this approach we do consider the yield while selecting the location at which a module is to be placed. We believe that incorporation of the yield into the selection criteria for modules to be placed will significantly increase the yield of the floorplan without paying a heavy penalty in terms of the primary objectives of floorplanning.

5. Acknowledgment

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6. References

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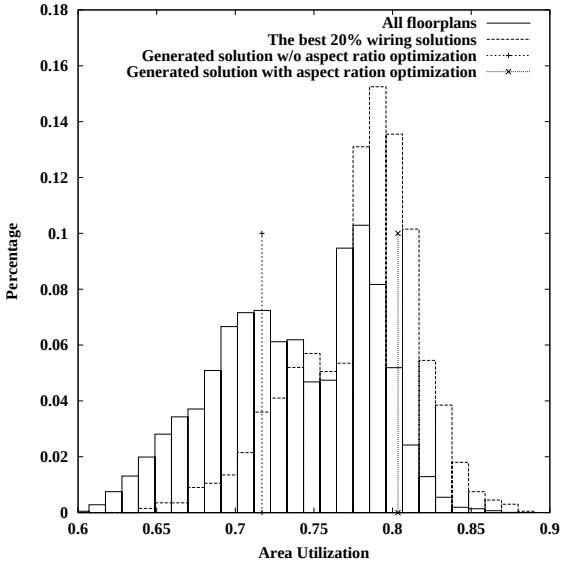
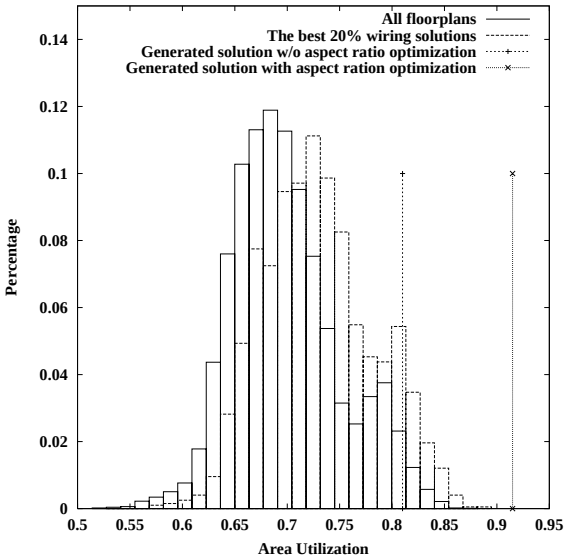
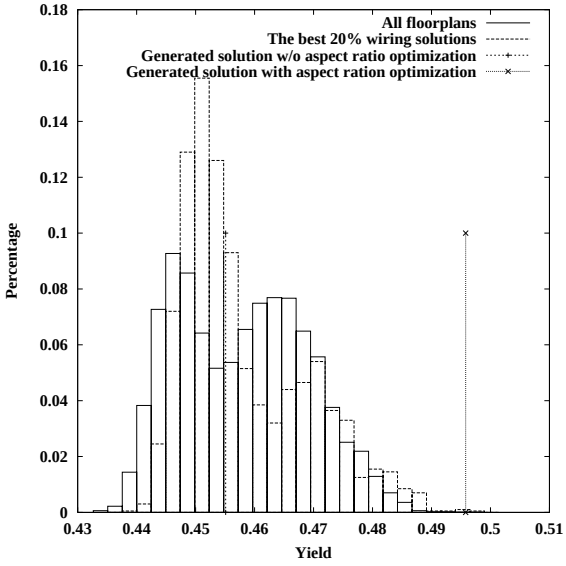


(a) Modules with similar size

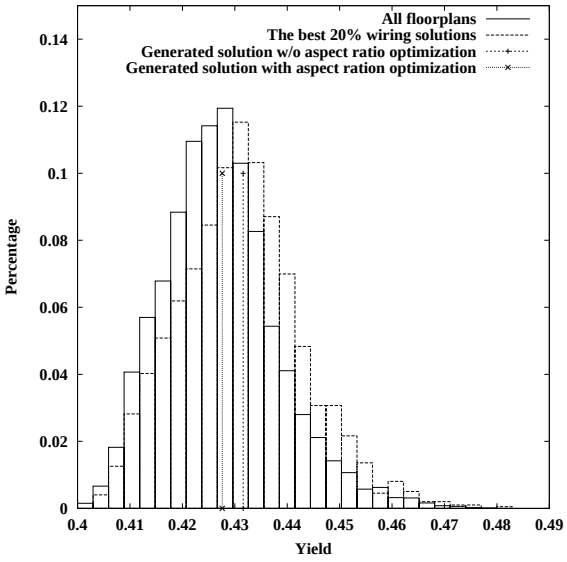


(b) Modules with varying size

Figure 4. Distribution of the area utilization of the floorplans.



(a) Modules with similar size



(b) Modules with varying size

Figure 5. Distribution of the yield of the floorplans.