

Nanoscale Application Specific Integrated Circuits

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Abstract—This fabric update summarizes recent advances for the Nanoscale Application Specific Integrated Circuits (NASICs) nanoscale computing fabric. We provide a brief overview of NASICs, and discuss recent work at all fabric levels. We present advances in device design and optimization including omega gated and junctionless nanowire field effect transistors, methodologies for validation of functionality and parameter variation evaluation, new circuit-level sequencing schemes and performance optimization techniques. We also discuss techniques for defect and parameter variation resilience, ongoing fabrication directions including prototyping and scalable assembly efforts, and directions for the future.

I. INTRODUCTION

Nanoscale Application Specific Integrated Circuits (NASICs) [1], [2], [3] is a semiconductor nanowire grid-based computing fabric targeted as a CMOS replacement technology. NASICs rely on 2-D grids of semiconductor nanowires with computational streaming supported from CMOS. A fabric-centric mindset or integrated approach across devices, circuit style, manufacturing techniques and architectures is followed, with design choices and optimizations at individual levels made compatible with the fabric as a whole. This mindset is anchored in a belief that at nanoscale the underlying fabric, rather than the device alone, is how significant progress could be made in system-level capabilities. This is in direct contrast to ‘device-first’ approaches that focus on MOSFET-replacement devices essentially preserving the CMOS circuit styles and manufacturing paradigms for interconnect intact.

In NASICs, many design choices are geared towards simplifying manufacturing requirements and realizing the fabric as a whole. These are summarized below:

- NASIC designs use regular semiconductor nanowire crossbars without any requirement for arbitrary sizing, placement or doping [1]. Regular nanostructures with limited customization are more easily realizable with unconventional nanofabrication approaches.
- NASIC circuits require only one type of device in logic portions of the design [3]. This eliminates the need for balancing switching characteristics across dissimilar devices through additional customization (e.g. switching delay, threshold and operating voltages of p- and n-type FETs).

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- Local interconnection between individual devices as well as between adjacent crossbars is achieved entirely on nanowires; in other words, device are achieved at the same time as the interconnect to form an ultra-dense fabric and interconnection of devices does not introduce new manufacturing requirements.
- NASICs use dynamic circuit styles with implicit latching on nanowires. Implicit latching reduces the need for complex or area expensive latch/flip-flop components that require local feedback.
- Tuning active devices to meet circuit requirements is done in a fabric-friendly fashion; techniques to tune threshold voltage and on-off current ratios of crossed-nanowire field effect transistors does not impose new manufacturing constraints.
- NASICs use built-in fault tolerance techniques to protect against manufacturing defects and timing faults caused by process variation. Built-in fault tolerance techniques do not need reconfigurable devices, extraction of defect maps, or complex micro-nano interfacing as required by reconfiguration based fabrics. All fault tolerance is added at nanoscale and made part of the design without additional interfacing requirements.

A brief overview of the NASIC fabric follows. Subsequent sections describe updates at each fabric level.

II. NASICs OVERVIEW

Semiconductor nanowires (NWs) have been demonstrated with a variety of materials including silicon [4], germanium [5], InSb [6] etc. By using non-conventional assembly techniques [7], [8], it may be possible to assemble these materials into regular arrays and grids.

The NASIC fabric is built on these types of 2-D semiconductor nanowire grids with crossed nanowire field-effect transistors (xnwFETs) at certain crosspoints. The channel of a xnwFET is aligned along one NW while the perpendicular NW above it acts as gate. A typical xnwFET behavior has been reported in Silicon NWs in [9].

Fig. 1 shows a 1-bit full adder implemented on the NASIC fabric. This includes a semiconductor nanowire grid with peripheral microwires (MW) that carry V_{DD} , V_{SS} and dynamic control signals. xnwFETs are shown at certain crosspoints in the diagram. Channels of xnwFETs (blue regions) are oriented horizontally on the left plane, and vertically on the right. Inputs are received from vertical nanowires in the left plane. These act as gates to horizontal nanowire FETs implementing one stage of a dynamic circuit. The output of horizontal nanowires acts as gate to the next set

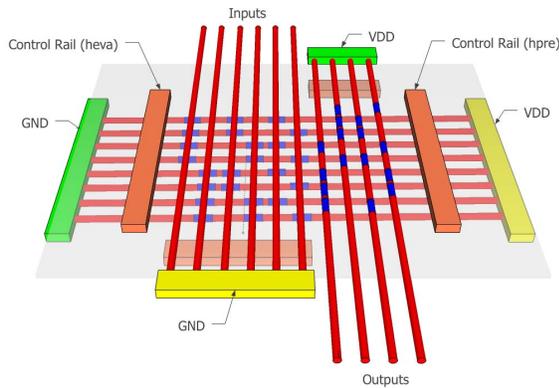


Fig. 1. 1-bit NASIC adder

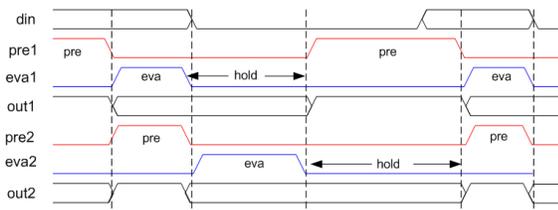


Fig. 2. 3-phase timing scheme for NASICs

of transistors whose channels are aligned in the vertical direction (right NAND plane). Multiple such NASIC tiles are cascaded together to form more complex circuitry such as microprocessors [10] and image processing systems [11].

All crossed nanowire devices used in the logic portions of the circuit are identical with no arbitrary doping or sizing requirement. Customization of the grid is limited to defining the positions of transistors. Furthermore, NASICs use a single doping type in all xnwFETs to reduce manufacturing requirements and improve performance [3].

NASICs use a dynamic circuit style with control signals driven from external reliable CMOS circuitry. Control signals coordinate the flow of data through NASIC tiles: horizontal and vertical signals are different, supporting cascading. Fig. 2 shows a typical NASIC control scheme but other schemes are also possible. Horizontal nanowire outputs are initially precharged to logic ‘1’ by asserting *pre1*. *pre1* is then switched off and *eva1* is asserted to evaluate inputs. Vertical nanowires are simultaneously precharged (*pre2* is asserted). In the next phase, both *pre1* and *eva1* are switched off, and the horizontal nanowires are in ‘hold’ phase, during which time *eva2* is asserted and outputs from the tile are evaluated. The hold phase implements implicit latching of the nanowire output after evaluation without the need for expensive flip-flops, and is essential for cascading multiple nanowire stages. Subsequent stages are evaluated using similar cascaded clocking schemes (*pre3* and *eva3*).

III. METHODOLOGY FOR DEVICE-FABRIC EXPLORATIONS

In a fabric-centric mindset it is necessary to evaluate material choices, device properties and circuit behavior in a tightly integrated fashion. For example, key questions may include: What are device I-V and C-V characteristics? How are they affected by choice of material, structure, doping and other

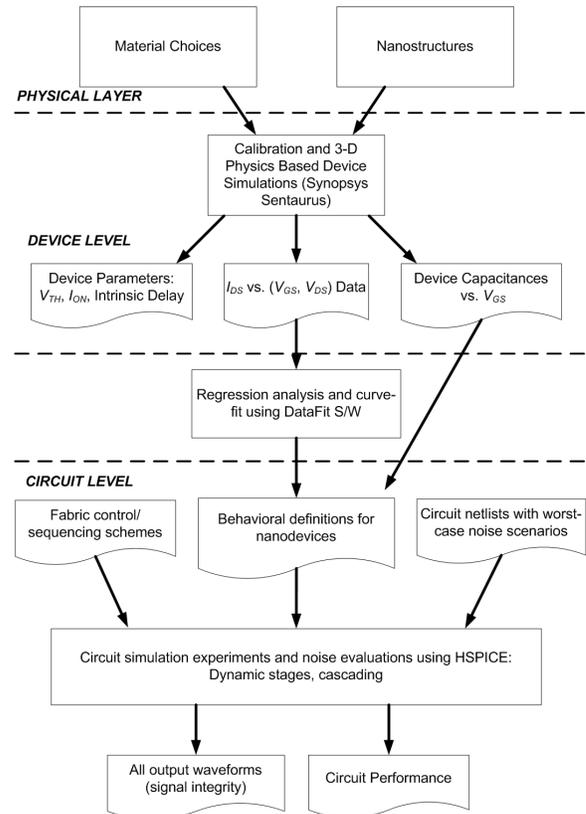


Fig. 3. Methodology for Integrated Device-Fabric Exploration and Noise Evaluation

manufacturing parameters? What are the noise implications for an integrated system with interacting devices, can circuits be made functional? etc. However, in general, conventional circuit simulators such as HSPICE [12] do not have built-in analytical models for emerging devices. Therefore, a bottom-up framework for evaluating nanodevices and fabrics across multiple design levels is needed.

In this section we discuss an integrated device-fabric methodology incorporating physical layer choices, accurate 3-D physics based simulation and characterization of device nanostructures and detailed circuit-level simulations for evaluating implications for a nanofabric. While the methodology has been evaluated extensively for the NASIC fabric, the approach itself is generic and applicable to other fabrics. For example, recent work with N³ASICs [13] and graphene-based memories has used this framework [14].

The methodology for noise exploration is summarized in the flow diagram shown in Fig. 3. A variety of physical layer assumptions such as choice of gate material and the structure of devices can be made targeting device metrics such as the threshold voltage, on-currents and intrinsic delay. For example, the gate material used in xnwFETs could be composed of crystalline silicon, nickel silicide or metals. Similarly, the structure of the device may be a top nanowire gate or an Omega gated structure for tighter electrostatics. In accordance with the fabric centric mindset, these assumptions need to be evaluated in terms of implications for manufacturing as well as for other design levels.

The electrical properties of individual xnwFETs may be

characterized using accurate 3-D physics based simulation of the nanostructures using Synopsys[®] SentaurusTM [15]. Calibration of the tool against experimental data at similar dimensions is required to account for nanoscale effects such as increased surface roughness and interface trap states. These device-level simulations provide 3 sets of data: i) Current data for different values of drain-source (V_{DS}) and gate-source (V_{GS}) voltages, ii) Device capacitances at different values of V_{GS} , and iii) key device parameters/metrics that determine noise margins and performance of the devices such as the on-currents (I_{ON}), threshold voltage (V_{TH}) and the intrinsic delays of the devices. These device parameters may be adjusted by changing underlying physical layer assumptions as well as the substrate bias (e.g. a higher threshold voltage may be obtained by modifying the metal work function or using a more negative back gate bias).

The current data is fitted as a function of V_{GS} and V_{DS} using regression analysis and curve fitting. This step expresses the current as a mathematical function of V_{GS} and V_{DS} . The expression for the current, in conjunction with a piecewise linear approximation for the device capacitances forms a behavioral model of the xnwFET, which may be incorporated into a standard circuit simulator such as HSPICE to carry out circuit level evaluations.

The circuit level simulations take as inputs the behavioral models for individual devices, circuit netlists with worst-case noise scenarios as well as fabric specific control and sequencing schemes. Different cascading and noise scenarios are evaluated and output waveforms are checked for signal integrity. Circuit level delay and fabric performance implications are also quantified from these simulations.

The methodology can be easily extended to account for parameter variation [16]. At the device-level, multiple I-V and C-V simulations are carried out based on varying device structures, doping parameters etc. The regression analysis may then be done to build expressions for current and capacitance as functions of the input voltage as well as the individual parameters (e.g. channel diameter, underlap etc.). The Monte Carlo simulation framework in HSPICE can then be used to build a library of delays/power numbers that can be incorporated into a higher level simulator for evaluating the implications of physical layer variability on a large-scale system. The methodology thus explores implications of physical layer and device assumptions on the fabric as a whole. While it has been explored extensively for the NASIC fabric, this integrated methodology is fairly generic and is applicable to other nano-fabrics as well.

IV. DEVICES

Crossed nanowire field-effect transistors (xnwFETs) are the active devices in NASIC designs. A typical inversion-mode xnwFET device structure targeting NASICs is shown in Fig. 4(a). In this, the top Silicon nanowire acts as the gate and modulates the conductivity of the bottom Silicon nanowire, which is the channel. In an n-type xnwFET, the gate, source and drain regions are doped n^+ and the channel is p-type. Applying a positive voltage on the gate causes

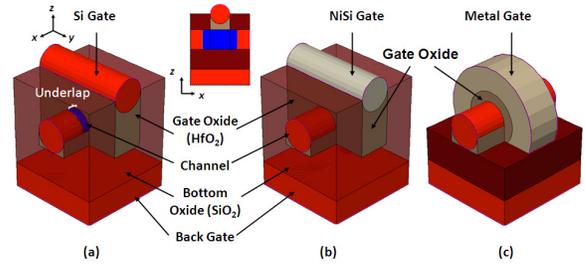


Fig. 4. Crossed Nanowire Field Effect Transistors (a) Basic device structure with self-aligned n^+ drain, gate, source and underlap (b) NiSi gate xnwFET (c) Omega-gated xnwFET.

TABLE I
DEVICE SIMULATION OUTPUT

	Si Gate		NiSi Gate		Omega-Gate	
V_{TH} (V)	0.21	0.32	0.22	0.31	0.21	0.31
I_{ON} (μA)	1.31	0.69	5.37	3.95	18.5	12.9
I_{ON}/I_{OFF}	6798	29831	1773	12046	10782	77875
Intrinsic delay (ps)	2.38	4.43	1.13	1.49	0.59	0.81

inversion in the p-region creating an n-type channel. A thin layer of high-permittivity (high-k) dielectric material (e.g. HfO_2) separates the gate from the channel. The gate oxide is defined using an oxide fill and gate self-aligned etch-back process.

The properties of a xnwFET device can be modified by changing the gate-underlap, the substrate bias as well as the gate material. For example, it is possible to create a fully-silicided (FUSI) gate (Fig. 4(b)) with nickel deposition and annealing. This eliminates some undesired effects such as gate depletion, and reduces the resistance of the gate nanowire needed for fast evaluation of the previous logic stage. Also NiSi gives a smaller gate-substrate workfunction difference and therefore, there is no need of applying large substrate biases or using large source/drain underlaps to achieve the desired threshold voltage. Alternatively, metal omega gates (Fig. 4(c)) could be used. This structure was chosen because it has a better gate to channel coupling than the two previous structures. Therefore it should have a better on current (I_{ON}) as well as a higher on-to-off current ratio (I_{ON}/I_{OFF}).

The three different xnwFET structures were simulated in Synopsys Sentaurus according to the methodology presented in Section II. Simulations were calibrated against experimental data from well characterized nanowire channel FETs with similar dimensions was employed [17], [18] to include effects such as carrier scattering due to surface roughness, and dielectric/channel interface trapped charges. By modifying the underlap, substrate bias, and gate workfunction values, two different threshold voltages, one approximately 0.2 V and another 0.3 V were obtained for each of the structures. The choice of threshold voltage, the intrinsic delays as well as the on/off current ratios have important implications for noise, as will be discussed in the next section.

The characteristics of the three nanowire transistor structures are summarized in Table I. For a given threshold voltage, the silicon gate xnwFET has the smallest I_{ON} , followed by the NiSi gate xnwFET and the Omega-gated xnwFET has

the highest I_{ON} as expected. First the NiSi structure has a higher I_{ON} than the Si gate structure because the Φ_{MS} value is lower for NiSi. Therefore a smaller source/drain underlap is needed to achieve the same V_{TH} , which in turn reduces the effective channel length, raising the drain current level. For the Omega-gated xnwFET, the higher current level is due to the increased ability of the gate to modulate the channel conductivity. In the Si gate or NiSi gate xnwFET structure, the inversion layer needed to turn on the device is formed mostly on the top part of the channel nanowire, near the gate nanowire, whereas in the Omega-gated xnwFET, the inversion layer can be formed almost all around the channel nanowire and therefore, this can be thought as increasing the effective channel width at the same gate voltage. Device-level performance can be further improved using techniques such as strain engineering to improve mobility of devices.

In addition to inversion mode devices, recent work in NASICs has focused on depletion-mode junctionless xnwFETs similar to junctionless devices proposed in [19]. Instead of sharp $n^+/p/n^+$ junctions for inversion behavior these devices are uniformly doped n^+ with the gate workfunction difference depleting the channel providing a positive threshold voltage. The key intuition is that this is possible at the nanoscale due to the ultra-small channel cross-section. In addition to simplifying manufacturing requirements at the device-level, the simplified doping profile implies significant reduction in manufacturing requirements for the NASIC manufacturing pathway [20], since it enables a grid-first functionalization approach. These devices also have bulk conductance, as opposed to inversion-layer conductance, implying potential for better intrinsic delays. Junctionless xnwFETs meeting V_{TH} and I_{ON} requirements have been simulated. Further device engineering optimizations are currently ongoing.

V. CIRCUITS

As discussed in section II, NASICs use a dynamic circuit style with control driven from external microwires. While this circuit style is amenable to implementation on regular nanowire grids with limited customization and no arbitrary sizing or routing of signals, noise and functionality issues for dynamic circuit styles need to be carefully managed due to high output impedance.

The six inversion-mode devices described in Section IV were evaluated for a worst-case circuit to evaluate noise implications and functionality [21]. The three-stage cascaded test circuit used in these noise evaluations is shown in Fig. 5. Stage 1 generates imperfect outputs that drive input xnwFETs of stage 2. Output integrity is checked at output nodes $do21$ and $do31$. Due to high output impedance during the hold phase, the output nodes at various stages may be susceptible to noise effects across device parasitic capacitances.

For example, key sources of noise for the $do21$ node include the Miller capacitances between this node and $do11$ and $do31$ nodes. If $do11$ evaluates to '0' it might cause a downward glitch (degradation of logic '1') at $do21$ due to the

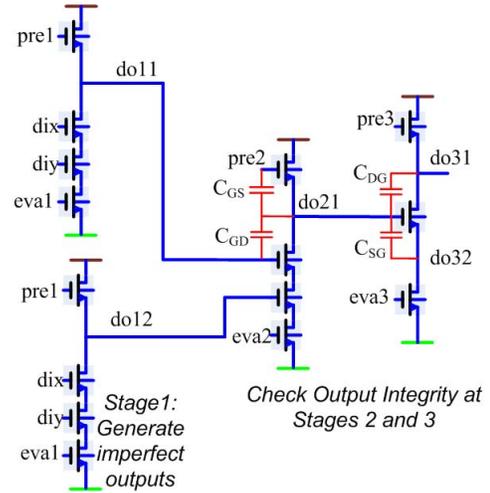


Fig. 5. Test circuit used for cascading evaluations.

C_{GD} capacitance between $do11$ and $do21$. Similarly, if $eva3$ is asserted, a downward glitch may occur at $do21$ due to the C_{SG} parasitic capacitance. Precharging of $do31$ could cause an upward glitch at the $do21$ node. Other similar parasitic effects exist between outputs and intermediate nodes in the design, leading to glitching and internal noise events.

Fig. 6 shows output waveforms for the NiSi 0.2 (left) and Omega 0.2 (right) devices for the 3-phase control scheme described in Fig. 2. In this control scheme, logic '1' glitching effects are not very severe. During the stage 2 hold phase, there can be some downward glitching due to C_{SG} between $do21$ and $do32$, in this scheme the parasitic capacitance C_{GD} to $do11$ does not hurt logic '1' integrity, since $do11$ is actually precharging during the stage 2 hold phase.

However, in this sequencing scheme, logic '0' glitching is an important consideration. Due to precharging of node $do11$, the output node $do21$ might have an upward glitch from logic '0' during its hold phase. For the Omega 0.2 device this upward glitch might cause a logic '0' value to reach above the threshold voltage of the device. Given that this device has the lowest intrinsic delay of all devices considered, the glitch may be sufficient to cause the stage 3 input xnwFET to operate in the linear region, leading to loss of signal integrity (Fig. 6 – right). In other words, faster devices are less resilient to logic '0' glitching effects. Of the 6 devices considered, the slowest NiSi 0.3 and Si 0.3 devices fail due to logic '1' glitching effects (i.e. logic '1' at an input is not sufficiently high to discharge a given stage), whereas the Omega 0.2 fails due to the logic '0' glitching. NiSi 0.2, Si 0.2 and Omega 0.3, which are middle-of-the-road devices in terms of intrinsic delay, pass all signal integrity tests and are correctly evaluated.

A. Noise-resilient control scheme

The 3-phase control scheme cannot be made functional with faster devices, owing to logic '0' glitching effects described previously. However, since control schemes are driven externally and do not have any nanoscale customization, it is possible to alter them without imposing new manufacturing requirements, alleviating noise effects and enabling

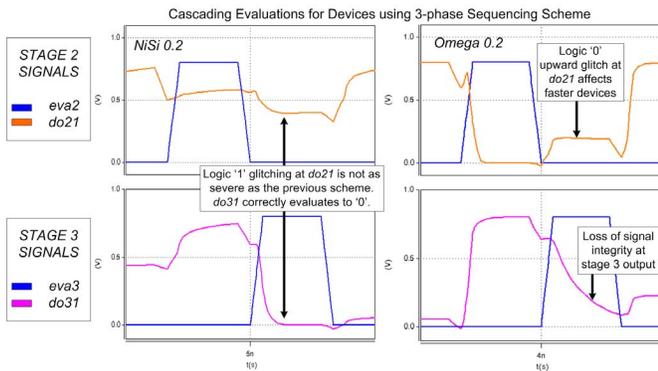


Fig. 6. Cascading evaluations for NiSi 0.2 and Omega 0.2 devices using 3-phase sequencing scheme.

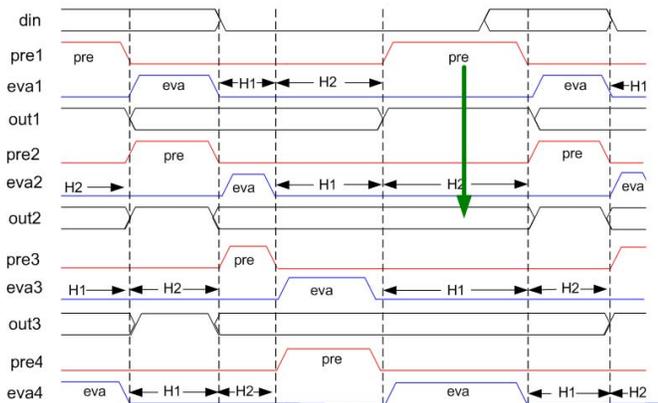


Fig. 7. Noise resilient 4-phase sequencing scheme for the NASIC fabric. faster devices. In this subsection, we present and evaluate a new noise-resilient dynamic control scheme that provides resilience against both logic ‘1’ and logic ‘0’ glitches across a variety of devices. The scheme is described and all devices are evaluated against it for the test circuit (Fig. 5).

Fig. 7 shows the new noise resilient sequencing scheme. Similar to the 3-phase scheme, *eva* phase of any stage overlaps with *pre* of the next stage. Also, since both neighboring stages do not simultaneously discharge, logic ‘1’ glitching is less severe than in the first scheme. However, the key difference for the noise resilient scheme is the introduction of a second hold stage (labeled *H2* in Fig. 7) to separate evaluation events from noise events. For example, in the 3-phase scheme (Fig. 2), *do11* precharging can cause an upward glitch at *do21*, which affects logic ‘0’ integrity. However, with the new scheme *do21* has already been ‘used’ as input for the next stage, i.e. *eva3* has completed before the noise event (i.e. *pre1*) occurs (shown by the green arrow in Fig. 7). In this new control scheme, signals repeat every four stages.

Fig. 8 shows the output waveforms for the Omega 0.2 device with the new noise resilient scheme. As expected, the logic ‘0’ at *do21* is already consumed before the glitching event occurs and does not affect *do31*. During *eva3*, stage 1 is in the new *H2* phase, which essentially isolates the noise event from the propagation event preserving signal integrity. Thus, using the new noise resilient timing schemes, devices

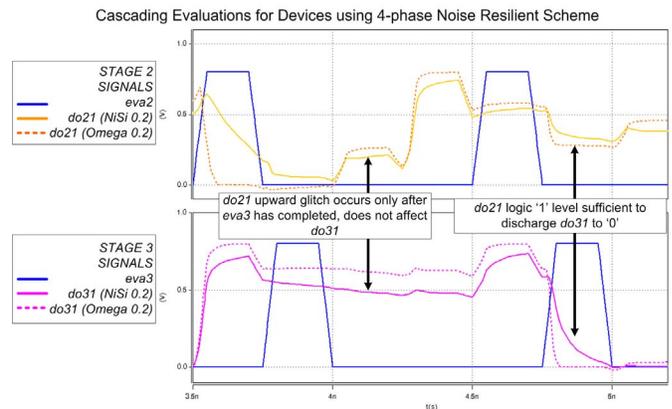


Fig. 8. Cascading evaluations for NiSi (solid) and Omega (Dotted) devices using the noise resilient 4-phase control scheme.

with lower intrinsic delays may be made functional in the NASIC fabric.

B. Performance Optimization

The 4-phase noise resilient scheme enables xnwFETs with lower intrinsic delays. However, even with faster devices, NASIC dynamic circuits need to be optimized for performance. Specifically, due to noise cascading effects and high output impedance, charge at driving nodes and the associated gate-driven voltages are typically expected to be lower than V_{DD} . Since I_{ON} is strongly dependent on V_{GS} , this implies that even devices with low intrinsic delays (e.g. Omega 0.2) may be operating at sub-optimal points. This leads to large evaluation delays and poor circuit performance. Therefore, circuits need to be optimized in-Fabric to improve V_{GS} and performance. However, conventional approaches such as keeper devices or domino logic are not compatible with a regular fabric with limited customization.

One promising technique for increasing charge at the driving nodes is capacitance engineering. The key idea is to increase the overall capacitance (and consequently the charge stored) at input nodes, thereby reducing the magnitude of noise glitching, leading to higher gate voltages. While increased load capacitance at a node will have a linear impact on performance; the expectation is that a net benefit will be achieved due to the better-than-linear relationship between I_{ON} and V_{GS} . Importantly, this technique does not impose new manufacturing challenges. A capacitance trench [22] may be created at an input stage, increasing net capacitance of all input nodes in that stage (Fig. 9). This would be done at the granularity of a NASIC stage (typically 10s – 100s of nm) using conventional photolithography steps and be easier to achieve than in a conventional DRAM process, which requires isolated capacitors for every memory bit.

Experiments were done to characterize the evaluation delay of NASIC dynamic circuits as a function of fan-in. Maximum operating frequency is defined as $1/N * delay$, where N is the number of distinct evaluate phases in the control scheme (explicitly, N is 4 for 4-phase). The reasoning is that the minimum duration of any single evaluate phase has to be at least equal to the delay for completely

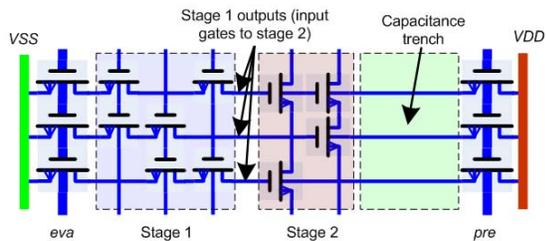


Fig. 9. Capacitance engineering of input gates: adding gate capacitance at outputs of Stage 1 increases gate-drive voltages of Stage 2 xnwFETs.

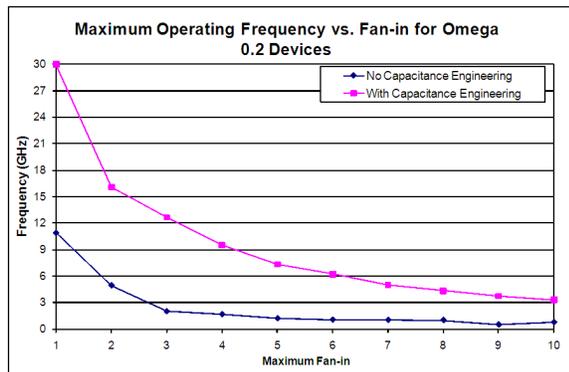


Fig. 10. Maximum operating frequency with and without capacitance loading vs. fan-in.

discharging the output node through the pull-down network. Capacitance was varied over a wide range of values. For capacitance loading between 9 aF and 30 aF, only a 5% standard deviation observed, implying that performance is not very sensitive to variations in the capacitance values. This is because as xnwFETs operate further in saturation, the net improvement in on-current due to operating a device at higher V_{GS} is more linear, and offset by the output load capacitance.

Fig. 10 shows the maximum operating frequency vs. maximum fan-in for the Omega 0.2 device with and without capacitance engineering. A consistent 4.5-6X performance improvement is seen for all fan-ins with capacitance engineering (e.g. for fan-in 10, maximum operating frequency increases from 798 MHz to 3.34 GHz). These results attest to the importance of achieving high drive voltages at input nodes.

VI. DEFECT TOLERANCE AND VARIATION RESILIENCE

Nanoscale computing fabrics are subject to high levels of parameter variation in conjunction with high defect rates. In this section we review recent advances in evaluating parameter variation for a nanoscale computing fabric and describe built-in fault tolerance techniques to mitigate variation.

Table II summarizes physical parameters and extent of variation for an inversion-mode xnwFET (Fig. 4). At the device-level, variation in physical parameters affects on-currents of the devices as well as parasitic capacitances. I_{ON} variation for parameters varying one-at-a-time is also shown. Channel diameter has up to a 3.5X impact on I_{ON} , followed by device underlap and bottom-oxide thickness. Full characterization of I-V curves for devices was carried out using

TABLE II
DEVICE PARAMETERS AND EXTENT OF VARIATION

Parameter	Nominal	Deviation	I_{ON} variation
Channel diameter (Cdiam)	10nm	10%	352%
Gate diameter (Gdiam)	10nm	10%	181%
Underlap (Ulap)	4nm	10%	147%
Gate oxide thickness (Gox)	3nm	10%	58%
Bottom oxide (Box)	10nm	10%	24%
Channel doping (Cdop)	$10^{18}/cm^3$	10%	16%
Source-drain doping (Sddop)	$10^{20}/cm^3$	10%	12%

Synopsys Sentaurus and behavioral models describing the current as a function of voltages and physical parameters was built. This was then incorporated in HSPICE for circuit simulations.

Behavioral models of device data were used to characterize the delays of NASIC N-input NAND gates. The Monte Carlo framework in HSPICE was used for these simulations, with individual parameters sampled independently. As expected, channel diameter and underlap had the maximum impact on circuit level delays, with up to 150% and 117% side-to-side deviation across nominal. A library of delays was created for different fan-ins, and this information was used by a custom-built architectural simulator to evaluate the impact on a the NASIC WISP-0 [2], [3] processor design.

The architectural simulator samples delays for each gate in the design and the maximum operating frequency at which the processor functioned without missed deadlines is estimated. It was shown that parameter variation causes 67% of the samples investigated to operate at frequencies below nominal.

Nanoscale fabrics based on self-assembly manufacturing processes tend to have very high defect rates (in NASICs we assume 10 orders of magnitude higher than CMOS or 100s of millions to billions of defective devices per cm^2) that necessitates the use of built-in fault tolerance for achieving acceptable effective yield. These techniques may also provide resilience against parameter variation related timing faults, since the fault-tolerance is agnostic to the source of the fault (permanent defects or parameter variation) and may be leveraged for parameter variation resilience. Results of simulations with simple 2-way and 3-way redundancy schemes showed that up to 75% of chips were operating at frequencies better than nominal, implying that redundancy helps against parameter variation in conjunction with permanent defects.

A. FastTrack: Leveraging asymmetric delay paths

A new family of fault tolerance schemes tailored towards parameter variation as opposed to defects was developed. In NASIC designs, owing to the dynamic circuit style where signals are precharged to '1' followed by evaluation, faulty '0's are less likely (a faulty '0' would require multiple stuck-on devices and/or multiple input faulty '1's). Furthermore, the delay of a stage is determined by the evaluation of a pull-down stack to '0'. This implies that voting schemes biased towards logic '0' could be used in conjunction with input modules with varying levels of redundancy. This would imply that a '0' on a low redundancy module could be fast-

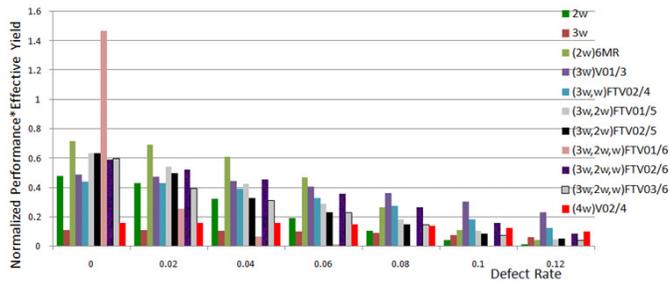


Fig. 11. Normalized performance * Effective yield vs. defect rate for redundancy, biased voting and FastTrack schemes

tracked to the next stage, without waiting for slower paths to switch, thereby improving the overall performance.

Performance * Effective Yield (PEY) products for a suite of FastTrack techniques is presented in Fig. 11. All techniques are specified by the input module organization in conjunction with a biased voting scheme. For example, $(3w,w)FTV_0^{2/4}$ represents two input modules, 3-way and no-redundancy, with a voting bias of 2 out of 4 zeros, i.e. the first 2 '0's will be fast-tracked to the next stage by the biased voter. At zero defect rate, the $(3w, 2w, w)FTV_0^{1/6}$ works best owing to its large performance advantage (20X faster than the 3-way redundancy scheme). However, its PEY product falls off rapidly with increasing defect rates owing to deterioration in yield. Therefore, while the $(3w, 2w, w)FTV_0^{1/6}$ technique has the best performance, it may not be suitable for cases where both yield and performance targets need to be met.

VII. ALIGNMENT AND OVERLAY CONSIDERATIONS

One key challenge for nanofabrics is registration between lithographic and nano-material layers. While conventional lithography masks have excellent overlay alignment (projected to be $3\sigma = 3.3\text{nm}$ for 16nm CMOS [23]), unconventional manufacturing processes such as imprint lithography suffer from poor overlay alignment ($3\sigma = 105\text{nm}$ [24]), which implies significant challenges in alignment against previously formed CMOS features.

In NASICs, an initial array of nanowires is patterned on the substrate *a priori* to lithographic functionalization. The uniform pattern of nanowires implies that an initial mask can be offset in one direction on the grid with no loss of functionality. Additionally, if a technique such as imprint lithography is used, alignment markers can be created as part of the mold itself, and transferred to the substrate. This implies that subsequent photolithographic steps for functionalization and creation of contacts will be very precise.

Yield implications of successive mask overlays were studied through simulation. Mask overlays were modeled as Gaussian random variables, and Monte Carlo simulations were carried out in a logic simulator to determine number of functioning chips. The results (Fig. 12) show that close to 75% yield is obtained for $3\sigma = \pm 5.7\text{nm}$ (manufacturing solutions known, according to ITRS), implying that mask overlay problems are alleviated in regular nanoscale fabrics with *a priori* nano-feature assembly.

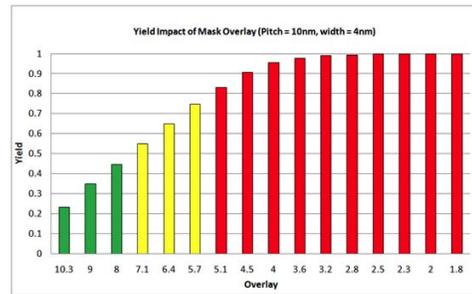


Fig. 12. Overlay-limited yield for NASICs

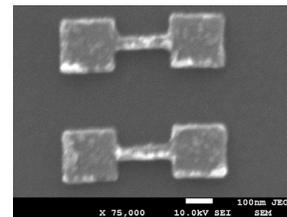


Fig. 13. Sub-50nm width nanowires direct patterned on SOI

VIII. MANUFACTURING APPROACHES

This section details recent efforts towards realization of NASICs. A prototyping approach based on direct patterning of SOI wafers with e-beam lithography and a scalable approach involving *ex-situ* alignment are discussed.

A. NASIC prototyping update

The objective of the NASIC prototyping effort is to demonstrate a functional NASIC block incorporating xn-wFETs and NASIC dynamic circuit styles. The first goal is to build and characterize junctionless xnwFETs at sub-50nm dimensions for both gate and channel. High-resolution Polymethyl Methacrylate (PMMA) positive photoresist was used for patterning sub-50nm channel features. Titanium was evaporated followed by lift-off to create an etch mask for pattern transfer. Titanium is chosen for its excellent adhesion to Silicon and subsequent easy, highly selective removability with dilute Hydrofluoric acid solution. Pattern transfer to the SOI was done using a highly anisotropic Reactive Ion Etch (RIE) using an SF_6/CHF_3 recipe, where SF_6 is used for the actual etching, and CHF_3 for sidewall passivation, similar to [25]. Nanowires with width down to 35nm were demonstrated (Fig. 13). Top and sidewall oxide can be created using Plasma Enhanced Chemical Vapor Deposition (PECVD). A top metal (semiconductor) gate will be formed using evaporation (PECVD) followed by another selective anisotropic oxide etch to define a self-aligning gate. After characterization and optimization of devices, the approach will be scaled to a NASIC functional block.

B. Scalable Manufacturing Update

A parallel aligned nanowire array with intrinsic control over number of nanowires, pitch and width may be created by direct pattern transfer to an SOI substrate using Nanoimprint Lithography [24], SNAP [26] or other approaches [27], [28]. This approach also enables fine-grain integration with CMOS, with overlay requirements existing only for subsequent photolithography steps [29].

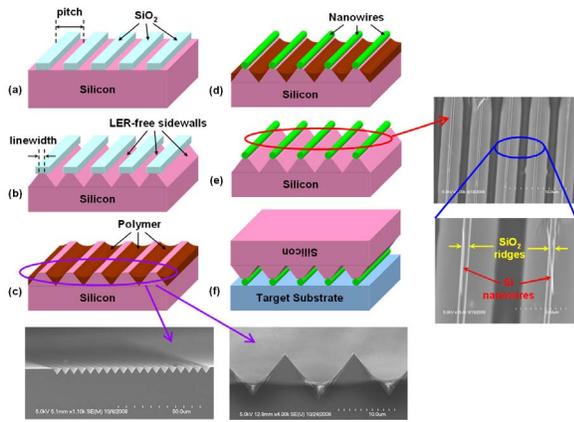


Fig. 14. Key manufacturing steps and selected accompanying SEM images of our nanowire array aligned assembly approach with intrinsic control. (a)-(c) Formation of a nanoscale line array on the assembling substrate with periodically dissimilar surface properties. (d)-(e) Conjugation of the aligned nanowires at the ridge of the LER-free triangular features. (f) Transfer of the aligned nanowire array onto the target substrate surface.

Additionally, *ex-situ* alignment and transfer approaches are also explored. Among various techniques [1], hybrid top-down/bottom-up directed self-assembly (DSA) are the most feasible per NASIC manufacturing criteria. The baseline strategy comprises three major steps: 1) Creation of an intrinsically controlled nanoscale periodic line array above the substrate surface 2) Selective conjugation of 1-D nanostructures only onto the lines within the array and 3) Transfer of the aligned nanostructure array to different substrates.

The approaches involved are based on wafer-scale, VLSI-compatible philosophy yet offer intrinsic control over the number, pitch, and linewidth of the resultant aligned nanostructure arrays (Fig. 14). Nanoscale, sub-lithographic pitch and linewidth are accomplished without advanced lithography. Selective conjugation of structures could be enabled by hydrophobic/hydrophilic interactions (e.g. crystallographic etch (Fig. 14)(c) or lamellar phase block copolymers). Alignment to pre-existing features on the target substrate during transfer is also inherently allowed. This work is ongoing yet preliminary results have revealed great promise of this novel technology.

IX. CONCLUSIONS AND FUTURE OUTLOOK

This fabric update provides a snapshot of recent developments for the NASIC fabric including devices, manufacturing approaches, noise and parameter variability implications as well as alignment requirements. Promising progress has been made in the areas of fabrication of xnwFETs and fabric prototypes, scalable manufacturing, alignment considerations as well as junctionless devices which could potentially simplify the manufacturing flow. While challenges still remain, it is hoped that a fully-functional NASIC fabric can be demonstrated in the near future.

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