CATASTROPHIC YIELD, PARAMETRIC YIELD AND RELIABILITY: CAN WE STILL VIEW THEM AS DISJOINT ISSUES?

(Invited Position Paper)

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A manufactured IC is operational at the desired levels of performance and reliability if:

1. It does not have catastrophic defects resulting in open- or short-circuit type faults;
2. It operates correctly at or above the desired frequency; and,
3. Its reliability is above a certain threshold, providing constrained sensitivity to phenomena like electromigration and hot-carrier effects.

The percentage of ICs which have no catastrophic defects is called the *catastrophic yield*. The percentage of ICs which do not have catastrophic defects *and* operate at or above the desired frequency is called the *parametric yield*. Catastrophic yield loss is mainly due to random spot defects, most of which are the result of unwanted dust or chemical particles deposited on the wafer during the many steps of manufacturing [6]. Parametric yield loss has been mainly due to global disturbances, such as mask misallignment and line width variations [3]. Unfortunately, this important distinction between the two kinds of yield is rarely discussed. The majority of technical publications concerned with yield and manufacturing issues use the term "yield" to refer to either parametric yield or catastrophic yield, but not to both. In almost all such publications the existence of the "other" kind of yield is completely ignored. In most cases reading the title, or even the abstract, is insufficient to decide which kind of yield is discussed, and one gets the impression that the author is unaware of the double meaning of the term.

This situation has been tolerable since the physical phenomena underlying the two kinds of yield loss were distinct, and as a result, the mathematical models and the techniques employed for improving the two different kinds of yield were completely different. Reliability issues have also historically been treated separately from either kind of yield, and justifiably so, because reliability-reducing factors were unrelated to yield.

This will not necessarily be true in the near future. If the current trend of increasing chip size and further reducing the already submicron feature size will continue as expected, designers will have to consider catastrophic yield, parametric yield and reliability simultaneously, and, in some cases, will have to make trade-offs.

We will illustrate the above through two examples, both concerning long on-chip interconnection lines.

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The first example illustrates the contribution to parametric yield loss which random spot defects may have in deep submicron technologies. We analyzed in [11] the effect of spot defects on the propagation delay of signals through two adjacent metal interconnection lines depicted in Figure 1. For high clock frequencies (200MHz and above) the effects of reflections in these transmission lines are not negligible and any discontinuities in the lines due to spot defects may result in an increase in the propagation delay of the signals.

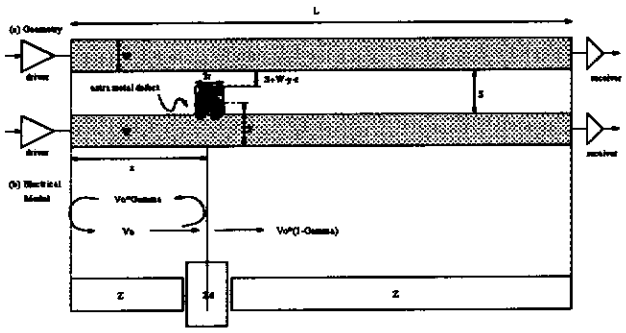

Figure 1. The effect of an extra metal defect on a line. The defect is modeled as a square of side $2r$.

Let f_0 denote the maximum possible operating frequency of the defect-free circuit (which in our simple example consists of two adjacent interconnection lines and the corresponding drivers). Let σ denote the *delay-increase factor* due to spot defects so that the propagation delay of a signal on the interconnection line increases by $(1+\sigma)$. This factor depends on the probability distribution function of the size of the defects which are assumed to be squares of size $2r \times 2r$ (see Figure 1). The operating frequency of the circuit reduces from f_0 to $f(\sigma)$ given by

$$f(\sigma) = \frac{f_0}{1+\sigma}$$

The following expression for σ has been derived in [11]

$$\sigma = \frac{2(x/L)^2 \log 2}{\log\left(\frac{S+W-y}{r}\right)}$$

where L and W are the length and the width of the line, respectively (see Figure 1), S is the line spacing, x is the distance between the driver and the center of the square defect and y is the distance between the bottom edge of the line and the center of the defect.

For the circuit to be operational at (or above) a given clock frequency f_m, the delay-increase factor must satisfy $\sigma \leq \sigma_m$ where σ_m is equal to $f_0/f_m - 1$. The value σ_m corresponds to a certain size r_m of a defect, and consequently, we can define and calculate the *delay-dependent critical area*, denoted by $A_c(\sigma_m)$, which is the generalization of the well-known critical area term for catastrophic defects. The latter is equal to $A_c(\infty)$. We can then write an expression for $A_c(f_m)$ and, define and calculate the *frequency-dependent yield*, denoted by $Y(f_m)$, using any existing yield model [5], [7].

If we select the simple Poisson yield model we obtain the results depicted in Figure 2, which shows the projected yield as a function of the frequency (assuming that the maximum working frequency of the defect-free interconnection line is $f_0 = 500$Mhz) for three different values of the line spacing. For very low values of the frequency f_m the projected yield is the catastrophic yield, while for high frequencies it is the (multiplicative) contribution to the overall parametric yield. From this figure we conclude that the separation between long lines should be much larger for frequencies above $0.4 f_0$, while in lower frequencies one may stick to the minimum spacing allowed by the technology ground-rules.

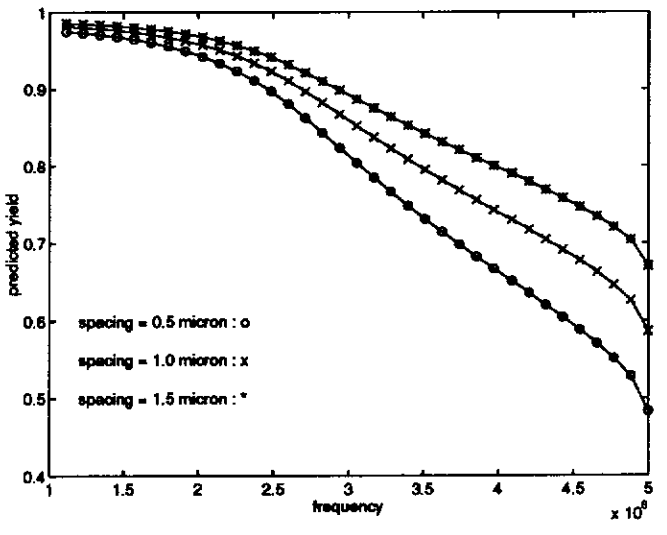

Figure 2. Yield vs. frequency for various values of the inter-line spacing S assuming that f_0 (the maximum working frequency of the line) is 500Mhz.

Our second example illustrates the fact that yield and reliability are not disjoint issues and that a tradeoff between the two is sometimes required. Various wear-out and internal noise mechanisms affect the reliability of VLSI circuits. These include the electromigration, crosstalk, thin oxide breakdown and leakage current phenomena. In the next example we focus on the crosstalk noise. Crosstalk between two wires is proportional to the coupling capacitance between the wires, which in turn is proportional to their coupling length (the total length of their overlapping segments), and inversely proportional to their separating distance [9]. A similar relationship exists between the sensitivity to short-circuit type defects and the layout parameters. Therefore, techniques similar to those for short-circuit critical area reduction can be used to minimize crosstalk faults [2]. For example, in order to reduce the catastrophic yield losses due to short-circuit type faults, spacing between some of the interconnect lines is increased. This redistribution of spacing will also help to minimize the crosstalk faults [8]. Our results [1] show that layout modifications for yield enhancement will also improve the circuit crosstalk reliability due to reduced coupling capacitance. However, the optimal solutions for yield and coupling are not always the same, mostly because they react differently to a change in the separating distance. In crosstalk, coupling capacitance between two lines is proportional to $s^{-1.45}$, where s is the distance between the two lines [9]; while in yield, the short-circuit critical area is proportional to s^{-3}. A simple example in Figure 3 illustrates the difference between the optimal results for the two objectives. We should conclude therefore, that in the future trade-offs between the yield and reliability objectives will often be required, and that yield and reliability are in fact intimately related.

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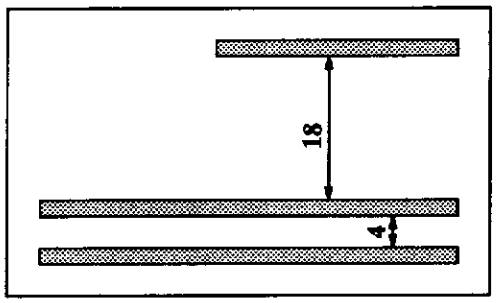
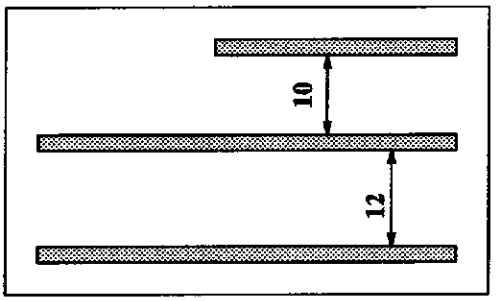
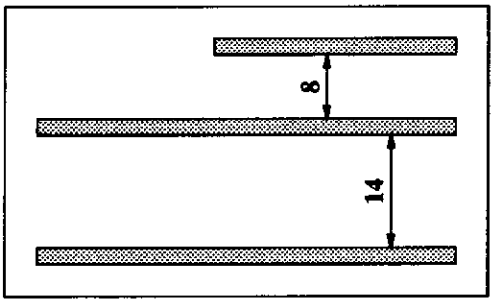


(a) Original Layout



(b) Layout for Yield Optimization



(c) Layout for Crosstalk Minimization

Figure 3. Difference between yield and crosstalk optimization.