A Unified Negative-Binomial Distribution for Yield Analysis of Defect-Tolerant Circuits

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***Abstract*—It has recently been recognized that the yield of fault-tolerant VLSI circuits depends on the size of the fault clusters. Consequently, models for yield analysis have been proposed for "large-area clustering" and "small-area clustering," based on the two-parameter negative-binomial distribution. We propose the addition of a new parameter, the *block size*, to the two existing parameters of the fault distribution. This new parameter allows us to unify the existing models and at the same time add a whole range of "medium-size clustering" models. Thus, we increase the flexibility in choosing the appropriate yield model. We present methods for estimating the newly defined block size and validate our approach through simulation and empirical data.**

***Index Terms*— Block-size estimation, defect tolerance, fault clusters, negative-binomial distribution, VLSI circuits, yield.**

I. Introduction

When manufacturing fault-tolerant VLSI circuits, the precise estimation of the yield is crucial since it determines the amount of redundancy to be added to the circuit. The accuracy of the estimated yield depends on the statistical model selected to describe the spatial distribution of manufacturing faults. We make the distinction between physical *defects* and circuit *faults*. A defect is any imperfection on the wafer, but only the fraction of defects that actually affect the circuit operation are called faults. Since our purpose is yield estimation, we concentrate in this paper on modeling the distribution of faults rather than that of defects.

For some time in the past the Poisson distribution was used to model the spatial distribution of faults on the wafer. This implies that the faults occurring in any two distinct areas are statistically independent, resulting in relatively simple yield calculations. Researchers today agree that the distribution of manufacturing faults has more clusters than predicted by the Poisson distribution [1]. Several distributions that allow such increased clustering of faults have been suggested, most notably the negative-binomial distribution, which was shown to have a good fit with actual fault distributions.

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The negative-binomial distribution has two parameters, λ and α. Assuming that the number of faults in an area of size A has a negative-binomial distribution with the parameters λ_A and α_A enables the calculation of the probability of x faults occurring in the given area, namely

$$\text{prob}(x \text{ faults in area } A) = \frac{\Gamma(\alpha_A + x)}{x!\Gamma(\alpha_A)} \frac{(\lambda_A/\alpha_A)^x}{(1+\lambda_A/\alpha_A)^{\alpha_A + x}} \quad (1)$$

where λ_A is the expected number of faults in area A, and α_A is the clustering parameter for the considered area, measuring the deviation from the Poisson distribution. The smaller its value, the larger this deviation. In particular, (1) enables calculating the probability of zero faults in area A that, if no redundancy exists, constitutes the yield of this area

$$\text{yield} = \text{prob}(0 \text{ faults in area A}) = (1+\lambda_A/\alpha_A)^{-\alpha_A}. \quad (2)$$

In yield calculations, however, it is often desirable to find probabilities pertaining to subareas of A (when some redundancy exists in A) or to extrapolate the probability to areas larger than A (when a larger circuit is designed). The two parameters (λ_A, α_A) are insufficient for any of these two purposes. They only specify the probability of x faults occurring in A but not the way in which these faults are distributed over area A. Two negative-binomial random variables with the same λ_A, α_A may have completely different clustering patterns and, consequently, different yield expressions when areas either smaller or larger than A are concerned. Note that the parameter λ_A can be easily interpolated or extrapolated to an area of any size A^* by $\lambda_{A^*} = \lambda_A \cdot (A^*/A)$. The parameter α, however, can not be extended to an area other than A without some additional information regarding the clustering pattern.

Most of the proposed models for estimating the manufacturing yield of fault-tolerant VLSI circuits have noticed this inadequacy of the two-parameter negative-binomial distribution and assumed "large-area clustering" [2]. Under this assumption, the size of the clusters is comparable to the size of the wafer, implying that the faults over the whole wafer are correlated, that the number of faults in any subarea of the wafer has a negative-binomial distribution, and that the parameter α is constant for any subarea of the wafer.

"Small-size clustering" is discussed in [3]. Under this assumption, the wafer is divided into small blocks that are statistically independent. Any subarea of the wafer is assumed to consist of a whole number of these blocks, and hence the faults in any disjoint subareas are independent. In addition,

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the number of faults in any subarea has a negative-binomial distribution, and the parameter α is proportional to the area.

Some papers ignore the clustering pattern altogether. An attempt to deal with the size of the clusters has been made in [4]; however, the approach there is impractical due to the prohibitive number of parameters in the model. Muehldorf [5] has presented a nonparametric method for determining clustering, but no method for calculating the effect of clustering on the yield is proposed. Another approximate model in which clusters are mentioned is presented in [6]. The proposed model assumes that every area on the wafer has a negative-binomial distribution, which for medium-size clustering is mathematically incorrect (as will be proven in Section II). Moreover, no method for calculating the yield of a chip with redundancy is suggested.

In this paper we do not attempt to define a cluster or to investigate cluster sizes and their effect on the yield. Instead, we view the clustering as an empirical phenomenon that is the result of the wafer area being divided into subareas we call *blocks*, such that the faults in distinct blocks are statistically independent. The number of faults in each block has a negative-binomial distribution, with a uniform distribution within the area of the block. The faults in partial areas of the same block are, therefore, correlated. We suggest the addition of the *block size* as the third parameter of the spatial negative-binomial distribution. This new parameter enables us to treat in a unified manner "small-area clustering" and "large-area clustering," which until now have been treated in two different ways, and "medium-area clustering" for which, to the best of our knowledge, no satisfactory model has been developed.

The notion of "block size" (to be defined in the next section) has several advantages over the previously used "cluster size." It can be defined mathematically, while we have not found any satisfactory definition of the cluster size. Due to the exact definition, statistical properties of the fault distribution can be proven rigorously. One such property that is significant for yield calculation is that the parameter α remains constant as long as the considered area is confined within the same block and increases when the area consists of more than one block. The introduction of the block size also enables the development of a unified approach to yield calculation for the different "cluster sizes." This provides more flexibility in choosing an appropriate yield model, and can be used in determining the sensitivity of the calculated yield to the specific block size assumed.

The objective of this paper is, therefore, to introduce a unified approach to yield analysis by adding a third parameter, i.e., the block size, to the two existing parameters of the negative-binomial distribution and to demonstrate its use when calculating the yield of fault-tolerant circuits.

This paper includes several results presented in [7] and [8]. These results are briefly reviewed here for the sake of completeness. The paper is organized as follows. In the next section we describe the yield model and define the suggested parameter—the block size. Section III demonstrates the use of the block size in calculating the yield of a chip with some redundancy in it. In Section IV we propose statistical methods for estimating the block size for given empirical data. Section V presents some numerical results that demonstrate and validate the use of the block size in yield calculations. Final conclusions are presented in Section VI.

II. The Model Description

In our model, a chip consists of basic units called modules. A module is a circuit block such as a memory subarray or a digital-logic macro that is replicated in a chip. The area of a module is assumed to be the unit area, and all other areas are measured in these units. To illustrate the use of the suggested third parameter for the unification of yield models we chose the problem of calculating the yield of a chip consisting of N identical modules, out of which M are needed for proper operation and $N-M$ are spares that can replace any of the M modules if they are faulty. The same analysis can be applied to the calculation of the yield of partially good chips, i.e., chips that have no redundancy but can still be used (though to a lesser degree) when some of their modules are faulty.

Any fault-tolerant circuit must include, in addition to the functional modules, some control circuitry whose purpose is to reconfigure the fault-free modules into an operational chip. In this paper we do not take this circuitry into account, since its inclusion in the calculation will only complicate the equations and will not add any insight into the fault model. Our model does allow the inclusion of the control circuitry in the yield calculation without assuming statistical independence between the functional and control circuits, but the specific layout of the circuit has to be considered in this case as further explained in Section III.

We further assume that a wafer consists of W modules and that the number of faults per wafer has a negative-binomial distribution with parameters (λ_w, α_w). The yield of the chip is the probability that at least M out of the N modules are fault-free, a probability whose calculation involves dealing with subareas of the chip. Hence, as explained before, the two parameters (λ_w, α_w) are insufficient and a third parameter is required to indicate which subareas within the wafer (and, consequently, within the chip) are statistically independent with respect to manufacturing faults. We suggest the use of a parameter called *block size* defined as follows.

Definition: The block size is the smallest number B such that the wafer can be divided into disjoint areas of size B modules each, so that these areas are statistically independent with respect to manufacturing faults.

The relationship between the block size and the cluster size is not very clear, mainly because there is no rigorous definition of the term "cluster size." Intuitively, the blocks form a division of the wafer into subareas in such a way that distinct fault clusters are contained in distinct blocks. However, actual clusters can be either smaller or larger than B.

In the next theorem we state several properties of the block size. In particular, we prove that the block possesses the same property formerly attributed to the cluster, namely, that the parameter α is constant for all areas within the same block and increases linearly with the number of blocks included in the given area.

Theroem 1: Let the number of faults in the wafer have a negative-binomial distribution with parameters (λ_w, α_w) and block size B, and let W denote the wafer size (measured in number of modules), then

1) The number of faults in a block has a negative-binomial distribution with parameters (λ_b, α_b), where

$$\lambda_b = \frac{\lambda_w}{W/B} \qquad \alpha_b = \frac{\alpha_w}{W/B} \tag{3}$$

and the block-size parameter equals B.

2) For any area of size A contained in one block, the number of faults has a negative-binomial distribution with parameters $(A/B\lambda_b, \alpha_b)$ and block size A.

3) For any area consisting of C complete blocks, the number of faults has a negative-binomial distribution with parameters $(C\lambda_b, C\alpha_b)$ and block size B.

Proof: The proof of all three parts of the theorem is based on the generating function of the negative-binomial distribution. Let $P(x)$ denote the probability function of a negative-binomial random variable with parameters (λ, α), and let $T(z)$ denote the corresponding generating function. Then,

$$\begin{aligned} T(z) &= \sum_{x=0}^{\infty} P(x) z^x \\ &= \sum_{x=0}^{\infty} \frac{\Gamma(\alpha + x)}{x!\Gamma(\alpha)} \frac{(\lambda/\alpha)^x}{(1+\lambda/\alpha)^{\alpha+x}} z^x \\ &= \left(1 + \frac{(1-z)\lambda}{\alpha}\right)^{-\alpha} \end{aligned} \tag{4}$$

Let $T_w(z)$, $T_b(z)$, $T_a(z)$, and $T_c(z)$ denote the generating functions of the number of faults in the wafer, in a block, in an area of size A contained in a block, and in an area consisting of C blocks, respectively.

1) Since there are W/B independent blocks in the wafer

$$T_w(z) = (T_b(z))^{\frac{W}{B}}$$

hence

$$\begin{aligned} T_b(z) &= (T_w(z))^{\frac{B}{W}} \\ &= \left(1 + \frac{(1-z)\lambda_w}{\alpha_w}\right)^{-\frac{B}{W}\alpha_w} \\ &= \left(1 + \frac{(1-z)\frac{B}{W}\lambda_w}{\frac{B}{W}\alpha_w}\right)^{-\frac{B}{W}\alpha_w} \end{aligned} \tag{5}$$

The right most side of (5) is the generating function of a negative-binomial distribution with parameters $(\frac{\lambda_w}{W/B}, \frac{\alpha_w}{W/B})$. The block size is clearly B.

2) Let $P_b(x)$, $P_a(x)$ be the probability functions of the number of faults in the whole block and in the partial area A, respectively. Given a fault in the block, its distribution inside the block area is uniform and its probability of falling within area A is A/B. Hence,

$$P_a(x) = \sum_{i=x}^{\infty} P_b(i) \binom{i}{x} \left(\frac{A}{B}\right)^x \left(1 - \frac{A}{B}\right)^{i-x}$$

and

$$\begin{aligned} T_a(z) &= \sum_{x=0}^{\infty} P_a(x) z^x \\ &= \sum_{x=0}^{\infty} \sum_{i=x}^{\infty} P_b(i) \binom{i}{x} \left(\frac{A}{B}\right)^x \left(1 - \frac{A}{B}\right)^{i-x} z^x. \end{aligned}$$

By interchanging the order of summation we obtain

$$\begin{aligned} T_a(z) &= \sum_{i=0}^{\infty} P_b(i) \sum_{x=0}^{i} \binom{i}{x} \left(\frac{zA}{B}\right)^x \left(1 - \frac{A}{B}\right)^{i-x} \\ &= \sum_{i=0}^{\infty} P_b(i) \left(1 - \frac{A}{B} + \frac{zA}{B}\right)^i \\ &= T_b\left(1 - \frac{A}{B} + \frac{zA}{B}\right) \end{aligned}$$

Since

$$T_b(z) = \left(1 + \frac{(1-z)\lambda_b}{\alpha_b}\right)^{-\alpha_b}$$

it follows that

$$T_a(z) = \left(1 + \frac{\frac{A}{B}(1-z)\lambda_b}{\alpha_b}\right)^{-\alpha_b} \tag{6}$$

The last expression is the generating function of a negative-binomial distribution with parameters $(\frac{A}{B}\lambda_b, \alpha_b)$. Since B is the block size for the whole wafer and $A < B$, the block size for the partial area must be A.

3) The C blocks are independent with respect to faults, each having a generating function $T_b(z)$, hence

$$\begin{aligned} T_c(z) &= (T_b(z))^C \\ &= \left(1 + \frac{(1-z)\lambda_b}{\alpha_b}\right)^{-C\alpha_b} \\ &= \left(1 + \frac{(1-z)C\lambda_b}{C\alpha_b}\right)^{-C\alpha_b} \end{aligned} \tag{7}$$

which is the generating function of a negative-binomial distribution with parameters $(C\lambda_b, C\alpha_b)$. The block-size parameter is clearly equal to B.

Corollary: The module parameters (λ_m, α_m) can be obtained as follows

$$\lambda_m = \frac{\lambda_b}{B} = \frac{\lambda_w}{W} \tag{8}$$

$$\alpha_m = \alpha_b = \frac{\alpha_w}{W/B}. \tag{9}$$

Proof: A module is a subarea of a block, hence (8) and (9) follow directly from parts 1) and 2) of Theorem 1.

Notice that unless $B = W$ (large-area clustering), there are areas on the wafer for which the distribution of the number of faults is *not* negative binomial. To be more specific, we state the following theorem.

Theorem 2: Let the number of faults in the wafer have a negative-binomial distribution with parameters (λ_w, α_w) and block size B, and let E be the size of an area divided among K blocks so that $E = \sum_{i=1}^{K} A_i$, where A_i is the size of the subarea contained in the ith block. The number of faults in area E has a negative-binomial distribution if and only if $A_1 = A_2 = \cdots = A_K = E/K$.

Proof: Similarly to the proof of Theorem 1, let $T_i(z)$ $(i = 1, \cdots, K)$ and $T_e(z)$ denote the generating functions of the number of faults in subarea A_i and in area E, respectively. Then,

$$\begin{aligned} T_e(z) &= \prod_{i=1}^{K} T_i(z) \\ &= \prod_{i=1}^{K} \left[\left(1 + \frac{\frac{A_i}{B}(1-z)\lambda_b}{\alpha_b} \right)^{-\alpha_b} \right] \\ &= \left[\prod_{i=1}^{K} \left(1 + \frac{\frac{A_i}{B}(1-z)\lambda_b}{\alpha_b} \right) \right]^{-\alpha_b}. \end{aligned}$$

The last expression is a generating function of a negative-binomial random variable if and only if $A_1 = A_2 = \cdots = A_K$. In this case, the parameters are $(\frac{E}{B}\lambda_b, K\alpha_b)$ or, equivalently, $(E\lambda_m, K\alpha_m)$.

Remarks:

1) Cases 1–3 of Theorem 1 are special cases of Theorem 2.

2) If $B = W$, then for any area E on the wafer $K = 1$ and the distribution of the number of faults in E is negative binomial.

We have so far found the block parameters and the module parameters given the wafer parameters and the block size B. In our model the chip parameters are not meaningful and are, therefore, not calculated. Since the chip area may be divided unequally among several adjacent blocks, then based on Theorem 2 the number of chip faults will not, in general, have a negative-binomial distribution. Instead, it will be the sum of several statistically independent negative-binomial random variables.

Our objective is to calculate the probability that exactly k out of the N chip modules are fault-free, based on the three parameters λ_w, α_w, and the block size B. Let the random variable G be the number of fault-free modules in the chip, then this probability can be denoted by $P_G(k)$. For a chip with $N - M$ redundant modules, the yield can be calculated by

$$Y(\text{chip}) = \sum_{k=M}^{N} P_G(k). \tag{10}$$

The equivalent yield (i.e., the expected fraction of operational modules) of partially good chips is

$$Y_{\text{EQ}} = \sum_{k=M}^{N} \frac{k}{N} P_G(k) \tag{11}$$

where M is the minimal number of modules that have to be fault-free for the chip to be usable. The calculations in the next section will be based on the module parameters (λ_m, α_m), but as can be seen from (8) and (9) they are a function of the wafer parameters (λ_w, α_w) and of the block size B.

III. Yield of Defect-Tolerant Chips

To avoid complex geometric considerations, we assume that both the chip and the block have rectangular shapes. The chip has dimensions (C_1, C_2) with $N = C_1 \cdot C_2$, while the block has dimensions (B_1, B_2) and $B = B_1 \cdot B_2$. We discuss a simple case first and the general case later.

A. A Simple Case

We first assume that B is a divisor of N and that every chip covers exactly N/B blocks. This includes the case $B \gg N$ (i.e., the large-area clustering case) that is equivalent to $B = N$. The following are three special cases:

(1) Small-Size Clustering: In this case $B = 1$, and all N modules are assumed to be statistically independent. $P_G(k)$ can, therefore, be calculated using the binomial probability as follows [3]

$$P_G(k) = \binom{N}{k} \left[\left(1 + \frac{\alpha_m}{\lambda_m} \right)^{-\alpha_m} \right]^k \cdot \left[1 - \left(1 + \frac{\alpha_m}{\lambda_m} \right)^{-\alpha_m} \right]^{N-k}. \tag{12}$$

(2) Large-Size Clustering: In this case $B = N$, which implies that the faults within the entire chip are uniformly distributed and that all sections of the chip are statistically dependent. The probability $P_G(k)$ for this case has been researched extensively and the equivalence of most of the proposed expressions has been proven in [2]. The probability $P_G(k)$ in this case is obtained by finding the probability of x faults occurring in a chip and then distributing them uniformly among the N modules in the chip. This results in

$$P_G(k) = a(k, N)$$

where the function a is defined by (see [2])

$$a(j, A) = \binom{A}{j} \sum_{l=0}^{A-j} (-1)^l \binom{A-j}{l} \left(1 + \frac{(j+l)\lambda_m}{\alpha_m} \right)^{-\alpha_m}. \tag{13}$$

(3) Medium-Size Clustering: i.e., $1 < B < N$.

To calculate $P_G(k)$ in case (3), we have to utilize an intermediate method, in which each block is considered in its entirety, and the different blocks are then combined relying on their statistical independence. This method includes (1) and (2) as two extreme special cases.

Let G_i, G be the random variables denoting the number of fault-free modules in the ith block and in the entire chip, respectively $(i = 1, \cdots, N/B)$. $G_1, \cdots, G_{N/B}$ are independent and identically distributed random variables and $G = \sum_{i=1}^{N/B} G_i$. For each block, the distribution of G_i can be obtained from (13), and the distribution of G can then be obtained by using either convolution or generating functions.

The generating-function technique is demonstrated in this subsection, while the convolution technique is used in the next subsection. Let $\Phi_{G_i}(z)$ and $\Phi_G(z)$ be the generating functions of G_i and G, respectively, then

$$\Phi_G(z) = (\Phi_{G_i}(z))^{N/B}. \tag{14}$$

Note that the generating functions $\Phi(z)$ are different from the generating functions $T(z)$ used in the previous section. The functions $T(z)$ characterize the number of *faults* in a given area, while the functions $\Phi(z)$ pertain to the number of *fault-free modules* in a given area.

The generating function $\Phi_{G_i}(z)$ is based on the probability function $P_{G_i}(k)$. Since G_i is the number of fault-free modules in one block, the "large-area clustering" equation must be used to calculate its probability function, i.e.,

$$P_{G_i}(k) = a(k, B)$$

(where $a(k, B)$ is defined in (13).)

Since all G_i's are identically distributed, the resulting generating function will not depend on i but on the block size B only.

$$\begin{aligned}\Phi_{G_i}(z) &= \sum_{k=0}^{B} P_{G_i}(k) \cdot z^k \\ &= \sum_{k=0}^{B} a(k, B) \cdot z^k \\ &= \sum_{k=0}^{B} \binom{B}{k} \sum_{l=0}^{B-k} (-1)^l \binom{B-k}{l} \\ &\quad \cdot \left(1 + \frac{(k+l)\lambda_m}{\alpha_m}\right)^{-\alpha_m} \cdot z^k.\end{aligned}$$

Using the identity

$$\binom{B}{k}\binom{B-k}{l} = \binom{k+l}{l}\binom{B}{k+l}$$

and substituting j for $k + l$ we obtain

$$\Phi_{G_i}(z) = \sum_{j=0}^{B} \sum_{l=0}^{B} (-1)^l \binom{j}{l} \binom{B}{j} \left(1 + \frac{j\lambda_m}{\alpha_m}\right)^{-\alpha_m} \cdot z^{j-l}.$$

Summing over l yields

$$\Phi_{G_i}(z) = \sum_{j=0}^{B} \binom{B}{j} (z-1)^j \left(1 + \frac{j\lambda_m}{\alpha_m}\right)^{-\alpha_m}. \tag{15}$$

The generating function of G (the number of fault-free modules in the entire chip), $\Phi_G(z)$, can now be obtained from (14). Note that for the special case $B = N$ (large-area clustering) we obtain

$$\Phi_G(z) = \Phi_{G_i}(z) = \sum_{j=0}^{N} \binom{N}{j} (z-1)^j \left(1 + \frac{j\lambda_m}{\alpha_m}\right)^{-\alpha_m} \tag{16}$$

while for $B = 1$ (small clusters)

$$\begin{aligned}\Phi_G(z) &= (\Phi_{G_i}(z))^N \\ &= \left(1 + (z-1)\left(1 + \frac{\lambda_m}{\alpha_m}\right)^{-\alpha_m}\right)^N.\end{aligned} \tag{17}$$

The generating function $\Phi_G(z)$ can be used for calculating the probabilities $P_G(k)$ by

$$P_G(k) = \frac{1}{k!} \frac{\partial^{(k)}}{\partial z^k} \Phi_G(z)/_{z=0}. \tag{18}$$

Differentiating (16) k times and substituting in (18) yields (13) for large-area clustering. Differentiating (17) k times and substituting in (18) results in (12) for small-area clustering.

For the special case $k = N$ (i.e., the chip is fault-free) we have

$$\frac{\partial^{(N)}}{\partial z^N} \Phi_G(z) = N! \left(1 + \frac{B\lambda_m}{\alpha_m}\right)^{-\alpha_m \frac{N}{B}} \tag{19}$$

which yields

$$P_G(N) = \left(1 + \frac{B\lambda_m}{\alpha_m}\right)^{-\alpha_m \frac{N}{B}}. \tag{20}$$

Substituting $B = N$ we obtain

$$P_G(N) = \left(1 + \frac{N\lambda_m}{\alpha_m}\right)^{-\alpha_m} \tag{21}$$

while for $B = 1$

$$P_G(N) = \left(1 + \frac{\lambda_m}{\alpha_m}\right)^{-N\alpha_m} \tag{22}$$

which again are the well-known probabilities of a fault-free chip for large-area clustering and for small-area clustering, respectively.

B. The General Case

In practice, the size of the chip is not necessarily an integer multiple of the block size, nor are the chip boundaries identical to the block boundaries. We need, therefore, to generalize our previous results to this more realistic situation. As before, we choose as the unit area the area of a module and as the basic parameters the module parameters λ_m and α_m. Consequently, the block parameters are $\lambda_b = B_1 \cdot B_2 \cdot \lambda_m$ and $\alpha_b = \alpha_m$.

Unless the block size is very large (comparable to the size of the wafer), the chip area will be divided into several subareas, each contained in a different block, and the number of fault-free modules in the entire chip is equal to the sum of the numbers of fault-free modules in each of the parts. Since these subareas are in different blocks, they are assumed to be statistically independent with respect to the number of faults. The distribution of the number of fault-free modules in each of these subareas can be obtained from (13), and the probability of k fault-free modules in the entire chip can be calculated using the convolution technique as detailed below. (The generating function method has been demonstrated in the previous subsection.)

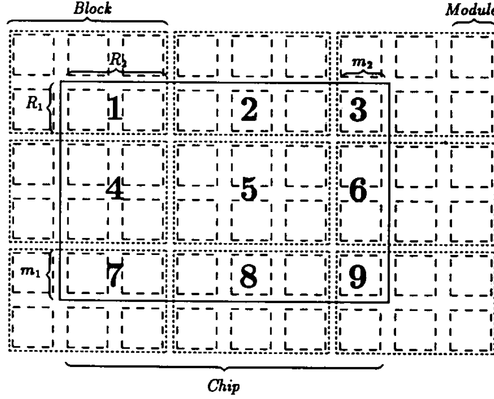

Fig. 1. A placement of a 4×6 chip relative to 2×3 blocks ($R_1 = 1$. $R_2 = 2$. $n_1 = n_2 = m_1 = m_2 = 1$).

There are $\min(B_1, C_1) \times \min(B_2, C_2)$ possible placements of the chip relative to the block (where min is the minimum function). Denote a placement by (R_1, R_2) where R_1 and R_2 are the vertical and horizontal distances, respectively, between the left top corner of the chip and the block boundaries, as depicted in Fig. 1. Clearly, $1 \leq R_1 \leq \min(B_1, C_1)$ and $1 \leq R_2 \leq \min(B_2, C_2)$. The placement (R_1, R_2) determines the way the chip is divided into complete and partial blocks. For given values of R_1 and R_2 denote

$$n_1 = \left\lceil \frac{C_1 - R_1}{B_1} \right\rceil; \qquad m_1 = (C_1 - R_1) \bmod B_1$$

$$n_2 = \left\lceil \frac{C_2 - R_2}{B_2} \right\rceil; \qquad m_2 = (C_2 - R_2) \bmod B_2.$$

Note that $C_1 = R_1 + n_1 \times B_1 + m_1$, $C_2 = R_2 + n_2 \times B_2 + m_2$, and that for $C_1 \leq B_1$, $n_1 = 0$ and $m_1 = C_1 - R_1$. Similarly, for $C_2 \leq B_2$, $n_2 = 0$ and $m_2 = C_2 - R_2$.

Once R_1 and R_2 are determined, the chip is divided into (at most) nine disjoint subareas in the following manner (see Fig. 1):

1) one partial block of size $R_1 \times R_2$.
2) n_2 partial blocks of size $R_1 \times B_2$.
3) one partial block of size $R_1 \times m_2$.
4) n_1 partial blocks of size $B_1 \times R_2$.
5) $n_1 \times n_2$ complete blocks of size $B_1 \times B_2$.
6) n_1 partial blocks of size $B_1 \times m_2$.
7) one partial block of size $m_1 \times R_2$.
8) n_2 partial blocks of size $m_1 \times B_2$.
9) one partial block of size $m_1 \times m_2$.

For $C_1 \leq B_1$ and $C_2 \leq B_2$, only four subareas, namely, areas 1, 3, 7, and 9, are nonempty.

To calculate the yield of a chip with redundancy, we need to find the probabilities $P_G(k)$, where G denotes the number of fault-free modules in a chip. These probabilities are first calculated for a given placement (R_1, R_2) and then averaged over all possible placements.

Denoting by G_i the number of fault-free modules in subarea i, $(i = 1, \cdots, 9)$, we have

$$G = \sum_{i=1}^{9} G_i .$$

Since the G_i's are statistically independent, the probability function of G is the convolution of the probability functions of $G_1, \cdots, G_9$, namely

$$P^{(R_1,R_2)}(G = k) = \sum_{k_1 + \cdots + k_9 = k} P(G_1 = k_1) P(G_2 = k_2) \cdots P(G_9 = k_9). \tag{23}$$

The superscript (R_1, R_2) indicates the dependence of the probabilities on the placement. For simplicity, it is omitted in the notation $P(G_i = k_i)$, although these probabilities clearly depend on (R_1, R_2).

To calculate the probability functions of G_i (for given (R_1, R_2)), we need to distinguish between $i = 1, 3, 7, 9$ and $i = 2, 4, 5, 6, 8$. For $i = 1, 3, 7, 9$ the subarea is contained in one block, and

$$P(G_i = k_i) = a(k_i, A_i) \tag{24}$$

where $a(k, A)$ is defined in (13) and A_i is the number of modules in subarea i, namely

$$A_1 = R_1 R_2, \quad A_3 = R_1 m_2, \quad A_7 = R_2 m_1, \quad A_9 = m_1 m_2 .$$

For $i = 2, 4, 5, 6, 8$, subarea i is itself divided into several parts, each contained in a different block. These parts have equal dimensions and are statistically independent. Denote by s_i the number of those parts, by A_i the number of modules in each of them and by k_{ij} the number of fault-free modules in part j of subarea i ($j = 1, \cdots, s_i$, $i = 2, 4, 5, 6, 8$), then

$$P(G_i = k_i) = \sum_{k_{i1} + k_{i2} + \cdots + k_{is_i} = k_i} a(k_{i1}, A_i) a(k_{i2}, A_i) \cdots a(k_{is_i}, A_i) \tag{25}$$

where $s_2 = n_2$, $A_2 = R_1 B_2$, $s_4 = n_1$, $A_4 = B_1 R_2$, $s_5 = n_1 n_2$, $A_5 = B_1 B_2$, $s_6 = n_1$, $A_6 = B_1 m_2$, $s_8 = n_2$, and $A_8 = B_2 m_1$.

Equations (24) and (25) are now substituted into (23), and (23) is averaged over all possible placements (R_1, R_2)

$$P_G(k) = \frac{1}{\min(B_1, C_1) \times \min(B_2, C_2)} \cdot \sum_{R_1=1}^{\min(B_1,C_1)} \sum_{R_2=1}^{\min(B_2,C_2)} P^{(R_1,R_2)}(G = k). \tag{26}$$

Finally, the yield of the chip is

$$Y(\text{chip}) = \sum_{k=M}^{N} P_G(k). \tag{27}$$

In the above analysis the probabilities $P(G_i = k_i)$ were calculated for subareas that include modules only. If the chip

includes some support circuitry as well, then the expression $P(G_i = k_i)$ for one or more subareas will have to be replaced by $P(G_i = k_i \cap \text{support circuitry is fault-free})$. As a result, the overall yield of the chip will depend upon the exact placement of the support circuitry within the chip layout.

IV. Estimating the Block Size

The correct estimation of all the model parameters, namely (λ_m, α_m), and the block size is essential for proper evaluation of the yield of circuits with redundancy. The parameters λ_m and α_m can be estimated using standard estimation techniques such as the moment method, the maximum likelihood method, or curve fitting.

Given S wafers with W modules each, let X_i denote the number of faults in module i $(i = 1, \cdots, S \cdot W)$ and $\overline{X}$ the average of the X_i's, then,

$$\widehat{\lambda_m} = \overline{X} = \frac{1}{S \cdot W} \sum_{i=1}^{S \cdot W} X_i \tag{28}$$

where $\widehat{\lambda_m}$ denotes the estimator of the parameter λ_m.

To obtain a moment-method estimator for α_m, note that when X has a negative-binomial distribution with (λ_m, α_m), then its variance $V(X)$ is

$$V(X) = \lambda_m \left(1 + \frac{\lambda_m}{\alpha_m}\right). \tag{29}$$

The estimator for the variance is

$$\widehat{V(X)} = \frac{1}{S \cdot W} \sum_{i=1}^{S \cdot W} {X_i}^2 - \overline{X}^2. \tag{30}$$

Equating (29) and (30) and substituting $\overline{X}$ for λ_m yields the following estimator for α_m

$$\widehat{\alpha_m} = \frac{\overline{X}^2}{\widehat{V(X)} - \overline{X}}. \tag{31}$$

A different estimator for α_m is obtained by "curve fitting" [2]. Denote by Y_m the fraction of fault-free modules out of the $S \cdot W$ modules, then $\widehat{\alpha_m}$ is the solution of the equation

$$Y_m = \left(1 + \frac{\widehat{\lambda_m}}{\widehat{\alpha_m}}\right)^{-\widehat{\alpha_m}}. \tag{32}$$

The maximum likelihood estimator of α_m can be found in [9].

The problem of determining the block size based on empirical data is not a classical statistical problem. Simple estimation based on averaging the sizes of actual clusters is very difficult since, given a fault map, it is not always clear what the boundaries of the clusters are. Moreover, even if the average cluster size can be estimated, its relation to the block size is not clear at this point. We, therefore, suggest two nonstandard methods of estimating the block size, both based on a procedure called "the quadrat method" or "the window method" [2].

Assuming, as we did before, that the block is rectangular, its size can be described by a tuple (B_1, B_2). The wafer is divided into rectangular subareas (windows or quadrats) that are increased at every step. Given S wafers with W modules each, start with windows of size $I = 1, J = 1$ and then alternately increase I and J by 1 until the appropriate value of the block size is reached. For each fixed value of (I, J) divide all the given wafers into windows of size $I \times J$ (thus having $U = (S \cdot W)/(I \cdot J)$ windows), and then count the number of faults in each window denoting by X_i the number of faults in window i, $(i = 1, \cdots, U)$.

The first method utilizes the fact (proven in Section II) that the parameter α remains constant within a block and increases when the area consists of several blocks. In this method, $\alpha(I, J)$ is estimated for every potential block size (I, J), and the values of $\widehat{\alpha}(I, J)$ are arranged in matrix form. We then search for the largest (I, J) for which $\widehat{\alpha}(I, J)$ is still close to $\widehat{\alpha}(1, 1)$, and this (I, J) is used as an estimate of (B_1, B_2).

The second method is based on the assumption that the different blocks are statistically independent with respect to the number of faults. The block size in this method is determined in two steps, first B_1 and then B_2. For every potential block size (I, J), each wafer is divided into windows of size (I, J). To determine the value of B_1, a chi-square statistic is calculated for every (I, J) to test independence between every two vertically neighboring blocks. The resulting values are then arranged in matrix form. The index I of the first row for which the chi-square values are significantly lower than those of the other rows is chosen as B_1. Similarly, B_2 is determined by testing for independence between horizontally neighboring blocks and by choosing the index J of the first column whose values are significantly low. The two methods for estimating (B_1, B_2) are demonstrated in the next section.

V. Model Validation and Numerical Results

We first validate the newly proposed yield formulas by using simulated wafers, then demonstrate the effect of the block size on the yield and on the optimal amount of redundancy to be incorporated in a chip, and finally test the block model on empirical data obtained from 12 particle maps of wafers manufactured by IBM [10].

As a first step, fault maps of 10 000 wafers, each of size 24×24 modules, were simulated. The goal of the simulation was to validate the techniques suggested for estimating the block size as well as the proposed yield equations. The parameters used were $\lambda_b = 0.1$, $\alpha_b = 0.25$, and a block size of 2×3 modules. The faults were simulated as follows: a number of faults x were generated according to the negative-binomial distribution with parameters (0.1,0.25) for each of the 960 000 blocks and then uniformly distributed among the six modules in the block.

The parameters λ_b, α_b, B_1, and B_2 were then estimated based on the simulated wafers. The estimate obtained for λ_b was $\widehat{\lambda_b} = 0.1007$. The matrix of the α estimates for block sizes between (1×1) and (8×8) is given in Table I. The two chi-square tests (one for rows and one for columns) have been performed for the same block sizes, and the resulting chi-square statistics are presented in Tables II and III. The block size (B_1, B_2) can be found either from the α matrix or from

TABLE I
THE α MATRIX FOR THE SIMULATED WAFERS

0.28	0.33	0.26	0.46	0.50	0.50	0.67	0.75
0.27	0.32	0.26	0.46	0.51	0.50	0.68	0.76
0.48	0.56	0.48	0.83	0.96	0.93	1.28	1.44
0.50	0.60	0.50	0.89	1.03	0.98	1.37	1.53
0.68	0.85	0.70	1.27	1.46	1.41	1.94	2.19
0.72	0.90	0.73	1.34	1.54	1.48	2.06	2.32
0.93	1.16	0.95	1.72	1.98	1.91	2.65	2.97
0.98	1.21	0.98	1.79	2.06	1.98	2.75	3.02

TABLE II
THE CHI-SQUARE MATRIX FOR THE ROWS OF THE SIMULATED DEFECT MAPS

229683.34	203881.48	245000.22	136178.55	96182.90	115760.10	71963.05	71715.63
0.28	10.27	1.15	3.07	3.10	5.14	3.21	7.33
8050.98	7101.01	8798.31	4260.57	2917.43	3280.47	1825.31	1715.88
1.88	10.22	5.87	1.94	2.66	2.67	1.81	6.53
1234.57	1049.30	1191.06	550.32	302.30	347.95	158.85	171.62
4.44	10.70	0.71	0.78	2.76	1.14	0.43	5.22
300.75	289.79	278.46	111.66	73.70	72.53	40.11	25.26
5.97	10.63	4.01	0.45	1.03	2.63	5.61	3.56

TABLE III
THE CHI-SQUARE MATRIX FOR THE COLUMNS OF THE SIMULATED DEFECT MAPS

100686.63	36679.00	0.07	4294.11	993.03	2.85	933.73	697.99
113273.83	35649.67	0.56	4179.13	938.29	1.41	865.55	620.23
58799.13	18425.02	1.43	1926.59	416.69	0.68	354.57	262.97
54168.29	16258.17	3.63	1691.40	359.87	1.06	244.62	150.38
30668.13	8739.49	1.22	836.14	181.54	2.22	99.11	66.78
34574.99	9604.63	0.65	880.34	125.98	3.37	84.79	55.49
22257.25	5940.09	2.30	544.87	104.04	5.95	70.72	32.58
24383.17	6195.51	3.18	518.31	78.54	2.67	40.53	23.38

the chi-square matrices. Observing the α matrix (Table I), it is easily seen that the value 0.26 in the $(2,3)$ position is the farthest entry close to 0.28 (the element in the (1,1) position). We therefore deduce that the block size is (2×3). The same conclusion is reached by observing the chi-square matrices. In the rows chi-square matrix (Table II), line 2 is the first to have very small entries (and so does every row whose index is a multiple of 2). In the columns chi-square matrix (Table III), column 3 is the first with significantly low values (so is column 6, since 6 is a multiple of 3). The block size is, therefore, estimated as $(2,3)$.

The estimated parameters were then used for yield calculations. A chip size of 4×6 modules was selected, and the yield of this chip with d of its modules as spares was calculated in four different ways. This yield is the cumulative probability of d or less faulty modules, or the probability of $N - d$ or more fault-free modules, denoted by $P(G \geq N - d)$ in the previous section. First, we found the actual proportion of simulated chips with d or less faulty modules ($d = 0, \cdots, 24$). The theoretical probability was then calculated based on three different yield models: the large-area clustering model (13), the small-area clustering model (12), and the equations obtained from the block model. The results are depicted in Fig. 2. As expected, the block model provides the best fit in this case. In addition, we can see that for $d \geq 2$, the large-area clustering model underestimates the yield, while the small-area clustering model overestimates it. For very small values of d, three of the graphs almost coincide but the small-area clustering model underestimates the yield.

We then analyzed the effect of varying the block size on the yield and on the optimal redundancy. We selected a wafer of size 24×24 modules and a chip of size 3×3 modules, with

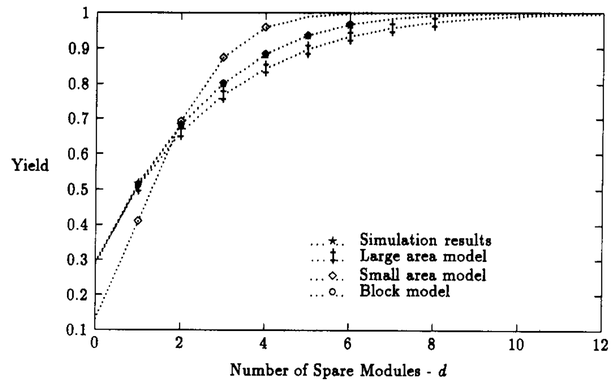

Fig. 2. Comparing three theoretical yield models to simulation results.

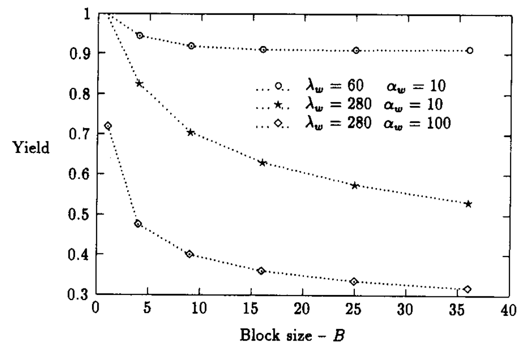

Fig. 3. Yield as a function of block size.

two spare modules (the chip requires at least seven modules for proper operation). We fixed the values of the parameters (λ_w, α_w) and calculated the yield of the chip as a function of the block size B. Fig. 3 shows the dependency of the yield on the block size for three sets of the parameters (λ_w, α_w). As can be seen, in all three cases the yield decreases as the block size increases. A possible explanation to this phenomenon is that for a larger block size, the fault clusters tend to be larger making it more likely to have more than two faulty modules per chip. We can also conclude that for certain combinations of (λ_w, α_w) the projected yield is considerably lower for high values of B (approaching large-area clustering) than for small values of B.

We next investigated the effect of B (and that of the other two parameters) on the optimal redundancy to be incorporated in a chip. We chose a wafer of size 24×24 and a basic chip of size 2×3 modules. We then added several spare modules and calculated the equivalent yield (i.e., the yield divided by the ratio between the area of the chip with redundancy and its area without redundancy). Fig. 4 depicts the equivalent yield as a function of the number of spare modules for several sets of parameters. The optimal redundancy for a given set of parameters is the number of spares for which the equivalent yield achieves its maximum. The optimal amount of redundancy clearly depends on all three parameters λ_w, α_w, and B. To isolate the effect of each of the parameters, we fixed

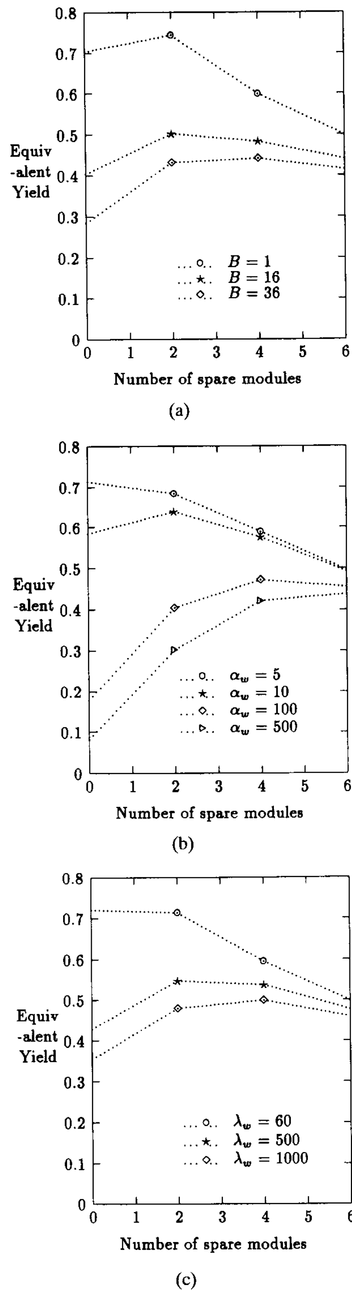

Fig. 4. The equivalent yield as a function of the amount of redundancy. (a) $\lambda_w = 280$ and $\alpha_w = 10$. (b) $\lambda_w = 280$ and $B = 4$. (c) $\alpha_w = 15$ and $B = 4$.

two out of the three and let the third vary. As can be seen from Fig. 4(a)–(c), the optimal redundancy is nondecreasing in each of the parameters λ_w, α_w and B.

As a last step for validating the proposed yield equations, we analyzed 12 particle maps of wafers manufactured by IBM [10], each consisting of 24×24 modules. We first estimated λ and obtained $\widehat{\lambda} = 0.1089$. We then estimated α for every

TABLE IV

THE α MATRIX FOR THE TWELVE DEFECT MAPS

1.10	0.56	0.52	0.40	0.91	0.49	0.57	0.48	0.72	0.74	0.56	0.48
0.53	0.44	0.44	0.35	0.61	0.46	0.55	0.47	0.66	0.67	0.59	0.48
0.48	0.44	0.44	0.36	0.56	0.46	0.48	0.43	0.60	0.60	0.54	0.45
0.41	0.42	0.42	0.36	0.54	0.49	0.52	0.43	0.62	0.65	0.59	0.49
0.38	0.39	0.38	0.33	0.44	0.43	0.48	0.39	0.64	0.57	0.49	0.45
0.46	0.45	0.47	0.42	0.64	0.53	0.57	0.51	0.70	0.69	0.62	0.53
0.46	0.48	0.48	0.38	0.57	0.53	0.58	0.47	0.79	0.73	0.65	0.54
0.44	0.47	0.48	0.43	0.65	0.55	0.58	0.50	0.72	0.80	0.70	0.58
0.43	0.43	0.44	0.37	0.53	0.45	0.49	0.46	0.68	0.64	0.55	0.49
0.45	0.47	0.49	0.41	0.54	0.51	0.56	0.44	0.71	0.68	0.58	0.56
0.48	0.51	0.51	0.42	0.62	0.53	0.61	0.47	0.77	0.72	0.62	0.60
0.52	0.51	0.52	0.45	0.72	0.59	0.62	0.51	0.83	0.91	0.87	0.72

TABLE V

THE CHI-SQUARE MATRIX FOR THE ROWS OF THE DEFECT MAPS

347.86	393.96	317.19	271.23	181.67	206.04	126.49	138.21	86.28	89.99	108.44	124.8
359.84	225.44	177.73	143.39	96.48	112.24	84.16	92.02	59.58	53.39	58.25	54.18
171.28	136.12	108.27	82.38	49.94	72.63	36.31	45.43	31.22	28.56	34.22	33.35
142.00	95.66	72.70	53.55	30.72	41.25	26.25	31.16	22.00	20.61	18.33	19.86
63.86	56.39	32.61	28.52	16.01	18.75	14.95	21.06	10.09	7.94	10.49	9.80
92.98	67.18	44.02	45.46	23.85	28.68	21.04	29.27	10.00	5.69	8.23	7.98
31.13	18.91	12.05	8.30	4.96	11.48	10.61	11.52	4.87	4.42	4.35	4.83
32.15	12.70	6.87	8.58	2.55	4.29	4.63	6.09	1.88	4.13	4.53	1.43
21.74	7.86	7.90	4.55	0.52	13.13	6.60	3.24	3.78	4.56	7.00	5.37
20.20	11.42	7.73	6.05	3.37	5.67	16.38	2.56	0.96	24.77	11.22	5.35
25.77	13.75	10.49	7.73	3.27	11.46	7.70	3.67	0.96	10.62	10.89	5.67
37.03	10.59	10.40	9.80	5.48	12.95	7.20	6.57	0.49	10.24	3.14	7.53

TABLE VI

THE CHI-SQUARE MATRIX FOR THE COLUMNS OF THE DEFECT MAPS

682.08	448.34	209.07	100.24	123.47	137.51	41.95	67.89	47.57	48.19	36.93	35.79
449.74	359.78	129.08	52.37	57.48	87.67	32.70	31.36	24.53	30.38	24.94	15.34
276.16	262.93	106.83	50.36	45.50	70.77	18.72	20.26	20.94	25.59	21.05	17.06
202.53	220.85	78.51	40.58	33.66	54.05	16.97	14.12	17.63	22.21	17.38	13.58
168.06	170.58	67.68	36.02	24.14	51.42	19.39	18.95	25.86	20.97	15.70	13.47
184.45	143.17	70.18	33.07	28.80	40.49	12.16	11.12	14.60	14.01	12.83	7.98
141.92	149.14	56.52	21.81	19.59	30.76	10.89	13.60	15.47	15.24	12.48	7.29
126.23	125.89	35.34	23.05	22.66	29.23	14.54	13.19	18.83	16.85	13.93	9.43
123.96	85.27	37.17	18.22	17.61	20.58	7.09	9.58	15.87	15.87	15.01	12.15
95.49	82.81	32.48	22.22	22.48	19.18	10.14	9.29	16.66	16.72	11.99	12.17
99.84	97.34	43.10	19.97	10.56	16.31	6.69	8.61	13.13	11.63	7.74	7.16
104.05	80.36	32.66	20.99	7.20	14.89	3.73	5.27	2.69	5.19	7.53	3.14

possible block size between (1×1) and (12×12), and the results are presented in Table IV. (Block sizes larger than (12×12) have not been considered.) The chi-square tests for independence were then performed, and the resulting statistics appear in Tables V and VI. The determination of the block size based on Tables IV–VI is not as straightforward here as it was in the case of the simulated wafers. The empirical data include only 12 wafers, which is a very small number for statistical purposes. We, therefore, have to combine both methods of the block-size estimation and consider all three tables simultaneously. By combining the information in Tables IV–VI we estimated the block size (B_1, B_2) to be (10×8).

Finally, we compared the empirical and theoretical yield of a chip of size (10×11) modules. The yield of this chip (as a function of the number of spare modules, denoted by d) was calculated based on both the large-area clustering model and the block model with a (10×8) block. The results were then compared to the empirical proportion of chips with d or less faulty modules in the actual wafer maps and are depicted in Fig. 5. As can be seen, the large-area clustering model is more accurate for very small values of d. For $d \geq 2$, however, the block model with a (10×8) block provides a much better fit to the empirical results.

To determine the sensitivity of the yield estimation to the exact choice of the block size, three other block sizes have

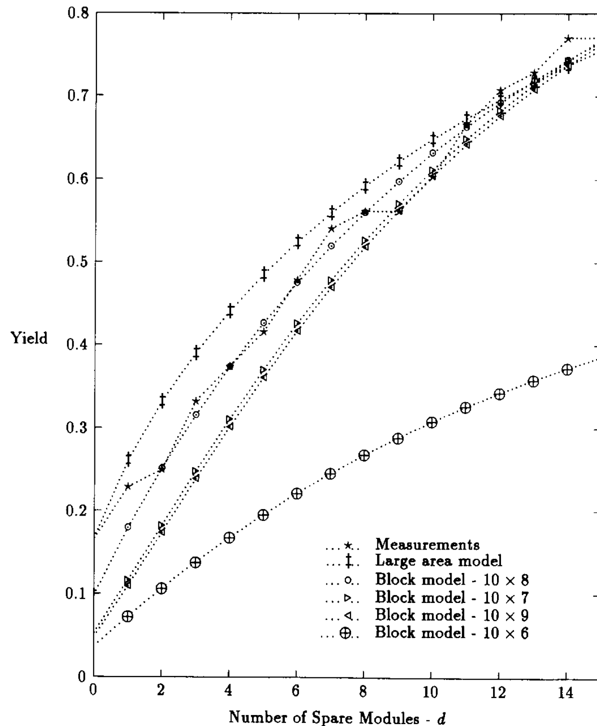

Fig. 5. Comparing the block model (with four different sizes of the block) and the large-area clustering model to the measurements for a 10 × 11 chip.

been chosen: (10×7), (10×9), and (10×6), and the estimated yield of a (10×11) chip was calculated for each one of them. The results appear in Fig. 5, and they demonstrate that if the deviation from the "correct" block size is small, so is the deviation of the predicted yield from the empirical results. This deviation increases as the error in estimating the appropriate block size increases.

VI. Conclusions

A unified negative-binomial distribution for yield analysis of fault-tolerant circuits has been presented in this paper. By adding a new parameter, namely, the block size, to the two existing parameters of the negative-binomial distribution, we have unified the yield analysis for large-area clustering, small-area clustering and medium-area clustering. We have demonstrated through several numerical examples the effect of the block size on the projected yield and consequently, on the optimal amount of redundancy. We have proposed methods for estimating the block-size parameter of the fault distribution and demonstrated (through simulation and empirical data) that in certain situations the more general model provides a more accurate yield projection compared to the previously suggested models. Additional analysis of empirical data needs to be performed to gain better understanding of the circumstances under which the more general model has to be employed.

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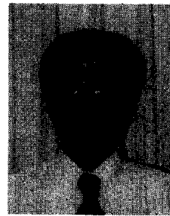

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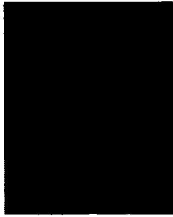

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