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THE IMPACT OF FLOORPLANNING ON THE YIELD OF FAULT-TOLERANT ICs[1]

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Abstract

Until now, VLSI designers rarely considered yield issues when selecting a floorplan for a newly designed chip. This paper demonstrates that for large area VLSI chips, especially those that incorporate some fault tolerance, changes in the floorplan can affect the projected yield. We study several general floorplan structures, make some specific recommendations, and apply them to actual VLSI chips.

1. Introduction

When designing a new chip, yield issues rarely affect the choice of the floorplan. This is justified when the chip is relatively small and the defect distribution can be accurately described by either the Poisson or the compound Poisson yield models ([1]). In particular, in the most commonly used compound Poisson model, i.e., the negative binomial (NB) distribution with large area clustering [2], the "size" of the defect clusters is assumed to be much larger than the size of the chip and selecting a different floorplan will not affect the projected yield of the designed chip.

Recent studies of defect maps of very large area VLSI ICs [3] have shown that the large area clustering NB distribution does not provide a sufficiently accurate yield model for such ICs. The newly proposed medium size clustering model [4] provides a much better match to empirical data [3]. Our objective is to study the possible impact that the floorplan of a large area chip (with or without redundancy) would have on the yield of the chip, under the new medium area clustering NB yield model.

In [5] we performed a preliminary study using two actual test cases, namely, DEC's Alpha chip [6] and Hitachi's SLSI (System integrated LSI) chip [7]. Our conclusion was that the floorplan of a chip can affect the projected yield of the chip in a non-negligible way. In this paper we perform a more detailed study of the relationship between floorplanning and yield. We analyze several general problems and propose theoretical solutions for them. We then make some practical recommendations and illustrate them through two actual test cases.

2. The Yield Model

We distinguish in our analysis between manufacturing defects and logical faults. Defects are the result of unwanted chemical and airborne particles deposited during the manufacturing process while faults are actual circuit failures such as line breaks and short circuits. Only a fraction of the defects cause circuit faults, with the precise number depending on the layout and density of the circuit.

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It is well known that manufacturing defects tend to cluster on the wafer, and are, therefore, better matched by a Negative Binomial (NB) distribution than by a Poisson distribution [2]. The same applies to logical faults, since they constitute a fraction of all defects. The negative binomial distribution has two parameters, λ and α. When it is used to model the spatial distribution of faults in an area of size A, both of the parameters depend on A, and

$$Prob\ (x\ faults\ in\ area\ A) = \frac{\Gamma(\alpha_A + x)}{x!\ \Gamma(\alpha_A)} \frac{\left(\frac{\lambda_A}{\alpha_A}\right)^x}{\left(1 + \frac{\lambda_A}{\alpha_A}\right)^{\alpha_A + x}} \tag{1}$$

In particular, (1) enables calculating the probability of zero faults in area A which, if no redundancy exists, constitutes the yield of this area

$$Yield = Prob\ (0\ faults\ in\ area\ A) = (1 + \lambda_A/\alpha_A)^{-\alpha_A} \tag{2}$$

The parameter λ_A denotes the expected number of faults in area A, satisfying $\lambda_A = \lambda A$, where λ is the expected number of faults per unit area. α_A is the clustering parameter for the considered area, measuring the deviation from the Poisson distribution. The smaller its value, the larger the deviation. α_A is a non-decreasing function of A, but the exact dependence of α_A on A is not uniquely defined and depends on the clustering pattern within the area. Most of the literature dealing with yield issues assumes large area clustering, i.e., large defect clusters comparable in size to the chip or even the wafer size. As has been demonstrated in [3], the empirical defect distribution (and consequently, the fault distribution) of large area chips has a better fit to a medium area clustering than to a large area clustering NB distribution. A detailed description of the medium area NB distribution, including several suggested ways of estimating the block size, appears in [4], and is briefly explained below.

Under the medium area NB model, we view the defect clustering as an empirical phenomenon which is the result of the wafer area being divided into sub-areas which we call *blocks*, such that the defects in distinct blocks are statistically independent. The number of defects in each block has a NB distribution, with a uniform distribution within the area of the block. The large area NB distribution is a special case with the whole wafer constituting one block.

As mentioned before, only a fraction of the defects turn into actual faults, and different circuits on the same chip may have different fault densities. Consider an area of size $A_1 + A_2$, where A_1 and A_2 have an expected number of faults λ_1 and λ_2, respectively. If A_1 and A_2 are located in the same block, then

$$P(no\ faults\ in\ an\ area\ of\ size\ A_1 + A_2) = \left(1 + \frac{\lambda_1 + \lambda_2}{\alpha}\right)^{-\alpha} \tag{3}$$

while if they are located in different blocks, then

$$P(no\ faults\ in\ an\ area\ of\ size\ A_1 + A_2) = \left(1 + \frac{\lambda_1}{\alpha}\right)^{-\alpha} \left(1 + \frac{\lambda_2}{\alpha}\right)^{-\alpha} \tag{4}$$

The two expressions have different numerical values, which indicates that different floorplans, i.e., different placements of the same logic modules, could result in different yields. This claim is further demonstrated in the next two sections.

3. Simple Test Cases

We demonstrate the possible effect of the floorplan on the yield by comparing the projected yields of different floorplans for several hypothetical chip layouts.

3.1 Example 1

In the first example, depicted in Figure 1, the chip consists of four equal-area modules (functional units), N_1, N_2, N_3 and N_4. The chip has no incorporated redundancy, and all four modules are necessary for the proper operation of the chip.

(*a*) (*b*)

Figure 1: Two floorplans for Example 1.

We assume the medium size NB distribution for the spatial distribution of the manufacturing defects. Suppose that N_1, N_2, N_3 and N_4 have different sensitivities to defects, resulting in different fault densities. Let λ_i be the fault density of N_i, and assume $\lambda_1 \leq \lambda_2 \leq \lambda_3 \leq \lambda_4$. This chip has 4!=24 possible floorplans, denoted by $(N_{i_1}, N_{i_2}, N_{i_3}, N_{i_4})$ where (i_1, i_2, i_3, i_4) is some permutation of $(1, 2, 3, 4)$. If small area clustering (clusters smaller than or comparable to the size of a module) or large area clustering (clusters larger than or equal to the chip area) are assumed, the projected yields of all possible floorplans will be the same. This is not the case, however, when medium area clustering (i.e., blocks of size 2 or 3 modules) is assumed.

Assuming blocks of size 2, the yield of floorplan $(N_{i_1}, N_{i_2}, N_{i_3}, N_{i_4})$ is

$$Yield(i_1, i_2, i_3, i_4) = \frac{1}{2}\left[\left(1 + \frac{\lambda_{i_1} + \lambda_{i_2}}{\alpha}\right)^{-\alpha}\left(1 + \frac{\lambda_{i_3} + \lambda_{i_4}}{\alpha}\right)^{-\alpha} + \left(1 + \frac{\lambda_{i_1}}{\alpha}\right)^{-\alpha}\left(1 + \frac{\lambda_{i_2} + \lambda_{i_3}}{\alpha}\right)^{-\alpha}\left(1 + \frac{\lambda_{i_4}}{\alpha}\right)^{-\alpha}\right] \tag{5}$$

It is clear from Equation (5) that different permutations will result in different yields. The best permutation can be found by exchanging modules whenever this exchange increases the yield. It can be shown algebraically that exchanging i_1 and i_2 will increase the yield if and only if $\lambda_{i_1} > \lambda_{i_2}$. Similarly, exchanging i_3 and i_4 will increase the yield if and only if $\lambda_{i_4} > \lambda_{i_3}$. Exchanging i_2 and i_3 will increase the yield if and only if $\lambda_{i_1} > \lambda_{i_4}$ and $\lambda_{i_2} < \lambda_{i_3}$, or $\lambda_{i_1} < \lambda_{i_4}$ and $\lambda_{i_2} > \lambda_{i_3}$. Exchanging i_2 and i_4 will increase the yield if and only if $\lambda_{i_2} > \lambda_{i_4}$, and similarly, exchanging i_1 and i_3 will increase the yield if and only if $\lambda_{i_1} > \lambda_{i_3}$. Taking into account all of the above inequalities, we conclude that the best permutation of the modules (under the condition $\lambda_1 \leq \lambda_2 \leq \lambda_3 \leq \lambda_4$) is (N_1, N_3, N_4, N_2), which is shown in Figure 1(b). The permutation (N_2, N_4, N_3, N_1) has the same yield.

If the block size is assumed to be 3 modules, the projected yield for the floorplan $(N_{i_1}, N_{i_2}, N_{i_3}, N_{i_4})$ is

$$Yield(i_1, i_2, i_3, i_4) = \frac{1}{3}\left[\left(1 + \frac{\lambda_{i_1}}{\alpha}\right)^{-\alpha}\left(1 + \frac{\lambda_{i_2} + \lambda_{i_3} + \lambda_{i_4}}{\alpha}\right)^{-\alpha}\right. \tag{6}$$

$$+\left(1+\frac{\lambda_{i_1}+\lambda_{i_2}}{\alpha}\right)^{-\alpha}\left(1+\frac{\lambda_{i_3}+\lambda_{i_4}}{\alpha}\right)^{-\alpha}+\left(1+\frac{\lambda_{i_1}+\lambda_{i_2}+\lambda_{i_3}}{\alpha}\right)^{-\alpha}\left(1+\frac{\lambda_{i_4}}{\alpha}\right)^{-\alpha}\Bigg]$$

The rules for selecting the best permutation happen to be the exact same rules as for a block of size 2. Our conclusion is that the floorplan (N_1, N_3, N_4, N_2) shown in Figure 1(b) results in the highest yield, for any block size.

3.2 A generalization of Example 1

The above conclusion can be generalized to a chip consisting of k modules $N_1, ..., N_k$ with different fault densities $\lambda_1 \leq \lambda_2 \leq \cdots \leq \lambda_k$. The possible floorplans can be represented by the permutations $(N_{i_1}, N_{i_2}, ..., N_{i_k})$. It can be shown, similarly to Example 1, that for any block size, the floorplan resulting in the highest yield is

$$(\ N_1, N_3, N_5, \cdots, N_k, \cdots, N_6, N_4, N_2\ )$$

shown in Figure 2. The general conclusion that we can draw based on Example 1 is that

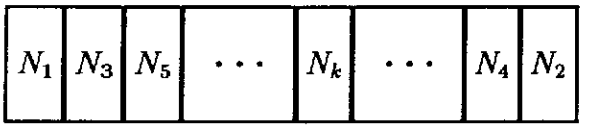

Figure 2: A floorplan with k modules.

the relative position (in a floorplan) of modules with no redundancy (i.e, all faults are chip-kill faults [2]) but with different fault densities may have a significant impact on the yield. This has been demonstrated in [5] through Hitachi's SLSI chip [7] for which the position of the 18K gate array relative to the six $64Kb$ SRAM units affected the yield. Our specific recommendation is to place the most sensitive modules in the center of the chip and the least sensitive modules in the boundaries. We illustrate this rule in Section 4 through another practical test case, namely, DEC's ECL RISC microprocessor ([8]).

3.3 Example 2

In the second hypothetical case, the chip consists of three circuits, S_1, S_2 and N. For proper operation, N, and either S_1 or S_2 have to be fault-free. The two possible floorplans for the chip are depicted in Figure 3. The difference between the two is that

Floorplan a Floorplan b

Figure 3: Two alternative floorplans for Example 2.

in floorplan (a), the module S_1 and its spare are placed next to each other, while in floorplan (b) they are separated by N. Clearly, there is no difference in the yield of the two floorplans if a block size of one module or three modules is assumed.

Let the number of defects have a NB distribution with a block size of two modules, and suppose that S_i and N have a fault density of λ_s and λ_n, respectively. The yields of

the two layouts will be

$$Yield(a) = \frac{1}{2} \cdot \left[\left(1+\frac{\lambda_n}{\alpha}\right)^{-\alpha} \left(2\left(1+\frac{\lambda_s}{\alpha}\right)^{-\alpha} - \left(1+\frac{2\lambda_s}{\alpha}\right)^{-\alpha}\right) \right. \tag{7}$$
$$\left. + \left(1+\frac{\lambda_s}{\alpha}\right)^{-\alpha}\left(1+\frac{\lambda_n}{\alpha}\right)^{-\alpha} + \left(1+\frac{\lambda_s+\lambda_n}{\alpha}\right)^{-\alpha} - \left(1+\frac{\lambda_s}{\alpha}\right)^{-\alpha}\left(1+\frac{\lambda_s+\lambda_n}{\alpha}\right)^{-\alpha}\right]$$

$$Yield(b) = \left(1+\frac{\lambda_s}{\alpha}\right)^{-\alpha}\left(1+\frac{\lambda_n}{\alpha}\right)^{-\alpha} + \left(1+\frac{\lambda_s+\lambda_n}{\alpha}\right)^{-\alpha} - \left(1+\frac{\lambda_s}{\alpha}\right)^{-\alpha}\left(1+\frac{\lambda_s+\lambda_n}{\alpha}\right)^{-\alpha} \tag{8}$$

It can be proven algebraically that for any λ_s and λ_n, $Yield(b) \geq Yield(a)$, with a strict inequality for $\lambda_s \neq \lambda_n$. The practical implication is that the circuit and its spare should be separated rather than being placed adjacent to each other.

3.4 Example 3

The third simplified example is that of a chip consisting of four modules, S_1, S_2, T_1 and T_2. For proper operation, one of S_1 and S_2, and one of T_1 and T_2 have to be

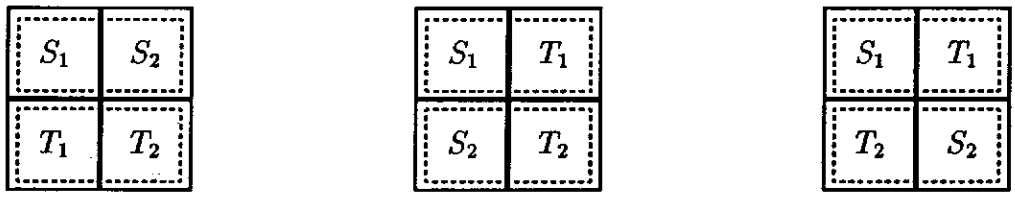

Figure 4: Three alternative floorplans for Example 3.

fault-free. The three possible floorplans for this chip are depicted in Figure 4. As before, let the number of faults have a NB distribution with densities λ_s and λ_t for S_i and T_i, respectively, and suppose that the chip consists of two horizontal blocks of two modules each (as shown in dashed lines in Figure 4), the yields of the three floorplans are

$$Yield(a) = \left[2\left(1+\frac{\lambda_s}{\alpha}\right)^{-\alpha} - \left(1+\frac{2\lambda_s}{\alpha}\right)^{-\alpha}\right]\left[2\left(1+\frac{\lambda_t}{\alpha}\right)^{-\alpha} - \left(1+\frac{2\lambda_t}{\alpha}\right)^{-\alpha}\right] \tag{9}$$

$$Yield(b) = Yield(c) = 2\left(1+\frac{\lambda_s+\lambda_t}{\alpha}\right)^{-\alpha} + 2\left(1+\frac{\lambda_s}{\alpha}\right)^{-\alpha}\left(1+\frac{\lambda_t}{\alpha}\right)^{-\alpha}$$
$$-2\left(1+\frac{\lambda_s+\lambda_t}{\alpha}\right)^{-\alpha}\left(1+\frac{\lambda_s}{\alpha}\right)^{-\alpha} - 2\left(1+\frac{\lambda_s+\lambda_t}{\alpha}\right)^{-\alpha}\left(1+\frac{\lambda_t}{\alpha}\right)^{-\alpha} + \left[\left(1+\frac{\lambda_s+\lambda_t}{\alpha}\right)^{-\alpha}\right]^2 \tag{10}$$

It can be easily proven that for any values of λ_s and λ_t, $Yield(b) = Yield(c) \geq Yield(a)$.

If, on the other hand, the chip consists of two vertical blocks, then clearly, $Yield(b)$ is given by Equation (14) and $Yield(a)$ is equal to $Yield(c)$ and is given by Equation (15). In this case, $Yield(a) = Yield(c) \geq Yield(b)$ for all values of λ_s and λ_t. Floorplan (c) should, therefore, be preferred over (a) and (b). An intuitive justification for the

choice of floorplan (c) is that it guarantees the separation between the primary modules and their spares for any block size and shape, which results in a higher yield.

4. Practical Test Cases

We illustrate the general principles stated above through two practical cases, namely, DEC's ECL microprocessor [8] and Hughes Research Laboratories' 3-D computer [9].

4.1 The ECL RISC Microprocessor

One of Digital Equipment Corporation's most recent ICs is a 300 MHz, 1.0 μm bipolar ECL RISC microprocessor. The 15.4 mm $\times$ 12.6 mm chip contains 468K bipolar transistors and implements a subset of MIPS R6000 architecture. It was designed in order to verify a new packaging technique, a new style of CAD tools and ECL circuit techniques. A simplified diagram of the chip's floorplan is shown in Figure 5. Figure 5

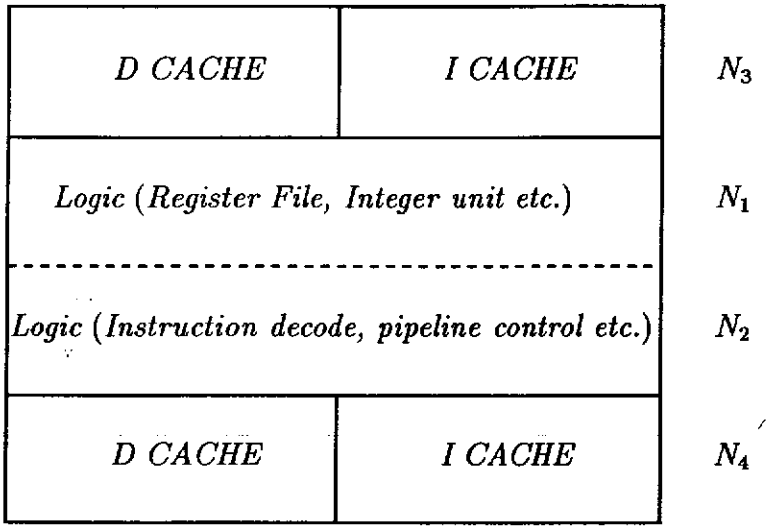

Figure 5: The original floorplan (simplified) of DEC's ECL RISC microprocessor.

shows that each of the two 2-KB cache units, the instruction cache and the data cache, has been separated into two halves, one at the top and the second at the bottom of the floorplan. Due to their small size, the two cache units do not include spare rows or columns for yield enhancement but include byte parity bits. The middle section of the chip, occupying almost half of its total area, contains the processor's logic units, e.g., a register file, an integer execution unit, instruction decode, pipeline control and alike.

The density of bipolar transistors and resistors in the two cache units is more than double the corresponding density in the remaining logic units [8]. The two cache units are, therefore, expected to have a higher fault density than the logic units, and we used the ratio $\lambda_{cache}/\lambda_{logic} = 2.5$ in our analysis. Consequently, we might consider alternative floorplans in an attempt to improve the projected yield, following the principles outlined in Sections 3.1 and 3.2. Using the notation introduced in Section 3.1, we partition the floorplan of DEC's ECL RISC processor into four, almost equal-sized, modules and denote them by N_3, N_1, N_2 and N_4 (as shown in Figure 5) so that the relation $\lambda_1 = \lambda_2 < \lambda_3 = \lambda_4$ is satisfied with $\lambda_1 = \lambda_2 = \lambda_{logic}$ and $\lambda_3 = \lambda_4 = \lambda_{cache}$. The "optimal" floorplan according to the analysis in Section 3.1 would be (N_1, N_3, N_4, N_2). This however, implies that the

processor will be divided into two almost equally sized modules and placed on both sides of the caches. If all the logic functional units must be kept adjacent to each other, then the floorplan (N_1, N_2, N_3, N_4) (i.e., the two halves of the cache units are placed next to each other) has been found to have a higher projected yield than that of the original floorplan. The optimal floorplan can, in principle, be implemented, but with an extra routing penalty. We clearly have a trade-off between yield improvement and increased routing overhead, a situation that we must expect to encounter in the general case.

Figure 6 shows the projected yield of the original floorplan, the alternative floorplan where the two halves of the cache units are placed next to each other, and the "optimal" floorplan. The yield has been calculated using the medium area clustering NB distribution with a block size of two modules (although similar results were obtained for a block size of three modules). The alternative floorplan has a higher projected yield than the original one. The "optimal" floorplan has the highest projected yield but it is not clear whether the relatively small marginal improvement in yield (compared to the alternative floorplan) justifies the additional routing penalty.

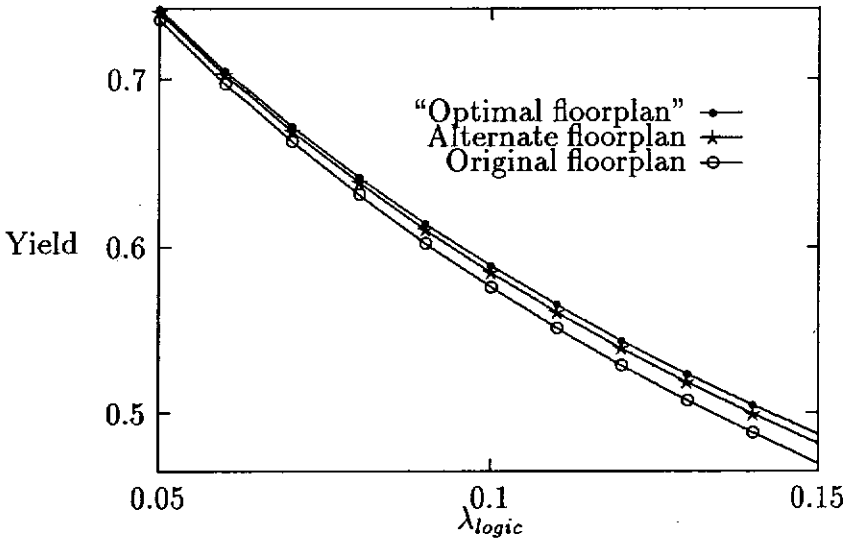

Figure 6: The yield of the original, alternate and "optimal" floorplans of DEC's ECL RISC microprocessor as a function of λ_{logic} (α=0.5, $\lambda_{cache}/\lambda_{logic}$=2.5).

4.2 The 3-D Computer

To illustrate the principles described in Sections 3.3 and 3.4 we study the floorplan of the 3-D computer designed by Hughes Research Laboratories [9]. The 3-D computer is a cellular array processor implemented in wafer scale integration (WSI) technology. The most unique feature of its implementation is the use of stacked wafers. The basic processing element is divided into five functional units, each of which is implemented on a different wafer. Thus, each wafer contains only one type of functional units and includes spares for yield enhancement as explained below. Units in different wafers are connected vertically through microbridges between adjacent wafers to form a complete processing element. The first working prototype of the 3-D computer, reported in [9], was of size 32×32. The current prototype includes 128×128 processing elements.

Fault tolerance in each wafer is achieved through a (2,4) interstitial redundancy scheme [10]. In this scheme, each primary unit is connected to two spare units, and each

spare unit is connected to four primary units, resulting in a redundancy of 50%. There are several ways in which the (2,4) scheme can be applied to two dimensional rectangular arrays [10]. The (2,4) structure that has been selected for implementation in the 3-D computer is shown in Figure 7 [9].

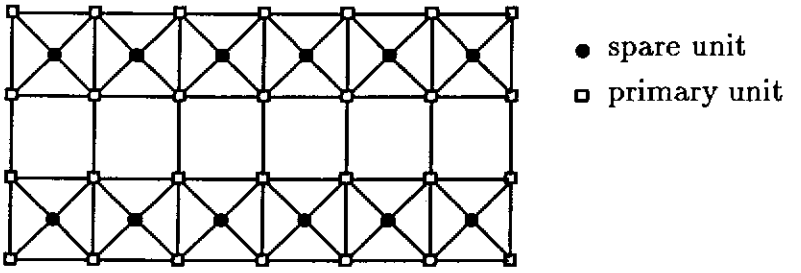

Figure 7: The original floorplan of a wafer in the 3-D computer.

The floorplan shown in Figure 7 has every spare unit adjacent to the four primary units that it can replace. This layout has short interconnection links between the spare and any primary unit that it may replace and as a result, the performance degradation upon a failure of a primary unit is minimal. However, the close proximity of the spare and primary units may lead to a low yield in the presence of clustered defects since a single cluster may cover several of these units, as has been experienced in practice [11]. There are several alternative floorplans that place the spare farther apart from the primary units connected to it (as recommended in Sections 3.3 and 3.4). Two such floorplans are shown in Figures 8 and 9. Another floorplan with similar characteristics has been followed in the current prototype of the 3D computer resulting in a higher yield [11].

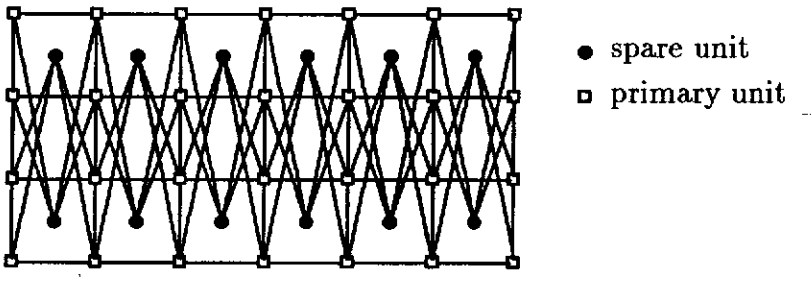

Figure 8: An alternative floorplan of a wafer in the 3-D computer.

The yield of the 128×128 array using either the original floorplan (depicted in Figure 7) or the alternative floorplan (depicted in Figure 8) are shown in Figures 10 and 11. The yield has been calculated using the medium area clustering NB distribution with a block size of two rows of primary units (see Figure 7). Figure 10 shows the yield of the original and alternate floorplans, depicted in Figures 7 and 8, respectively, as a function of λ (the average number of faults per unit) with α=2. It clearly shows that the alternative floorplan, in which the spare unit is separated from the primary units that it can replace, has a higher projected yield. Figure 11 shows the yield of the original and alternate floorplans as a function of α for two values of λ. We can see that for low values

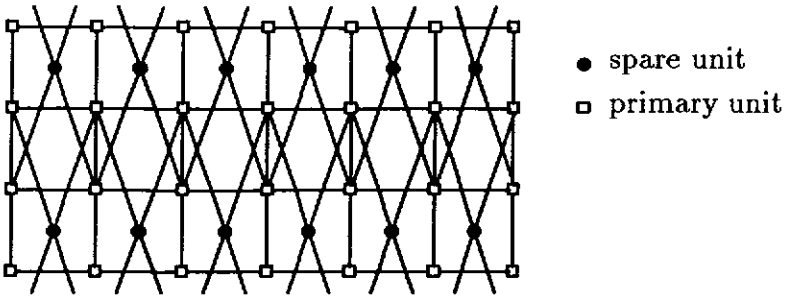

Figure 9: Another alternative floorplan of a wafer in the 3-D computer.

of the clustering parameter α, indicating heavy clustering, the chosen floorplan has a higher impact on the yield, while as α increases and the defect distribution approaches the Poisson distribution, the impact of the particular floorplan becomes less important.

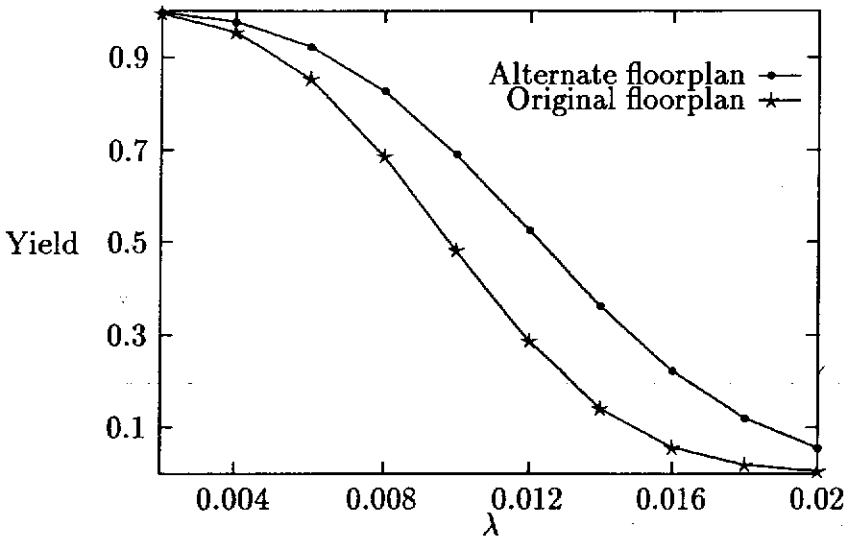

Figure 10: The yield of the original and alternate floorplans, depicted in Figures 7 and 8, respectively, as a function of λ (α=2).

5. Conclusions

The impact of floorplanning on the yield of large area fault-tolerant ICs with medium size fault clusters has been analyzed in this paper. We have shown that under certain circumstances, the selected floorplan can significantly affect the projected yield. This has been demonstrated through several theoretical test cases and through two practical examples, namely, DEC's ECL RISC processor and Hughes Research Laboratories' 3-D computer. In some cases, the exact size of the block (cluster of faults) has no effect on the resulting optimal floorplan, while in other cases, a different optimal floorplan emerges under different block sizes. In the latter case, the estimation of the block size is crucial to the floorplan selection, and several estimators for the block size have been suggested in [4]. We conclude that VLSI chip designers should take the yield into consideration, in addition to the more traditional factors like complexity of routing, when determining the floorplan of a new chip.

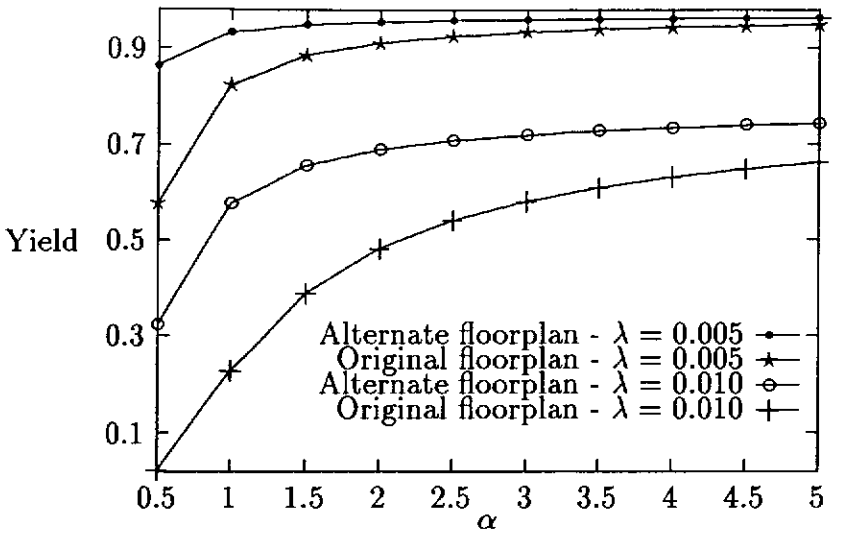

Figure 11: The yield of the original and alternate floorplans, depicted in Figures 7 and 8, respectively, as a function of α.

References

[1] F. Meyer and D.K. Pradhan, "Modeling Defect Spatial Distribution," *IEEE Trans. on Computers,* vol. 38, pp. 538-546, April 1989.

[2] I. Koren and C.H. Stapper, "Yield Models for Defect Tolerant VLSI Circuit: A Review," *Defect and Fault Tolerance in VLSI Systems*, I. Koren (ed.), pp. 1-21, Plenum, 1989.

[3] I. Koren, Z. Koren and C.H. Stapper, "A Statistical Study of Defect Maps of Large Area VLSI ICs," *IEEE Trans. on VLSI Systems*, Vol. 2, pp. 249-256, June 1994.

[4] I. Koren, Z. Koren and C.H. Stapper, "A Unified Negative Binomial Distribution for Yield Analysis of Defect Tolerant Circuits," *IEEE Trans. on Computers*, vol. 42, pp. 724-437, June 1993.

[5] Z. Koren and I. Koren, "Does the Floorplan of a Chip Affect Its Yield?," *1993 IEEE Workshop on Defect and Fault Tolerance in VLSI Systems*, pp. 159-166, Oct. 1993.

[6] D. W. Dobberpuhl *et al.*, "A 200-MHz 64-b Dual-Issue CMOS Microprocessor," *IEEE J. of Solid-State Circuits*, vol. 27, pp. 1555-1565, Nov. 1992.

[7] K. Sato *et al.*, "A Wafer-Scale-Level System Integrated LSI Containing Eleven 4-Mb DRAM's, six 64-Kb SRAM's, and an 18K-Gate Array," *IEEE J. of Solid-State Circuits*, vol. 27, pp. 1608-1613, Nov. 1992.

[8] N. P. Jouppi *et al.*, "A 300-MHz 115-W 32-b Bipolar ECL Microprocessor," *IEEE J. of Solid-State Circuits*, vol. 28, pp. 1152-1166, Nov. 1993.

[9] M. Yung, M. Little *et al.*, "Redundancy for Yield Enhancement in the 3D Computer," *Proc. IEEE Conf. on WSI,* pp. 73-82, Jan. 1989.

[10] A.D. Singh, "Interstitial Redundancy: An Area Efficient Fault Tolerance Scheme for Larger Area VLSI Processor Array," *IEEE Trans. on Computers*, Vol. 37, No. 11, November 1988, pp. 1398-1410.

[11] M. Yung, Private communication.