DOES THE FLOORPLAN OF A CHIP AFFECT ITS YIELD? [1]

Zahava Koren and Israel Koren*

Department of Industrial Engineering and Operations Research
*Department of Electrical and Computer Engineering
University of Massachusetts, Amherst, MA 01003

Abstract

The floorplan of a VLSI chip and its projected yield are usually considered to be completely unrelated issues. This commonly used assumption does not necessarily hold for several recently designed VLSI chips that incorporate some defect tolerance. The purpose of this paper is to investigate the relationship between floorplanning and yield for this type of chips.

1. Introduction

Until recently, yield issues were rarely considered when the floorplan of a new chip was decided upon, mainly for two reasons. First, most designed integrated circuits had no redundant circuitry (for the purpose of defect tolerance) and as such, their yield has been independent of their floorplan. Second, even for ICs with built-in defect tolerance, the exact floorplan of the chip has no effect on the projected yield when either the Poisson or the compounded Poisson yield models are employed (as was pointed out in [1]). In particular, the above statement applies to the most commonly used compounded Poisson model, which results in the negative binomial distribution with the large area clustering assumption [2] (i.e., the "size" of the defect clusters is assumed to be much larger than the size of the chip).

This situation is changing now with the introduction of defect-tolerant integrated circuits with a total area of $2cm^2$ and up [3]. Recent studies of defect maps of large area VLSI ICs [4] have shown that the commonly employed large area clustering negative binomial distribution does not provide a sufficiently accurate yield model for such large area ICs. Instead, the newly proposed medium size clustering model [5] proved to provide a much better match to empirical data [4].

The objective of this paper is to study the possible impact that the floorplan of a large area chip with redundancy may have on the yield of the chip, under the new yield model employing the medium area clustering negative binomial distribution. Our test cases are DEC's Alpha chip, with die size of $1.68cm \times 1.39cm$, containing 1.68 million transistors [3] and Hitachi's SLSI (System integrated LSI) chip with die size of $3.86cm \times 5.04cm$, containing eleven 4-Mb DRAM's, six 64-Kb SRAM's, and an 18K-Gate Array [6].

In Section 2 we present an example of a simplified yield analysis of some hypothetical chip. Section 3 then focuses on the Alpha chip, while Section 4 includes the analysis of the

[1] This work was supported in part by NSF, under contract MIP-9305912.

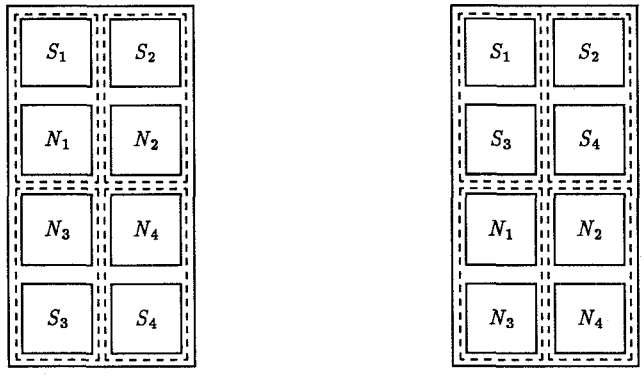
0-8186-3502-9/93 $3.00 © 1993 IEEE

SLSI chip. In all cases we show that different floorplans may result in different chip yields, although this difference may in some cases be insignificant.

2. A Simplified Model

To demonstrate the possible effect of the floorplan on the yield, we compare the yield of two floorplans a and b of a hypothetical chip depicted in Figure 1, making several assumptions for the sake of simplicity. The chip consists of eight equal-area modules, N_1, N_2, N_3, N_4, S_1, S_2, S_3 and S_4. N_1, N_2, N_3 and N_4 have no incorporated redundancy, S_2 is a spare for S_1 and S_4 is a spare for S_3. In the following discussion, we distinguish between manufacturing defects and logical faults. Only a fraction of the defects actually become faults, with the precise number depending on the layout of the circuit. We assume that for proper operation of the chip, either S_1 or S_2 and either S_3 or S_4 have to be fault-free, and N_1, N_2, N_3 and N_4 all have to be fault-free.

Clearly, if small area clustering (clusters smaller than or comparable to the size of a module) or large area clustering (clusters larger than or equal to the chip area) is assumed, the estimated yields of both floorplans will be equal. The conclusion is different, however, when medium area clustering is assumed. Suppose the block size (i.e., the approximate size of the defect clusters) is equal to the area of 2 modules (see Figure 1) and denote by p the probability that a block is defect-free. Each of the N_i modules can tolerate a defect



Floorplan a Floorplan b

Figure 1: Two alternative floorplans.

with probability g_N (i.e., $1 - g_N$ is the probability that a defect occurring in N_i will result in a chip-kill fault), while each of the S_i modules can tolerate a defect with probability g_S. Assuming statistical independence among the different blocks, we obtain for floorplan a in Figure 1

$$Yield(a) = \left[p^2 + 2p(1-p)g_N + (1-p)^2 g_N^2 (2g_S - g_S^2)\right]^2$$

and for floorplan b

$$Yield(b) = \left[p^2 + 2p(1-p)g_N^2 + (1-p)^2 g_N^4\right] \cdot \left[1 - (1-p)^2(1-(2g_S - g_S^2)^2)\right]$$

It can be shown algebraically that for $0 < p < 1$, $0 < \gamma_N < 1$ and $0 < g_S < 1$

$$Yield(a) < Yield(b)$$

Floorplan b should therefore be preferred over floorplan a (if yield maximization is the only consideration), and the two modules with redundancy should be placed next to each other rather than be separated by the modules without redundancy.

3. Yield Analysis of the Alpha Chip

The floorplan of the Alpha chip is depicted in Figure 2. The chip consists of the following

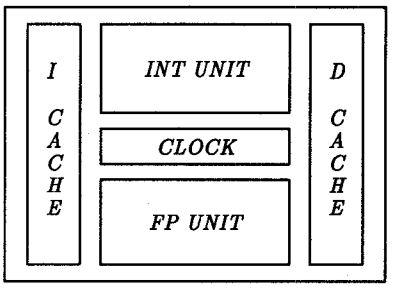


Figure 2: The floorplan of the Alpha chip.

functional units: the integer unit, the floating-point unit, the clock circuitry and two cache units. The two internal cache units are for data only (D-CACHE) or instructions only (I-CACHE). These two cache units have almost identical implementations. Each has 8 kilobytes (of data or instruction) organized as an array of 1024 cells wide by 66 cells tall. The top two rows (out of the 66 rows) constitute the redundant cells to replace either defective rows or defective individual cells. The remaining functional units have no redundancy incorporated into them and as such, each fault occurring in them is a *chip-kill* fault [2].

The current floorplan as shown in Figure 2 has the D-CACHE on one side and the I-CACHE on the other side of the chip. Another possible floorplan is depicted in Figure 3. Here, the two cache units are located next to each other. The effect of a cluster of defects intersecting the area of the I-CACHE may differ in the two alternative floorplans. In the current floorplan, such a cluster would result in chip-kill faults, rendering the chip useless. The same cluster of defects in the alternate floorplan (Figure 3) would possibly be tolerated. However, one can easily imagine a scenario of clusters of defects for which the first floorplan may prove to be better than the second one. There is a need, therefore, for a more careful analysis of the impact of the floorplan on the yield.

For the purpose of yield calculation, one row in a cache (1024×1 cells) is considered a module and its area has been chosen as the unit area. The total area of the chip, measured in these units, can be approximated by 396 area units. The fault density per unit area is denoted by λ_1 for the caches and by λ_2 for the remaining area. Usually, $\lambda_2 < \lambda_1$ since the layout of the random logic portion of the chip is less dense than that of the cache units. The fault distribution is the medium-area negative binomial distribution, with a clustering

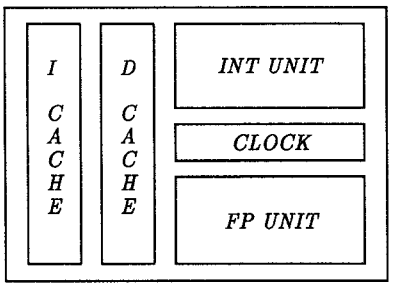


Figure 3: An alternate floorplan.

parameter α and block size (the size of the defect clusters) varying between 1 and 396 (the chip area). The projected yields of the two floorplans are depicted in Figures 4 and 5.

Figure 4 shows the yield of the original and alternate floorplans (depicted in Figures 2 and 3, respectively) as a function of λ (the average number of defects per mm^2) for two values of the ratio λ_2/λ_1, namely 0.1 and 0.9. The examined block size has a width equal to the width of the entire chip and a height of 198 cache rows. The value of the clustering parameter is determined so that $\alpha_{chip} = 2.0$ [8]. We can see that there is no difference in the two yields for $\lambda_2/\lambda_1 = 0.9$, while for $\lambda_2/\lambda_1 = 0.1$ the alternate floorplan is slightly better, especially for the larger values of λ. However, for practical values of λ around $0.003/mm^2$ [8] the difference is negligible.

Figure 5 shows the yield of the original and alternate floorplans of the Alpha chip as a function of the block size for two values of λ_2/λ_1 and two values of λ_1. The width of the block is fixed (set at the width of a single cache row) and the height is variant. For all values of λ_1 and λ_2, and either very small or very large values of the block size, the two floorplans have the same projected yield. Very small and very large block sizes correspond to the small area negative binomial distribution and the large area negative binomial distribution, respectively. For medium size blocks the difference between the yield of the two floorplans may have some significance only for low values of λ_2/λ_1, and a high value of the defect density. We conclude therefore that for practical purposes the two floorplans are equally good.

4. Yield Analysis of the SLSI Chip

The floorplan of Hitachi's SLSI chip is depicted in Figure 6. The chip size is $38.16 \times 50.4 = 1923.26mm^2$ and could not fit the conventional reticle, which allows a maximum chip size of about $200mm^2$. Therefore, to manufacture the SLSI chip, the wafer underwent four separate fabrication steps in which the gate array, the SRAMs, the DRAMs and the interconnections were patterned. The 11 4Mb DRAMs which consume most of the chip area use a $0.8\mu m$ process and incorporate redundancy for defect tolerance. The remaining units in the chip use a $1.3\mu m$ relaxed process and have no redundancy.

In what follows we will concentrate on the DRAMs, the only units in the chip that employ some defect tolerance technique. Each DRAM is internally organized as a 1M word $\times$ 4 bits

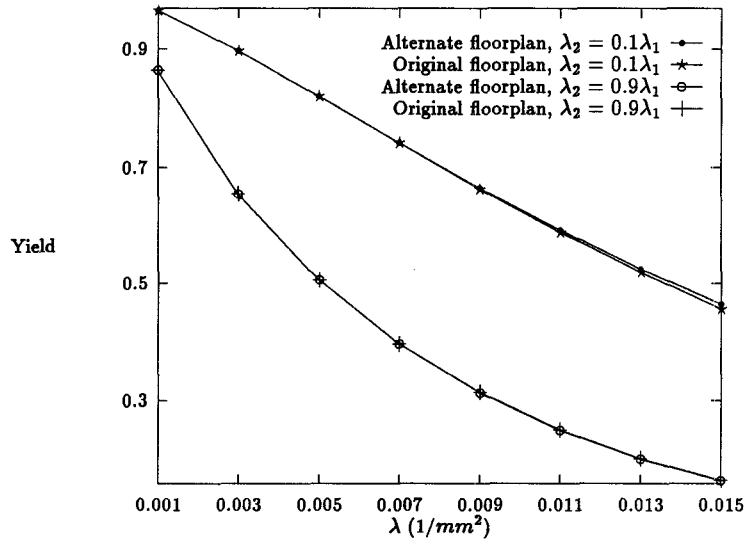


Figure 4: The yield of the original and alternate floorplans of Alpha as a function of λ for two values of the ratio λ_2/λ_1 (with block size=198 and $\alpha_{chip} = 2.0$).

memory. Thus, the DRAM consists of four identical parts, and each one of these four parts, in turn, is divided into 8 sections which are called 'mats'. This is done to reduce resistance and stray capacitance on the bit lines. We estimate the DRAM size to be $13mm \times 5.5mm$ and assume that the internal organization of each mat is 128 words × 1K bits, i.e., there are 1K bit lines in every mat with 128 memory cells per bit line. Such an internal organization is typical of most 4Mb DRAM chips.

The DRAM employs two defect tolerance techniques: adding spare lines, and using only six out of the 11 fabricated DRAMs. Even the first technique is somewhat different from the traditional technique of adding spare lines. Instead of adding spare lines to every mat, all eight mats (in a quarter of the 4 Mb DRAM) share a set of redundant word lines that can be used to replace defective lines in each one of the eight mats. The traditional technique of adding spare lines to each mat separately would require a large number of spare lines since defects tend to cluster. The alternate technique of providing spare lines that are common to all eight mats requires fewer spares. Since each DRAM contains 32 mats, the requirement of having six operational DRAMs means that out of $32 \times 11 = 352$ mats, $32 \times 6 = 192$ acceptable mats are needed. Some of these 192 mats may be defect-free mats and some may have a few defective lines which are replaced by spare lines.

In the original floorplan depicted in Figure 6, the 18K gate array is positioned at the center of the chip. This equalizes the length of the communication links between the gate array and the SRAMs and DRAMs to eliminate timing mismatches. An alternative floorplan that will still keep the communication link equalized is shown in Figure 7. For

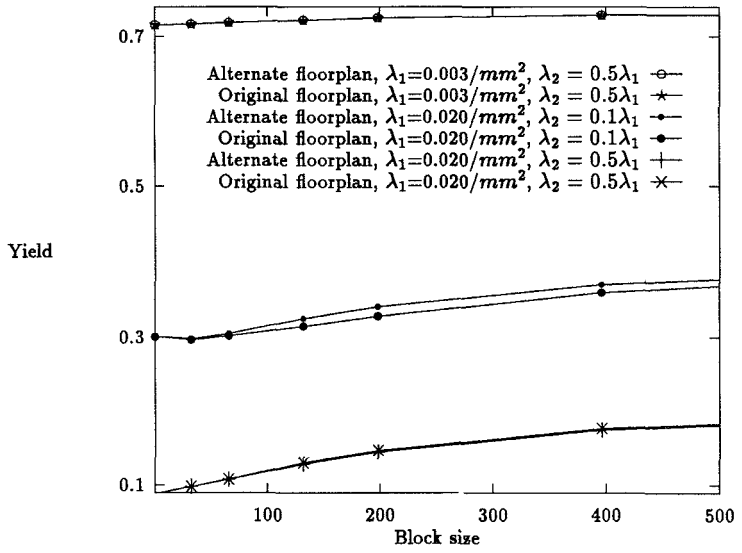


Figure 5: The yield of the original and alternate floorplans of Alpha as a function of the block size for two values of λ_1 and two values of λ_2/λ_1 (with $\alpha_{chip} = 2.0$).

yield calculation purposes, we divided the chip area into 36 modules, enabling the choice of block sizes between 1×1 and 6×6. As can be expected, there was no significant difference in yield between the two floorplans when either very small or very large block sizes have been selected. There were some noticeable differences, however, for medium size blocks, as can be seen in Figure 8. This figure depicts the yield of both the original and the alternate floorplans as a function of λ_1 (the defect density of the DRAM's) for $\lambda_2/\lambda_1 = 0.5$, $\alpha = 1.5$ and two block sizes, namely 6×2 and 2×3. Figure 8 demonstrates that for a block size of 6×2 the yield of the original floorplan is much higher than that of the alternate, while for a block size of 2×3, the alternate floorplan is slightly better than the original one.

5. Conclusion

We have shown that for recently designed integrated circuits the selected floorplan may affect the expected yield of the chip. Still, the complexity of routing (including number and length of wires, total area consumption, and design time) is expected to remain the major factor to be considered when deciding on the floorplan of a chip. The designer should, however, be aware of the impact of the selected floorplan on the yield and take it into consideration.

Acknowledgment: The authors would like to thank Randy Collica for providing estimates for the values of λ and α for the Alpha chip.

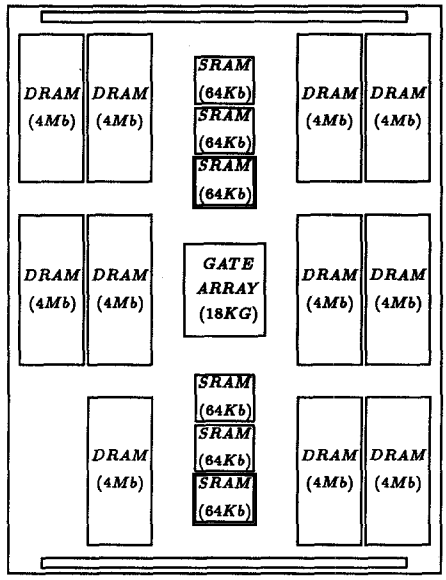


Figure 6: The floorplan of the SLSI chip.

References

[1] F. Meyer and D.K. Pradhan, "Modeling Defect Spatial Distribution," *IEEE Trans. on Computers*, vol. 38, pp. 538-546, April 1989.

[2] I. Koren and C.H. Stapper, "Yield Models for Defect Tolerant VLSI Circuit: A Review," *Defect and Fault Tolerance in VLSI Systems*, I. Koren (ed.), pp. 1-21, Plenum, 1989.

[3] D. W. Dobberpuhl *et al.*, "A 200-MHz 64-b Dual-Issue CMOS Microprocessor," *IEEE J. of Solid-State Circuits*, vol. 27, pp. 1555-1565, Nov. 1992.

[4] I. Koren, Z. Koren and C.H. Stapper, "Analysis of Defect Maps of Large Area VLSI ICs," *1992 IEEE Workshop on Defect and Fault Tolerance in VLSI Systems*, pp. 267-276, 1992.

[5] I. Koren, Z. Koren and C.H. Stapper, "A Unified Negative Binomial Distribution for Yield Analysis of Defect Tolerant Circuits," *IEEE Trans. on Computers*, vol. 42, June 1993.

[6] K. Sato *et al.*, "A Wafer-Scale-Level System Integrated LSI Containing Eleven 4-Mb DRAM's, six 64-Kb SRAM's, and an 18K-Gate Array," *IEEE J. of Solid-State Circuits*, vol. 27, pp. 1608-1613, Nov. 1992.

[7] R. S. Collica et al., "A Yield Enhancement Methodology for custom VLSI Manufacturing," *Digital Technical Journal*, vol. 4, no. 2, pp. 83-99, Spring 1992.

[8] R. S. Collica, Private communication.

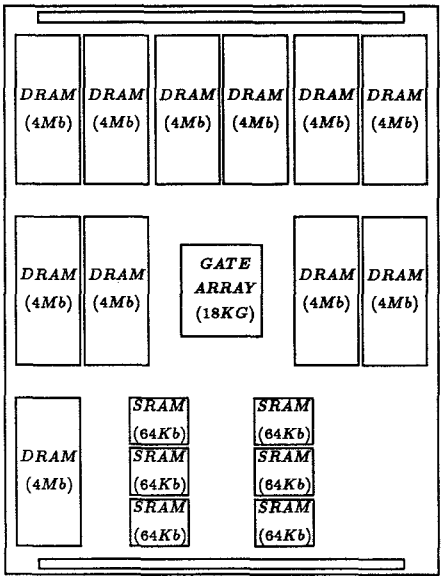


Figure 7: An alternative floorplan for the SLSI chip.

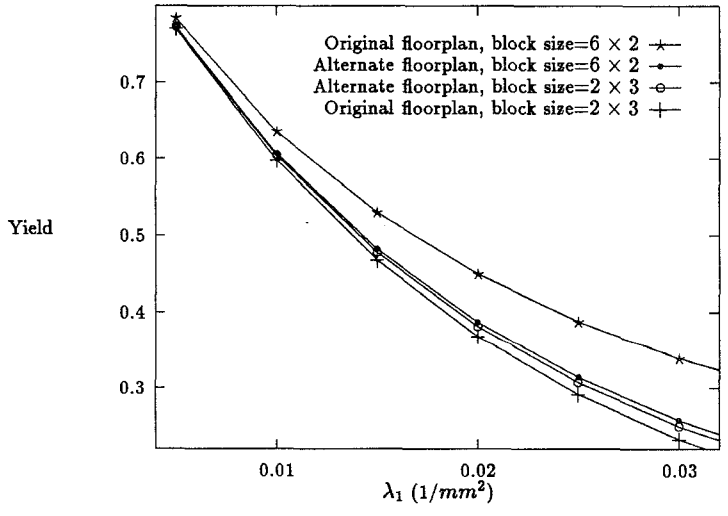


Figure 8: The yield of the original and alternate floorplans of the SLSI chip as a function of λ_1 for two values of the block size (with $\lambda_2 = 0.3\lambda_1$ and $\alpha = 1.5$).