A UNIFIED APPROACH TO YIELD ANALYSIS OF DEFECT TOLERANT CIRCUITS [1]

Zahava Koren and Israel Koren

University of Massachusetts at Amherst
Department of Electrical and Computer Engineering
Amherst, MA 01003

ABSTRACT

The dependence of the yield of defect tolerant VLSI circuits on the size of defect clusters (relative to the chip size) has been recently recognized. Consequently, models for yield analysis have been proposed for "large area clustering" and "small area clustering". By adding a new parameter, the *block size*, to the existing parameters of the defect distribution we unify the analysis of the existing models and at the same time add a whole range of "medium size clustering" models, thus increasing the flexibility in choosing the appropriate yield model. We illustrate our approach through several numerical examples and propose methods for estimating the newly defined block size.

1. INTRODUCTION

When manufacturing defect tolerant VLSI circuits, the precise estimation of the yield is crucial since it determines the amount of redundancy to be added to the circuit. The accuracy of the estimated yield depends on the model selected to describe the spatial distribution of manufacturing defects. For some time in the past the Poisson distribution was used, resulting in simple yield calculations since under the Poisson assumption the defects occurring in distinct areas are statistically independent. Researchers today agree that the distribution of manufacturing defects has more clusters than predicted by the Poisson distribution. Several distributions that allow such increased clustering of defects have been suggested, most notably the negative binomial distribution which was shown to have a good fit with actual defect distributions.

The negative binomial distribution has two parameters, λ - the average number of defects, and α - the so called clustering parameter, which actually measures the deviation from the Poisson distribution. The smaller the value of α, the larger the deviation. However, these two parameters are not sufficient for yield calculations of

[1] This work was supported in part by NSF under contract MIP-8805586.

circuits with redundancy. The assumption that the number of defects in an area of size A has a negative binomial distribution with parameters (λ_A, α_A) enables only the calculation of the probability of having x defects in the given area, namely,

$$Prob\ (x) = \frac{\Gamma(\alpha_A + x)}{x!\ \Gamma(\alpha_A)} \frac{(\lambda_A/\alpha_A)^x}{(1 + \lambda_A/\alpha_A)^{\alpha_A + x}}$$

In particular, it enables finding the probability of zero defects which, if no redundancy exists, constitutes the yield of the given area,

$$Yield = Prob\ (0) = \ (1 + \lambda_A/\alpha_A)^{-\alpha_A}$$

However, if the circuit has some redundancy in it, it is essential to calculate probabilities pertaining to partial areas, a task which is impossible without some additional assumptions regarding the clustering. This results from the fact that although the parameter λ_A can be extrapolated to an area of size A^* by $\lambda_{A^*} = \lambda_A \cdot \frac{A^*}{A}$, the parameter α_A cannot be easily extrapolated to areas either larger or smaller than A. Such an extrapolation would depend on the clustering pattern within A, a pattern which the two parameters (λ_A, α_A) fail to provide.

Most of the proposed models for estimating the manufacturing yield of defect tolerant VLSI circuits have noticed this inadequacy, and therefore assumed "large area clustering" [1], implying that α is constant for any sub-area of the wafer. Very few technical papers have addressed the cases of small and medium sized clustering, relative to the chip size, e.g., [4] in which α is assumed almost proportional to the area. Some papers ignore the size of the clusters altogether. An attempt to deal with the size of the clusters has been made in [2], however the approach there is impractical due to the prohibitive number of parameters in the model.

In this paper we do not investigate the cluster behavior and its effect on the yield. Instead, we view the size of the clusters as the result of the wafer area being divided into sub-areas which we call "blocks", such that the defects in distinct blocks are statistically independent. The defects within each block (if any exist) are uniformly distributed, hence the partial areas of the same block are statistically dependent. We suggest the addition of the *block size* as the third parameter of the spatial negative binomial distribution. This new parameter enables us to treat in a unified manner "small area clustering" and "large area clustering" which until now have been treated in two different ways, and "medium area clustering" for which, to the best of our knowledge, no satisfactory model has been developed.

The notion of "block size" (to be defined in the next section) has several advantages over the previously used "cluster size". It can be defined mathematically, while we have not found any satisfactory definition of the cluster size. Due to the exact definition, statistical properties of the fault distribution can be proven rigorously. One such property which is significant for yield calculation is that α remains constant as long as the considered area is confined within the same block and increases when the area exceeds that of the block. The introduction of the block size enables also the development of a unified approach to yield calculation for the different "cluster sizes". This provides more flexibility in choosing an appropriate yield model, and can be used to find how sensitive the calculated yield is to the specific block size assumed.

The objective of this paper is therefore, to introduce a unified approach to yield analysis by adding a third parameter, i.e., the block size, to the two parameters of

the negative binomial distribution and to demonstrate its use when calculating the yield of defect-tolerant circuits.

The paper is organized as follows. In the next section we describe the yield model and define the suggested parameter - the block size. In Section 3 we demonstrate the use of the block size in yield calculation for a relatively simple case, while in Section 4 the calculation is generalized to a more practical situation. Section 5 presents some numerical results illustrating the use of the formulas of Section 4, and in Section 6 we propose statistical methods for estimating the block size for given empirical data. Final conclusions are presented in Section 7.

2. THE MODEL DESCRIPTION

To illustrate the use of the suggested third parameter for the unification of yield models we chose a relatively simple problem, namely that of calculating the yield of a chip consisting of N equivalent modules, out of which M are needed for proper operation and $N - M$ are spares which can replace any of the M modules if they are defective. The same analysis can be applied to calculating the yield of partially good chips, i.e., chips which have no redundancy but can still be used (though to a lesser degree) when some of their modules are faulty.

To further simplify the obtained expressions and to avoid complex geometrical considerations we assume that the chip is, for computational purposes, one-dimensional, i.e., its modules are arranged in a row whose height is equal to the height of each module. The area of a module is defined to be the unit area. We further assume that a wafer consists of S modules and that the number of defects per wafer has a negative binomial distribution with parameters (λ_W, α_W). The yield of the chip is the probability that at least M out of the N modules are defect-free. Calculating this probability involves dealing with sub-areas of the chip, hence, as explained before, the two parameters (λ_W, α_W) are not sufficient and a third parameter is required which would indicate which sub-areas within the wafer are statistically independent with regard to the manufacturing defects. We suggest the use of a parameter called *Block Size* defined as follows.

Definition: The *Block Size* is the smallest number B such that the wafer can be divided into disjoint areas of size B each, so that these areas are statistically independent with regard to manufacturing defects.

The relationship between the block size and the vague "cluster size" is not very clear. Though it seems that defect clusters will tend to be confined to areas of size B, actual clusters can be either smaller or larger than B. It would be tempting to assume that B is equal to the average cluster size, however, we know of no formal proof for that, mainly because there is no rigorous definition of the term "cluster size".

In the next theorem we state several properties of the block size. In particular, we prove that the block possesses the same property once attributed to the cluster, namely, that the parameter α is constant for all areas within the same block and is increasing linearly with the number of blocks included in the given area.

Theorem: Let the number of defects in the wafer have a negative binomial distribution with parameters (λ_W, α_W) and block size B, and let S denote the wafer size (measured in number of modules), then

1. The number of defects in a block has a negative binomial distribution with parameters $(\lambda_{BL}, \alpha_{BL})$ where

$$\lambda_{BL} = \frac{\lambda_W}{S/B} \quad ; \quad \alpha_{BL} = \frac{\alpha_W}{S/B} \tag{1}$$

and the block size is B.

2. For any area of size A contained in a block, the number of defects has a negative binomial distribution with parameters $(\frac{A}{B}\lambda_{BL}, \alpha_{BL})$ and block size A.

3. For any area consisting of C blocks, the number of defects has a negative binomial distribution with parameters $(C\lambda_{BL}, C\alpha_{BL})$ and block size B.

Proof: The proof of all three parts of the theorem is based on the generating function of the negative binomial distribution. Let $P(x)$ denote the probability function of a negative binomial random variable with parameters (λ, α), i.e.,

$$P(x) = \frac{\Gamma(\alpha + x)}{x!\,\Gamma(\alpha)} \frac{(\lambda/\alpha)^x}{(1 + \lambda/\alpha)^{\alpha+x}} \tag{2}$$

Then,

$$G(z) = \sum_{x=0}^{\infty} P(x) z^x = \left(1 + \frac{(1-z)\lambda}{\alpha}\right)^{-\alpha} \tag{3}$$

Let $G_1(z)$, $G_2(z)$, $G_3(z)$, and $G_4(z)$, denote the generating functions of the number of defects in the wafer, in a block, in an area of size A contained in a block, and in an area consisting of C blocks, respectively.

1. Since there are S/B independent blocks in the wafer,

$$G_1(z) = (G_2(z))^{S/B}$$

hence,

$$G_2(z) = (G_1(z))^{B/S} = \left(1 + \frac{(1-z)\lambda_W}{\alpha_W}\right)^{-\frac{B}{S}\alpha_W} = \left(1 + \frac{(1-z)\frac{B}{S}\lambda_W}{\frac{B}{S}\alpha_W}\right)^{-\frac{B}{S}\alpha_W} \tag{4}$$

The right most side of (4) is the generating function of a negative binomial distribution with parameters $(\frac{\lambda_W}{S/B}, \frac{\alpha_W}{S/B})$. The block size is clearly B.

2. Let $P_{(2)}(x)$, $P_{(3)}(x)$ be the probability functions of the number of defects in the whole block and in area A, respectively. Since we assume a uniform distribution of the defects inside the block, the probability of each block defect to fall within area A is A/B. Hence,

$$P_{(3)}(x) = \sum_{i=x}^{\infty} P_{(2)}(i) \binom{i}{x} \left(\frac{A}{B}\right)^x \left(1 - \frac{A}{B}\right)^{i-x}$$

and,

$$G_{(3)}(z) = \sum_{x=0}^{\infty} P_{(3)}(x) z^x = \sum_{x=0}^{\infty} \sum_{i=x}^{\infty} P_{(2)}(i) \binom{i}{x} \left(\frac{A}{B}\right)^x \left(1 - \frac{A}{B}\right)^{i-x} z^x$$

By interchanging the order of summation we obtain

$$G_{(3)}(z) = \sum_{i=0}^{\infty} P_{(2)}(i) \sum_{x=0}^{i} \binom{i}{x} \left(\frac{zA}{B}\right)^x \left(1 - \frac{A}{B}\right)^{i-x}$$

$$= \sum_{i=0}^{\infty} P_{(2)}(i) \left(1 - \frac{A}{B} + \frac{zA}{B}\right)^i = G_{(2)}\left(1 - \frac{A}{B} + \frac{zA}{B}\right)$$

Since $G_{(2)}(z) = \left(1 + \frac{(1-z)\lambda_{BL}}{\alpha_{BL}}\right)^{-\alpha_{BL}}$, it follows that

$$G_{(3)}(z) = \left(1 + \frac{\frac{A}{B}(1-z)\lambda_{BL}}{\alpha_{BL}}\right)^{-\alpha_{BL}} \tag{5}$$

The last expression is the generating function of a negative binomial distribution with parameters $(\frac{A}{B}\lambda_{BL}, \alpha_{BL})$. Since B is the block size for the whole wafer and $A < B$, the block size for the partial area must be A.

3. The C blocks are independent with regard to defects, each having a generating function $G_{(2)}(z)$, hence

$$G_{(4)}(z) = \left(G_{(2)}(z)\right)^C = \left(1 + \frac{(1-z)\lambda_{BL}}{\alpha_{BL}}\right)^{-C\alpha_{BL}} = \left(1 + \frac{(1-z)C\lambda_{BL}}{C\alpha_{BL}}\right)^{-C\alpha_{BL}} \tag{6}$$

which is the generating function of a negative binomial distribution with parameters $(C\lambda_{BL}, C\alpha_{BL})$. □

Corollary: The module parameters (λ_M, α_M) can be obtained as follows,

$$\lambda_M = \frac{\lambda_{BL}}{B} = \frac{\lambda_W}{S} \tag{7}$$

$$\alpha_M = \alpha_{BL} = \frac{\alpha_W}{S/B} \tag{8}$$

Proof: A module is a sub-area of a block, hence (7) and (8) follow directly from parts 1 and 2 of the theorem. □

We have so far found the block parameters and the module parameters based on the wafer parameters and the block size B. In our model, the chip parameters are not calculated since the relation between the chip parameters and the module parameters depends on the exact location of the chip relative to the blocks. A chip may lie entirely within one block or stretch over several blocks. Even when the block is larger than the chip, the chip area may still be divided between two adjacent blocks. In our calculations, only the module parameters will be used, but as can be seen from (7) and (8) they are a function of the block size B.

Given the three parameters λ_W, α_W and the block size B, our aim is to calculate the probability that exactly k out of the N chip modules are fault-free, denoted by $P_N(k)$. This probability can be used to obtain the yield of chips with redundancy,

$$Y = \sum_{k=M}^{N} P_N(k) \tag{9}$$

or to find the equivalent yield (i.e., the expected number of operational modules) of partially good chips,

$$Y_{EQ} = \sum_{k=J}^{N} \frac{k}{N} P_N(k) \tag{10}$$

where J is the minimal number of modules that have to be fault-free for the chip to be usable.

3. A SIMPLE CASE

We begin by discussing the simple case in which B is a divisor of N, and the chip covers exactly $\frac{N}{B}$ blocks. This includes the case $B > N$ which is equivalent to $B = N$. We will deal with the general case in the next section.
The above includes the following special cases:

(a) *Small size clustering.* In this case, $B = 1$ and all modules are assumed to be statistically independent.

(b) *Large size clustering.* In this case $B = N$, which implies that the defects within the entire chip are uniformly distributed and that all sections of the chip are statistically dependent. The probability $P_N(k)$ for this case has been researched extensively and the equivalence of most of the proposed expressions has been proven in [1].

(c) *Medium size clustering,* i.e., $1 < B < N$.

In case (a), the fault distribution of a single module is considered, and then the N modules are combined using the binomial distribution. In case (b), on the other hand, the defects in the entire chip are considered and distributed uniformly throughout the chip. In case (c) we have to utilize an intermediate method, in which each block is considered in its entirety, and the different blocks are then combined relying on their statistical independence. This method includes (a) and (b) as two extreme special cases.

Let J_i, K be the random variables denoting the number of fault-free modules in the i-th block and in the entire chip, respectively ($i = 1, ..., N/B$). $J_1, ..., J_{N/B}$ are independent and identically distributed random variables, and $K = \sum_{i=1}^{N/B} J_i$. For each block, the distribution of J_i can be obtained following the analysis of case (b), i.e., finding the probability of m defects occurring in a block and then distributing them uniformly among the B modules in the block. Once the distribution of J_i is found, the distribution of K can be obtained either by using convolutions, or as it is done in this paper, by using generating functions. Let $\Phi_{(B)}(z)$ and $\Phi_{(CH)}(z)$ be the generating functions of J_i and K, respectively, then

$$\Phi_{(CH)}(z) = \left(\Phi_{(B)}(z)\right)^{N/B} \tag{11}$$

Note that the generating functions $\Phi(z)$ are different from the generating functions $G(z)$ which were used in the previous section. The functions G characterize the number of defects in a given area, while the functions Φ pertain to the number of fault-free modules in a given area.

It has been shown in [1] that for a block of B modules for which the "large area clusters" assumption holds (i.e., the clusters are approximately the size of the block), the probability $P_B(j)$ of exactly j fault-free modules out of the B is equal to $a_{j,B}$ where

$$a_{j,B} = \binom{B}{j} \sum_{l=0}^{B-j} (-1)^l \binom{B-j}{l} \left(1 + \frac{(j+l)\lambda_M}{\alpha_M}\right)^{-\alpha_M} \tag{12}$$

$a_{j,B}$ serves as the probability function for the random variable J_i - the number of fault-free modules out of the B modules in block i $(i = 1, ..., \frac{N}{B})$, and can be used for calculating the generating function $\Phi_{(B)}(z)$. Since all J_i's are equivalent, the resulting generating function will not depend on i but on the block size B only.

$$\Phi_{(B)}(z) = \sum_{j=0}^{B} P_B(j) \cdot z^j = \sum_{j=0}^{B} a_{j,B} \cdot z^j$$

$$= \sum_{j=0}^{B} \binom{B}{j} \sum_{l=0}^{B-j} (-1)^l \binom{B-j}{l} \left(1 + \frac{(j+l)\lambda_M}{\alpha_M}\right)^{-\alpha_M} \cdot z^j$$

Using the identity $\binom{B}{j}\binom{B-j}{l} = \binom{j+l}{l}\binom{B}{j+l}$ and substituting m for $j+l$ we obtain,

$$= \sum_{m=0}^{B} \sum_{l=0}^{B} (-1)^l \binom{m}{l} \binom{B}{m} \left(1 + \frac{m\lambda_M}{\alpha_M}\right)^{-\alpha_M} \cdot z^{m-l}$$

Summing over l yields,

$$\Phi_{(B)}(z) = \sum_{m=0}^{B} \binom{B}{m} (z-1)^m \left(1 + \frac{m\lambda_M}{\alpha_M}\right)^{-\alpha_M} \tag{13}$$

The generating function of K (the number of fault-free modules in the entire chip), $\Phi_{(CH)}(z)$, can now be obtained from (11). Note that for the special case $B = N$ (large area clustering) we obtain,

$$\Phi_{(CH)}(z) = \Phi_{(N)}(z) = \sum_{m=0}^{N} \binom{N}{m} (z-1)^m \left(1 + \frac{m\lambda_M}{\alpha_M}\right)^{-\alpha_M} \tag{14}$$

while for $B = 1$ (small clusters),

$$\Phi_{(CH)}(z) = \left(\Phi_{(1)}(z)\right)^N = \left(1 + (z-1)\left(1 + \frac{\lambda_M}{\alpha_M}\right)^{-\alpha_M}\right)^N \tag{15}$$

The generating function $\Phi_{(CH)}(z)$ can be used for calculating the probabilities $P_N(k)$ by,

$$P_N(k) = \frac{1}{k!} \frac{\partial^{(k)}}{\partial z^k} \Phi_{(CH)}(z) \;/\; _{z=0} \tag{16}$$

Differentiating (14) k times and substituting in (16) yields,

$$P_N(k) = \binom{N}{k} \sum_{m=0}^{N-k} (-1)^m \binom{N-k}{m} \left(1 + \frac{(k+m)\lambda_M}{\alpha_M}\right)^{-\alpha_M} \tag{17}$$

which is analogous to (12) and is the known result for large area clustering [1]. Differentiating (15) k times and substituting in (16) we obtain,

$$P_N(k) = \binom{N}{k} \left(1 - \left(1 + \frac{\lambda_M}{\alpha_M}\right)^{-\alpha_M}\right)^{N-k} \left(1 + \frac{\lambda_M}{\alpha_M}\right)^{-\alpha_M k} \tag{18}$$

which is the known result for small area clustering [4].

For the special case $k = N$ (i.e., the chip is fault-free) we have,

$$\frac{\partial^{(N)}}{\partial z^N} \Phi_{(CH)}(z) = N! \left(1 + \frac{B\lambda_M}{\alpha_M}\right)^{-\alpha_M \frac{N}{B}} \tag{19}$$

which yields,

$$P_N(N) = \left(1 + \frac{B\lambda_M}{\alpha_M}\right)^{-\alpha_M \frac{N}{B}} \tag{20}$$

Substituting $B = N$ we obtain,

$$P_N(N) = \left(1 + \frac{N\lambda_M}{\alpha_M}\right)^{-\alpha_M} \tag{21}$$

while for $B = 1$,

$$P_N(N) = \left(1 + \frac{\lambda_M}{\alpha_M}\right)^{-N\alpha_M} \tag{22}$$

which again are the well-known probabilities of a fault-free chip for large area clustering and for small area clustering, respectively.

4. THE GENERAL CASE

In practice, the size of the chip is not necessarily an integer multiple of the block size, nor are the chip boundaries identical to the block boundaries. We need therefore, to generalize equation (11), which provides the generating function of the number of fault-free modules in a chip, to this more realistic situation.

Assuming that the chip is placed randomly within the block, there are B possible placements of the chip. The placement of the chip boundary relatively to the block boundary determines how the chip is divided between the adjacent blocks. In general, the chip will cover an integer number of full blocks and up to 2 partial blocks on both sides (see Figure 1). Let R_1 be the number of chip modules contained in the first (partial) block, F the number of full blocks covered by the chip and R_2 the number of chip modules contained in the last (partial) block. The chip area is thus divided into $(F + 2)$ areas (up to 2 of which may be empty) which are statistically independent with regard to their defects.

For a given configuration (R_1, F, R_2), the generating function for K - the number of fault-free modules in the whole chip can be obtained as a product of $(F + 2)$ generating functions of the form derived in (13),

$$\Phi_{(CH)}(z) = \Phi_{(R_1)}(z) \left(\Phi_{(B)}(z)\right)^F \Phi_{(R_2)}(z) \tag{23}$$

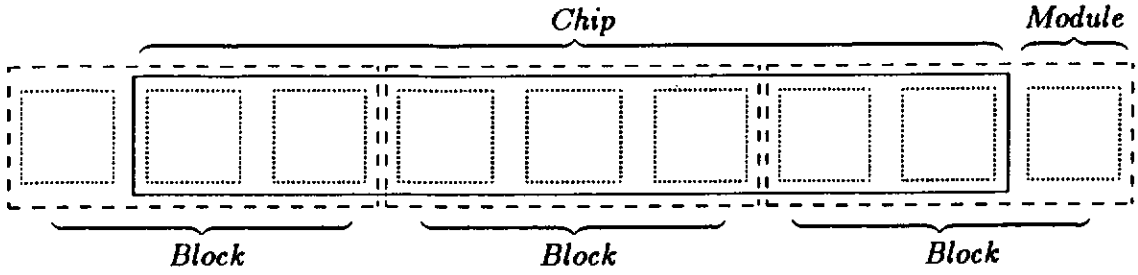

Figure 1: A placement of a chip relative to blocks, $F=1, R_1=R_2=2, B=3, N=7$.

where $\Phi_{(R)}(z) \equiv 1$ for $R=0$.

Assuming that the chip is equally likely to start at any of the B modules within the block, (23) has to be averaged over all values of R_1. Since R_1 is the size of a partial block, clearly $R_1 \leq B-1$. In addition, $R_1 \leq N$, hence $0 \leq R_1 \leq min(N, B-1)$. Given the value of R_1, $F = \left[\frac{N-R_1}{B}\right]$ and $R_2 = (N-R_1) \bmod B$. Note that for $B \leq N$, $R_1 = 0, ..., B-1$ while for $B > N$, the first N values are $R_1 = 0, ..., N-1$ and the last $B-N$ values of R_1 are all equal to N (indicating that the chip lies entirely inside the block). Denoting $R_1^* = min(N, R_1)$ and substituting the values of F and R_2 yields,

$$\Phi_{(CH)}(z) = \frac{1}{B} \sum_{R_1=0}^{B-1} \Phi_{(R_1^*)}(z) \left(\Phi_{(B)}(z)\right)^{\left[(N-R_1^*)/B\right]} \Phi_{\left((N-R_1^*) \bmod B\right)}(z) \qquad (24)$$

As in the previous case, $P_N(k)$ can be obtained by differentiating $\Phi_{(CH)}(z)$, and the yield of a chip with M out of N redundancy can be found using (9).

5. NUMERICAL RESULTS

To demonstrate the effect of using the concept of block size in yield calculation we calculated the yield of a chip consisting of 10 modules within a wafer of size 1000 modules. The numerical results are depicted in Figures 2, 3 and 4.

In Figure 2 we assume a fixed redundancy, i.e., 2 redundant modules were added for a total of 12. We show the dependency of the yield on the block size, for different values of the parameters (λ_W, α_W). As can be seen, for fixed values of (λ_W, α_W), the yield decreases as the block size increases. A possible explanation to this phenomenon is that for a larger block size, the defect clusters tend to be larger and it is more likely that more than 2 modules per chip will become faulty.

Figure 3 demonstrates the use of equation (24) for determining the optimal redundancy once the parameters λ_W, α_W and B are given. For three sets of parameters, the equivalent yield (i.e., the yield divided by the ratio between the area of the chip with redundancy and its area without redundancy) is depicted as a function of the amount of redundancy. As can be seen from this figure, the optimal amount of redundancy (if any) depends on the three parameters λ_W, α_W and B.

We have further analyzed this dependency and our results are depicted in Figure 4. This figure shows the optimal amount of redundancy (to be added to a chip consisting of 10 modules) as a function of the block size, for three sets of the parameters (λ_W, α_W). The optimal redundancy increases with each of the three parameters, λ_W, α_W and B.

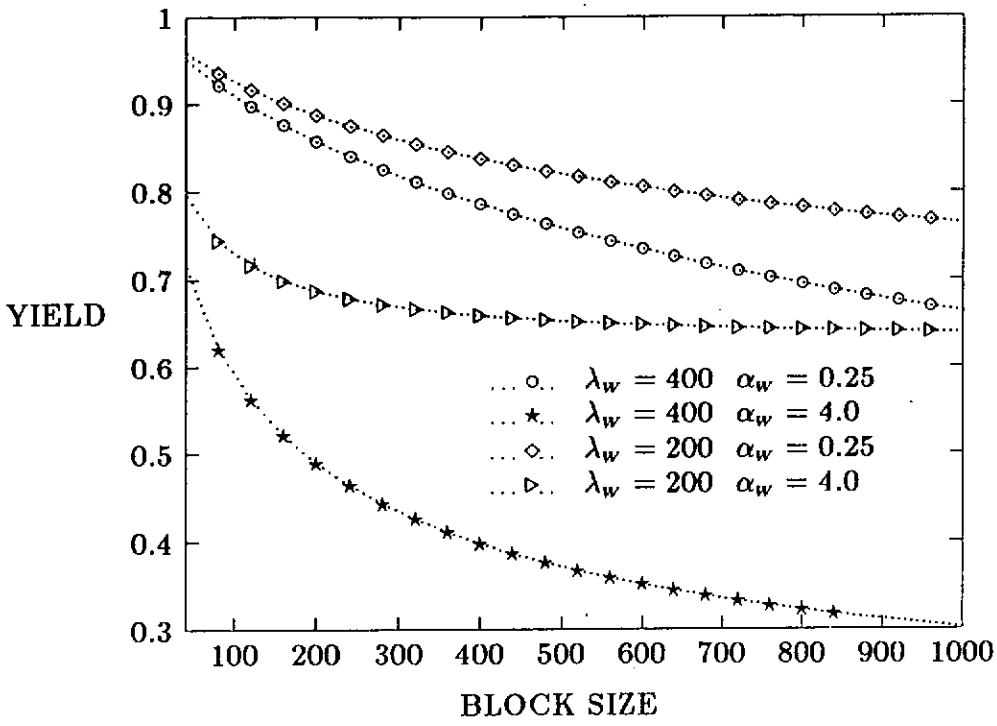

Figure 2: Yield as a function of block size.

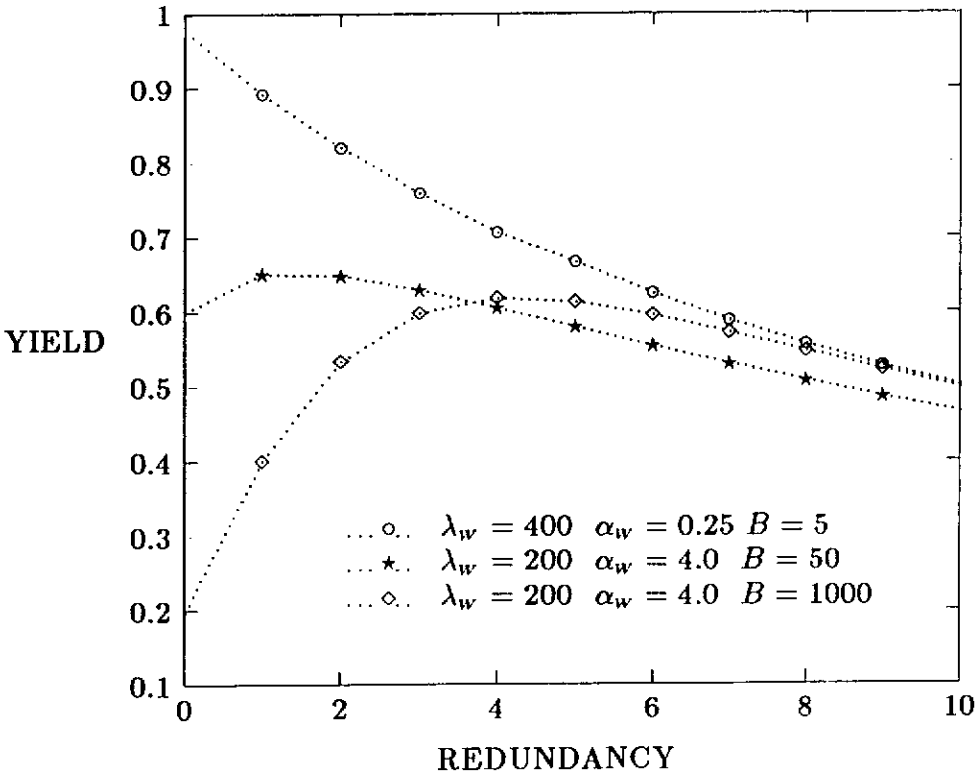

Figure 3: The equivalent yield as a function of the amount of redundancy.

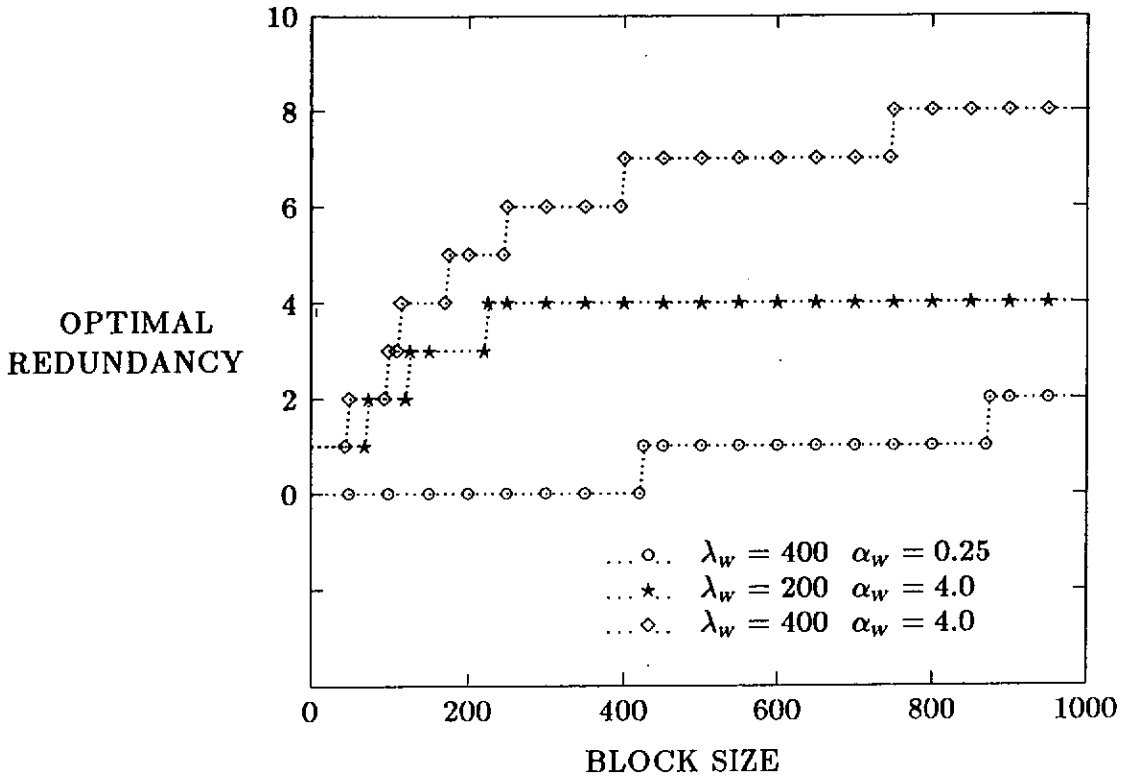

Figure 4: Optimal redundancy as a function of block size.

6. ESTIMATING THE BLOCK SIZE

As demonstrated in the previous sections, correct estimation of the block size is essential for proper evaluation of the yield of circuits with redundancy. The problem of determining the block size based on empirical data is not a standard statistical problem. Simple estimation based on averaging the sizes of actual clusters is very difficult since, given a defect map, it is not always clear what the boundaries of the clusters are. Moreover, even if the average cluster size can be estimated, its relation to the block size is not clear at this point.

We suggest two methods for estimating the block size. The first measures variations in the parameter α, similarly to what is suggested in [4]. The other is based on the statistical independence between adjacent blocks. A similar idea appears in [3] suggesting to check the correlation between adjacent blocks (or "regions" as they are called there). However, statistical dependence is a much stronger property than correlation and is much easier to detect.

Both approaches are based on a procedure called "the window method" [1] in which the wafer is divided into sub-areas (windows) which are increased at every step. Given W wafers with S modules each, start from $B = 1$ and then increase B by 1 at each step until the appropriate value of the block size is reached. For each fixed value of B, divide all the given wafers into windows of size B (thus having $T = \frac{WS}{B}$ windows) and then count the number of defects in each window denoting by X_i the number of defects in window i, $(i = 1, ..., T)$.

The first approach estimates B by utilizing the fact that the clustering parameter α is fixed for all areas within a block while it increases when the area consists of more than one block. For each fixed B, α is estimated using, for example, the following moment-method estimator. When a random variable X has a negative binomial distribution with parameters (λ, α), its expected value equals λ while its variance is given by,

$$V(X) = \lambda\left(1 + \frac{\lambda}{\alpha}\right) \tag{25}$$

The parameter λ is therefore estimated using

$$\bar{X} = \frac{1}{T}\sum_{i=1}^{T} X_i. \tag{26}$$

while the variance is estimated using

$$\hat{V} = \frac{1}{T}\sum_{i=1}^{T} X_i^2 - \bar{X}^2 \tag{27}$$

Equating (25) and (27), and substituting $\bar{X}$ for λ yields the following estimator for α,

$$\hat{\alpha} = \frac{\bar{X}^2}{\hat{V} - \bar{X}} \tag{28}$$

B is increased as long as $\hat{\alpha}$ remains more or less constant, and the block size is reached when $\hat{\alpha}$ starts increasing.

The objective in the second approach is to detect independence between adjacent blocks. For each value of B, all T windows are divided into $T/2 = WS/2B$ pairs of adjacent windows, counting the number of defects in each pair. Let $f(a,b)$ be the number of pairs with a defects in their first window and b defects in the second, and let $f(a,*) = \sum_b f(a,b)$ be the number of pairs with a defects in their first window, $f(*,b) = \sum_a f(a,b)$ the number of pairs with b defects in their second window. If adjacent windows were statistically independent, we would expect $\frac{f(a,b)}{T/2}$ to be close to $\frac{f(a,*)}{T/2} \times \frac{f(*,b)}{T/2}$ for all (a,b). A Chi-Square test can be used to test the goodness of fit. Denoting by $E(a,b)$ the expected frequencies, i.e., $E(a,b) = T \times \frac{f(a,*)}{T/2} \times \frac{f(*,b)}{T/2}$, we calculate

$$\chi^2 = \sum_{a,b} \frac{(f(a,b) - E(a,b))^2}{E(a,b)} \tag{29}$$

The block size is chosen as the first B for which the calculated value of χ^2 goes below some critical value (determined by the desired level of significance).

7. CONCLUSIONS

A unified approach to yield analysis of defect tolerant circuits has been presented in this paper. By adding a new parameter, namely, the block size, to the two existing parameters of the negative binomial distribution, we have unified the yield analysis for large area clustering, small area clustering and medium area clustering. We have

demonstrated through several numerical examples, the effect of the block size on the projected yield and consequently, on the optimal amount of redundancy. Finally, we have proposed methods for estimating the block size parameter of the defect distribution.

REFERENCES

[1] I. Koren and C.H. Stapper, "Yield Models for Defect Tolerant VLSI Circuit: A Review," *Defect and Fault Tolerance in VLSI Systems*, I. Koren (ed.), pp. 1-21, Plenum, 1989.

[2] F.J. Meyer and D.K. Pradhan, "Modeling Defect Spatial Distribution," *IEEE Trans. on Computers*, Vol. 38, pp. 538-546, April 1989.

[3] C.H. Stapper, "Correlation Analysis of Particle Clusters on Integrated Circuit Wafers," *IBM J. Res. Develop.*, Vol. 31, pp. 641-650, Nov. 1987.

[4] C.H. Stapper, "Small-Area Fault Clusters and Fault-Tolerance in VLSI Circuits," *IBM J. Res. Develop.*, Vol. 33, March 1989.