3.2 The Effect of Scaling on the Yield of VLSI Circuits

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INTRODUCTION

As IC technology advances, the minimum feature size of VLSI circuitry continues to decrease. The smaller feature size of transistors has the potential of speeding up the circuits and increasing the yield of the manufactured chips. The latter is due to the smaller silicon area of the chip resulting in a lower average number of defects per chip. Manufacturers of existing VLSI chips also attempt to take advantage of the possible reduction in feature size by scaling (shrinking) the existing designs of their VLSI chips.

The effect of scaling the physical dimensions of VLSI circuits on their electrical characteristics (and consequently on their speed of operation) has already been studied (e.g., Saraswat and Mohammadi 1982). The effect of scaling on the yield has been studied until now only for special cases like interconnection buses (Stapper 1984, Koren *et al* 1987). The subject of this paper is the effect of scaling on the yield of more general VLSI circuits.

The analysis of the effect of scaling on yield is complicated by the variety of types of manufacturing defects that can occur in VLSI circuits. These include dielectric pinhole defects, photolithographic defects, junction leakage defects etc. The number of these defects clearly depends on the physical dimensions of the chip. However, the dependence of one type of defects on the physical dimensions does not necessarily equal that of another type. Thus, the various types of manufacturing defects have to be considered and the effect of scaling on each of them has to be analyzed separately. Only then can the total effect of scaling on yield be determined.

In this paper we consider several types of manufacturing defects and analyze the possible changes in their effect on the yield, when scaling of a VLSI circuit is performed.

YIELD ANALYSIS

Defects may occur in the different steps of the manufacturing process. Some of these defects may result in missing patterns or open circuits while other defects may result in extra patterns or short circuits. Since these defects happen in separate manufacturing

steps, they may have different statistical characteristics and can usually be considered statistically independent (Stapper *et al* 1983). This leads to the following general expression for yield,

$$Y = \prod_{i=1}^{m} Y_i$$

where Y_i is the yield associated with step i and m is the number of manufacturing steps. It has been generally agreed upon that the distribution followed by most defects is a Poisson distribution whose parameter λ is not a constant but a random variable. This allows the modeling of defect clustering, a phenomenon that has been observed in practice. A convenient choice for the distribution function of λ is the Gamma function resulting in a Negative Binomial distribution (for the defects) for which the yield Y_i is given by,

$$Y_i = \left(1 + \frac{\bar{\lambda}_i}{\alpha_i}\right)^{-\alpha_i}$$

where $\bar{\lambda}_i$ is the average number of circuit faults occurring in step i, and α_i is the corresponding clustering parameter.

Note that $\bar{\lambda}_i$ is defined as the average number of circuit faults rather than manufacturing defects. The reason for this is that not all manufacturing defects result in faulty circuits which affect the yield of the chip. For example, a open-circuit type photolithographic defect occurring in a conductor can be harmless if its size is smaller than the width of the conductor (Ferris-Prabhu 1985, Stapper 1984). A dielectric pinhole defect will result in a short-circuit only if it occurs in the overlapping area between two conductors that cross each other and were produced at different photolithographic steps.

The average number of manufacturing defects is usually defined as $d_i A$ where d_i denotes the average number of defects per unit of area and A is the chip area. To calculate the average number of circuit faults we define a probability θ_i that a defect in step i will result in a faulty circuit and thus, $\bar{\lambda}_i = \theta_i d_i A$. The product $A\theta_i$ is also called the critical area for defects occurring in step i (Stapper 1984, Ferris-Prabhu 1985) and we denote it by $A_c^{(i)}$. The yield is therefore given by,

$$Y_i = \left(1 + \frac{d_i A_c^{(i)}}{\alpha_i}\right)^{-\alpha_i}$$

The probability that a defect will cause a circuit failure may be constant for one type of defects and may depend on the relative size of the defects (compared to the physical dimensions of VLSI patterns) for a different type of defects. Hence, to study the effect of scaling on the yield we analyze in what follows each of these two cases separately. We consider first dielectric pinhole defects for which the above probability is constant and then photolithographic defects for which this probability is a random variable.

Dielectric Pinhole Defects

The size of a dielectric pinhole defect is usually very small (compared to the size of VLSI patterns) and the probability that it will cause a circuit failure is simply the ratio between the area of the overlapping region to the total area A. If the physical dimensions of all patterns within the chip are scaled by the same factor a, i.e, *ideal scaling*, then the above probability remains unchanged.

Consequently, the effect of scaling on the critical area $A_c^{(i)} = A * \theta_i$ for pinhole defects is determined only by the change in the area A. Note that this simple dependence holds for any other manufacturing defects for which the probability that they will result in circuit faults is constant and does not change with scaling. For ideal scaling with $a < 1$, the area of the chip reduces to $a^2 A$ resulting in a similar reduction in the critical area $A_c^{(i)}$ which in turn may result in a higher yield Y_i.

The final effect of scaling on the yield Y_i depends also on any possible change in the clustering parameter α_i. The dependence of α_i on the area has been studied by Stapper (1986) and experimental data have shown that the clustering parameter can either decrease or increase when the chip area decreases. Any increase in the clustering parameter will increase the yield of the chip and vice versa. Combining this with the expected reduction in the critical area, we may conclude that if α_i increases with scaling ($a < 1$) or remains unchanged, the yield Y_i due to dielectric pinhole defects will increase. However, if α_i decreases with scaling, then the final effect of scaling on Y_i can be in either direction.

There is a different type of dielectric pinhole defects whose average number is proportional to the length of one conductor crossing over a second conductor. In this case,

$$Y_j = \left(1 + \frac{\theta_j d_j l}{\alpha_j}\right)^{-\alpha_j}$$

where d_j is the average number of defects per unit of length (instead of unit of area) and l is the length of the overlapping region. Again, the probability that such a defect will cause a circuit failure is constant and the final effect of scaling on the yield due to this type of defects is similar to the effect of scaling on the yield due to the previous type of "area" pinhole defects. The only difference is that l is reduced by the scaling factor a rather than by a^2.

Photolithographic Defects

The situation is different when photolithographic defects are considered. Here, the defects have a randomly distributed size which is comparable to that of VLSI patterns. Therefore, the probability that such a defect will cause a circuit failure depends on the exact shape of the pattern and its dimensions relatively to the size of the defect. Hence, when scaling a given pattern (with $a < 1$), less photolithographic defects can occur in the smaller area on one hand, but smaller defects may now cause a circuit failure on the other hand. The area A decreases to $a^2 A$ but the probability θ_i may increase. The final change in their product (i.e, the critical area) depends both on the specific given pattern and on the distribution of the defect size.

For convenience, we adopt the assumption made by Ferris-Prabhu (1985) and Stapper (1984) that a defect is circle shaped and we denote its diameter by x. Experimental data on defects in many wafers lead to the conclusion that the diameter x of a defect has a density function $f(x)$ which increases as x^q up to the mode x_o of the distribution (i.e., the value of x for which the density function is maximal) and then decreases as $1/x^p$ up to a maximum value of x_M, i.e.,

$$f(x) = \begin{cases} cx^q/x_o^{q+1} & \text{if } 0 \le x \le x_o \\ cx_o^{p-1}/x^p & \text{if } x_o \le x \le x_M \\ 0 & \text{if } x > x_M \end{cases}$$

where q and p are not necessarily integers but can be real numbers and the constant c for $p \neq 1$ is given by (Ferris-Prabhu 1985),

$$c = (q+1)(p-1)/[(q+p) - (q+1)(x_o/x_M)^{p-1}]$$

Data gathered through many experiments showed that $q \approx 1$ and $p \approx 3$ with "typical" values for the latter between 2.85 and 3.1 (Stapper 1984).

With defects of size comparable to that of many VLSI patterns, the probability that a defect will result in a circuit failure is a random variable rather than a constant. We define therefore, the critical area for defects of diameter x, as the area in which the center of a defect (of diameter x) must fall in order to cause a circuit failure. We denote this critical area by $A(x)$ and compute its expected value A_c using,

$$A_c = \int_o^\infty A(x)\ f(x)\ dx$$

Note that we omitted the subscript i to simplify the derived expressions.

Expressions for the critical area $A(x)$ have been derived by Stapper (1984) and Ferris-Prabhu (1985) for a number of long conducting lines on a chip. For these long lines the width w of a conductor and the spacing s between two adjacent conductors are very small compared to the length L of these conductors; a fact that simplifies the derivation of an expression for $A(x)$. In what follows we analyze two basic geometrical patterns that can be found in ordinary VLSI designs and derive expressions for their critical area. Most VLSI layouts contain these basic patterns and analysis of these allows us to estimate the effect of scaling on their critical area.

Consider first a conductor of length L and width w as shown in Figure 1. Assume that an open-circuit defect will cause the conductor to fail if at any point along the conductor, a width of δ (or less) of material is left. To simplify the expressions to be derived for $A(x)$ we set this minimum allowable conductor width δ to be zero. This simplification does not change the functional dependence of $A(x)$ on the physical dimensions of the conductor.

To derive an expression for the critical area $A(x)$ for open-circuit defects (in the conductor shown in Figure 1) note that this area consists of a rectangular part and four circular-shaped parts. The rectangular part was shown (Stapper 1984 and Ferris-Prabhu 1985) to have an area of size $(x-w)L$. The area of each of the four circular

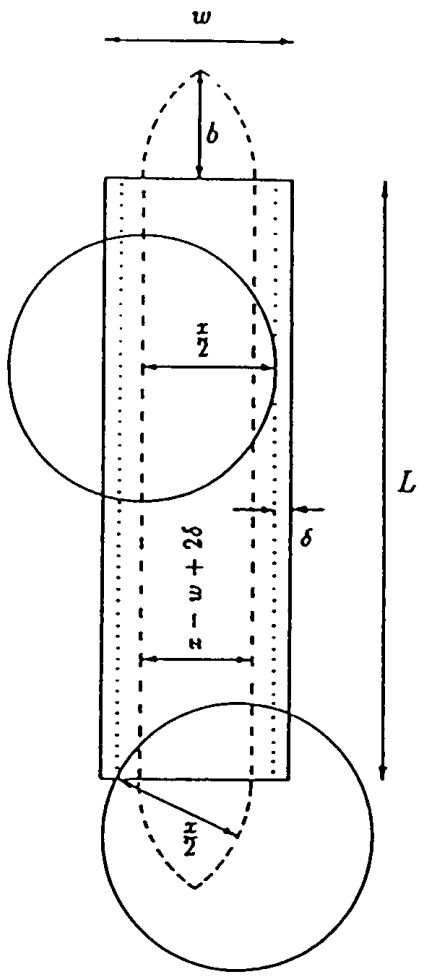

Figure 1: The critical area of a conductor of length L and width w.

parts is approximately equal to that of a triangle having a height of $(x-w)/2$ and a base of $b = \frac{1}{2}\sqrt{x^2 - w^2}$ (see Figure 1). The area of the triangle is,

$$\frac{1}{8}\,(x-w)\sqrt{x^2-w^2}$$

Finally, we obtain,

$$A(x) = \begin{cases} 0 & \text{if } x < w \\ (x-w)L + \frac{1}{2}(x-w)\sqrt{x^2-w^2} & \text{if } x \geq w \end{cases}$$

Notice that the critical area is a quadratic function of the defect size. Also note that for $L \gg w$, the quadratic term in $A(x)$ becomes negligible. Thus, for very long conductors we may use the linear term only. An analogous expression for $A(x)$ for short-circuit

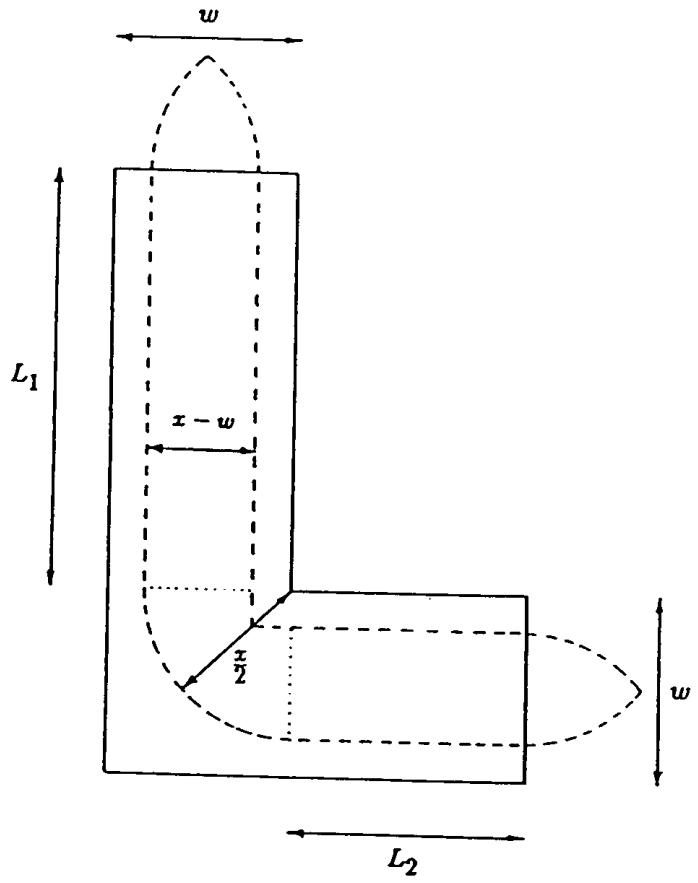

Figure 2: The critical area of an L shaped conductor.

defects in a rectangular area of width s (between two adjacent conductors) can be obtained by replacing w by s in the above equation.

Another very common pattern in VLSI layouts is an L shaped pattern, depicted in Figure 2. As is evident from this figure the shapes and sizes of most parts of the critical area are identical to those of the previous simpler pattern in Figure 1, except that the critical area at the corner of the L has the shape of a quarter of a circle of diameter x. The resulting approximation for the critical area is,

$$A(x) = \begin{cases} 0 & \text{if } x < w \\ (x-w)(L_1+L_2) + \frac{1}{2}(x-w)\sqrt{x^2-w^2} + \frac{1}{4}\pi x^2 - (\frac{x}{2}-w)^2 & \text{if } x \geq w \end{cases}$$

The expression for the critical area in this case is very similar to the one for the conductor in Figure 1 and again, if $(L_1 + L_2) \gg w$, the linear term in $A(x)$ is the dominant one.

Common VLSI layouts consist of several patterns of the shapes shown in Figures 1 and 2, in different sizes and orientations. Consequently, the exact expression for

the critical area of one layout will be different from that of another layout. However, we may still analyze the possible effects of scaling on the critical area of an arbitrary layout by studying the effect of scaling on certain terms which may appear in the expression for the critical area.

Generalizing the results presented by Stapper (1984) we can conclude that the expression for the critical area of a layout will be a linear combination of the expressions for the critical areas of its components (i.e., the basic geometric patterns). Hence, we may expect to find in the critical area expression for any general VLSI layout, a linear term which will usually be the most dominant one. Analysis of this term can indicate the nature of changes in the critical area that will occur when scaling is performed.

Even the analysis of the linear term only is not trivial since the exact form of the corresponding expression for A_c depends on the relative size of the width w of the conductors (or the spacing s between two adjacent conductors if short-circuit defects are considered) and the mode x_o of the defect size distribution.

Let L denote some "equivalent length" of the general pattern (e.g., $L_1 + L_2$ for the pattern in Figure 2). The precise value of L is immaterial; as will be shown next we only have to know that it reduces to aL when ideal scaling is performed. The average value of the critical area due to a linear term of the form $(x - w)L$ is given by

$$A_c = \int_w^\infty (x - w)L\, f(x)\, dx$$

Because of the special form of the defect-size density function $f(x)$ we have theoretically, to analyze two separate cases, namely, $x_o < w$ and $x_o > w$. In practice however, it has been observed (Maly 1985) that x_o is close to the maximal resolution of the lithography process and therefore, only the case $x_o < w$ is of interest. For this case we obtain

$$A_c = \int_w^{x_M} (x - w)L\, \frac{cx_o^{p-1}}{x^p}\, dx$$

and for $p > 2$,

$$A_c = \frac{cL}{(p-1)(p-2)} \frac{x_o^{p-1}}{w^{p-2}} - \frac{cL}{(p-1)(p-2)} \frac{x_o^{p-1}}{x_M^{p-2}} \left[(p-1) - (p-2)\frac{w}{x_M}\right]$$

When scaling is performed, the resulting average critical area A_c' is calculated from the above expression by substituting L and w by aL and aw, respectively, yielding

$$A_c' = \frac{cL}{(p-1)(p-2)} \frac{x_o^{p-1}}{w^{p-2}} \frac{1}{a^{p-3}} - \frac{cLa}{(p-1)(p-2)} \frac{x_o^{p-1}}{x_M^{p-2}} \left[(p-1) - (p-2)\frac{w}{x_M}a\right]$$

We may now compute the ratio A_c'/A_c,

$$\frac{A_c'}{A_c} = \frac{\frac{1}{a^{p-3}} - \left(\frac{w}{x_M}\right)^{p-2} a \left[(p-1) - (p-2)\frac{w}{x_M}a\right]}{1 - \left(\frac{w}{x_M}\right)^{p-2} \left[(p-1) - (p-2)\frac{w}{x_M}\right]}$$

For $x_M \gg w$ and $p > 3$ the ratio A_c'/A_c increases approximately as $1/a^{p-3}$. The exact value of this ratio for three values of p, i.e., $p = 2.8, 3$ and 3.2, is depicted in Figure 3

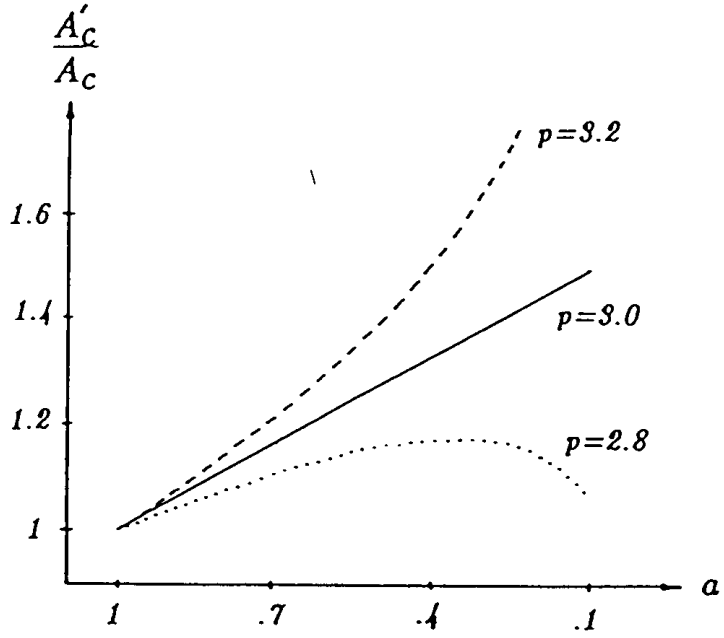

Figure 3: The critical area ratio in the case of $x_o < w$ for different values of p.

for $w/x_M = \frac{1}{6}$. Very similar curves were obtained for many other values of the ratio w/x_M. We may therefore conclude that scaling (with $a < 1$) results in an increase in the expected value of the critical area which in turn reduces the yield.

To finally determine the effect of scaling on the yield due to photolithographic defects, any possible changes in the clustering parameter α must be taken into account. For large area VLSI chips the clustering parameter will in most cases decrease when the area of the chip is being reduced. This will tend to lower the yield of the scaled chip. The expected increase in the average critical area A_c combined with the smaller clustering parameter, will result in a lower yield (due to photolithographic defects) for the scaled chip.

CONCLUSIONS

The exact effect of scaling on the yield of an arbitrary VLSI chip consisting of a variety of different geometrical patterns can not be predicted. However, we may still draw some important conclusions out of the analysis done in the previous sections. If the number of photolithographic defects is larger than the number of pinhole defects, the final effect of scaling on yield will mainly depend on the ratio A_c'/A_c for photolithographic defects. Consequently, as long as the scaled feature size is still larger than the

mode x_o we may expect a reduction in yield. Note that this analysis does not take into account other factors, mostly fabrication related ones, which may influence the final yield of the scaled VLSI design.

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