Should Yield be a Design Objective?

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Abstract

The objectives of good chip design have traditionally included issues like performance, power and reliability. Yield is rarely considered during the design process, except in the design of memory ICs, where specific defect-tolerance techniques are incorporated into the architecture for yield enhancement.

In order to make the case for establishing yield as another design objective we must first prove that a chip's yield can not only be affected, but consistently improved, by decisions made during the design process.

1. Introduction

The traditional objectives during the design of integrated circuits include timing, area, power and reliability. Designers take these objectives into consideration and will redo portions of their design if certain values of these quality measures are not achieved. Most existing CAD systems include tools to evaluate these measures and assist the designer in meeting the product goals.

The situation is different with respect to yield. Yield is still, in most cases, considered an issue which is of concern only to fabrication engineers, and not to chip designers. Most designers are not even aware that some of the design decisions which they make, and some of the techniques/tools which they use, have an impact on the product yield.

The question we raise here is, should yield be made a design objective to be added to traditional quality measures? To answer positively, we must first establish the impact of design decisions on the yield, and then prove that the design at certain stages of the process can be modified in order to achieve a higher yield for the final product.

Yield can be made into a design objective in several different stages of the design process: architecture, floorplanning, routing and compaction. The impact of architectural choices on yield is well-known, and is used regularly in the design of large capacity memory ICs with built-in redundancy. Since this is currently a well established practice, we will not discuss it in this paper. In contrast, techniques for yield enhancement during floorplanning, routing and compaction are hardly ever used. We will present the various techniques which have been developed for yield enhancement during the routing and compaction stages and discuss their benefits. The effect of floorplanning on yield has only recently been recognized. We will demonstrate this effect and show how the yield objective can be integrated into the floorplanning process together with the traditional objectives.

2. Preliminaries

Manufacturing defects can be roughly classified into two types: systematic defects and random spot defects. Systematic defects, which include parametric defects and mask misallignements, must be dealt with during the fabrication process. Random spot defects, on the other hand, cannot be eliminated during fabrication and may therefore be a target for reduction techniques during the design process. The expected number of these random spot defects increases with the chip area and as a result, they are of great significance when yield is of concern.

Some spot defects cause missing material, which may result in open circuits, while others cause extra patterns, which may result in short circuits. These defects can also be classified into intra-layer defects and inter-layer defects. Intra-layer defects occur as a result of particles deposited during the lithographic processes. Examples include missing or extra metal, diffusion or polysilicon, and defects in the silicon substrate due to contamination in the deposition processes. Inter-layer defects include missing material in the vias between two metal layers or between a metal

layer and polysilicon, and extra material between the substrate and metal (or diffusion or polysilicon) or between two separate metal layers. These inter-layer defects occur as a result of local contamination, e.g. dust particles.

Spot defects do not necessarily result in structural faults such as line breaks or short circuits. In order to cause a circuit fault, a defect has to be large enough to connect two disjoint conductors or disconnect a continuous pattern. Thus, the probability of a defect resulting in a fault depends on the location of the defect, its size and the density of the layout. The fraction of manufacturing defects which result in functional (circuit) faults is called the *probability of failure* (POF) and the product of the total chip area and the POF is called the *critical area* [16]. The critical area for defects of a certain type, say type i, is denoted by $A_i^{(c)}$ and is equal to the average size of the area in which the center of a defect of type i must fall in order to cause a circuit failure, for a given distribution of the defect size.

Since the POF and the critical area are related, either one can be calculated first. Several methods for calculating these parameters are used in practice. Some methods are geometry-based and calculate the critical area first, while others are Monte-Carlo type (e.g., [28]) and calculate the POF first. A detailed description of the methods for calculating the critical area is available in [12].

Once the critical areas are calculated for a given chip layout and for all the various defect types, they are then used to compute the average number of faults on the chip, denoted by λ, using

$$\lambda = \sum_i A_i^{(c)} d_i$$

where d_i is the average number of defects of type i per unit area. λ is the most important parameter of all mathematical models which are presently used to calculate the projected yield of a chip. Such models include the basic Poisson model, which assumes that the defects are uniformly distributed on the wafer and the Negative Binomial model which allows for defect clustering, a phenomenon which has been observed in most manufacturing lines [8]. The expressions for the chip yield are

$$Y = Y_0\, e^{-\lambda} \quad ; \qquad Y = Y_0\, (1 + \lambda/\alpha)^{-\alpha}$$

for the Poisson and Negative Binomial models, respectively. Y_0 is the gross yield factor; this is the probability that the chip is not hit by gross defects caused by systematic processing problems. α is the *clustering parameter*, which indicates the severity of the clustering of defects on the wafer. Values for the three parameters, Y_0, λ and α, are commonly obtained by semiconductor manufacturers using simple estimation techniques.

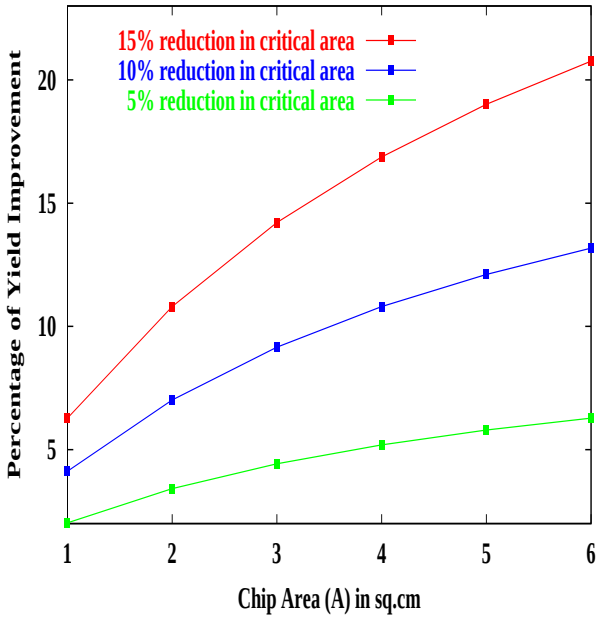

Figure 1: The effect of critical area reduction on yield improvement

$$\text{Percentage of Yield Improvement} = \frac{\text{New Yield - Old Yield}}{\text{Old Yield}} \times 100$$

3. The Impact of placement, routing and compaction on yield

The final steps in the design procedure, namely placement, routing and compaction, all affect the yield similarly. All three determine the proximity of adjacent devices and interconnects, and thus set the value of the critical area, which, in turn, affects the value of λ. The effect of reduction in the critical area on the yield of a chip depends on its size, as shown in Figure 1. The yields in this figure were calculated using the Negative Binomial model with $Y_0 = 0.95$, $\alpha = 2.0$ and

$d = 0.5/cm^2$. For example, the yield of a $3.0cm^2$ chip can be improved by 14.2% if a reduction of 15% in the critical area is achieved.

Most current CAD tools for these steps attempt to optimize the designed circuit with respect to performance and total silicon area while making sure that the basic design rules are not violated. Devices are put as close to each other as possible so that the area will be minimal, and interconnects are made as short as possible in order to minimize the signal delays. These objectives tend, in most cases, to lead to layouts with uneven density of devices and wires. Some portions of the layout have a very high density, resulting in a very high POF value, which makes them very sensitive to defects, while other portions of the layout are more sparse. This is due to the fact that patterns (like polygons) of various shapes are packed into a rectangular area.

From the point of view of yield, the best layout is one with almost uniform spacing between adjacent patterns and with as short wires as possible. Uniform spacing reduces the sensitivity to short-circuit type defects, while short wires reduce the sensitivity to open-circuit type defects. In most cases, these are two conflicting objectives and a tradeoff between the two sensitivities is inevitable. This tradeoff is greatly simplified in practice, since short-circuit type defects have a considerably higher density than open-circuit type defects [7]. Much more significant improvements in yield can be made by focusing on uniform spacing than on having short wires.

One might assume that reaching a uniform layout is best achieved in the compaction step. However, by this stage of the physical design the relative positions of all the layout patterns and the assignment of wire segments to different layers have already been completed; as a result, the capabilities of the compaction step are limited. We must, therefore, pay attention to the yield during the placement and routing steps as well.

We now briefly outline the methods which have been developed for yield enhancement during the last steps of the physical design procedure. The main goal of the compaction step is area minimization with the purpose of increasing the number of chips in the wafer. Most compactors also have some secondary objectives, like minimizing the total wire length and minimizing the number of jogs, with the goal of performance improvement. Unfortunately, some compactors place all circuit elements as closely as the design rules permit, unnecessarily packing many elements very close together, which results in a large critical area for short-circuit defects. Moreover, some compactors stretch various wire segments in order to maintain the original topology, resulting in longer nets with a large critical area for open-circuit defects.

Two approaches to yield-enhanced compaction have been proposed. In one, local modifications in the layout are made as a post-compaction step [1, 5]. These modifications reduce the sensitivity to defects by redistributing the spacing between elements and by increasing the width of several wires. Reductions in critical area of about 8% were reported [5]. In the second approach (e.g., [2]) the compaction algorithm is modified so that both the critical area and the more traditional objectives of compaction are optimized.

Since compaction is the last stage of the physical layout synthesis, the effectiveness of the yield enhancement at this stage is highly dependent on the quality of the layout generated by the previous stages. Additional yield improvements can therefore be achieved through strategies for routing, layer assignment and the like.

Most routers try to minimize the number of vias in the layout. The minimum width and spacing requirements for vias are larger than those for wires and thus, more compact designs are usually accomplished with fewer vias. Sometimes, to avoid a via, routers may introduce very long wire segments, which clearly result in a higher critical area. However, in certain situations it may be worthwhile to leave the vias intact (or even add new ones) to avoid unnecessarily long interconnects. For example, for the defect densities reported in [7], adding a via which can eliminate more than 15 microns of polysilicon reduces the critical area.

As for the compaction step, two approaches for yield-enhanced routing have been followed, one making post-routing modifications and the other modifying the routing algorithm to add yield to the design objectives. In [4, 6], algorithms for modifying two-layer channel routing to reduce the wire length were presented, moving nets from one track to another, interchanging nets and entire tracks, and reassigning nets to different layers. Reduction of about 14% in the to-

tal wire length of the vertical layer and of about 30% in the number of vias were reported.

New routing algorithms (for channels [20], sea of gates [13] and gridless channels [27]) have been developed with yield as an objective. A reduction of 6.4% in the layout sensitivity to defects has been reported [13].

4. The Impact of floorplanning on yield

The floorplanning step seems to be the least likely to have an impact on the yield and, consequently, VLSI designers rarely consider yield issues when selecting a floorplan for a newly designed chip. This is still justified for chips which either have almost no clustered defects (allowing the use of the Poisson yield model) or are small relative to the size of the defect clusters. However, large area integrated circuits (e.g., $2cm^2$ and up) may have different yields depending on their floorplan [15]. The dependence between the floorplan and the projected yield is especially significant for chips which either have different types of modules with different fault densities, or have some incorporated redundancy.

Exact analysis of several floorplans using the medium-size clustering yield model [14] has revealed that in order to achieve the best yield, the most sensitive (to defects) modules should be placed near the center of the chip while the least sensitive modules should be placed at the corners. This makes sense intuitively, because a fault cluster that occurs at a corner is more likely to hit two or even four adjacent chips on the wafer. Modules placed in the corners should thus be as insensitive (to defects) as possible. A difference in yield of about 14% between the most favorable floorplan and the least favorable one was reported in [16] for a 64-bit microprocessor of size $14.7 \times 15.3\ mm^2$. Gains in yield due to floorplan modifications were also reported for some memory ICs with built-in redundancy [18].

In contrast to the layout modifications for yield enhancement which are made during the last steps of the physical design, changes made in the floorplan in order to increase yield are more likely to adversely affect the conventional objectives, which are minimizing the total chip area and reducing the routing cost, i.e., the total length of the interconnecting wires. Since there is no direct relationship between the defect density of a module and its connectivity to other modules, it is very likely that the floorplans with the highest possible yield will not have the smallest wiring cost. Clearly, minimizing the total wiring length, which impacts the performance of the chip, will always be more important than increasing the expected yield.

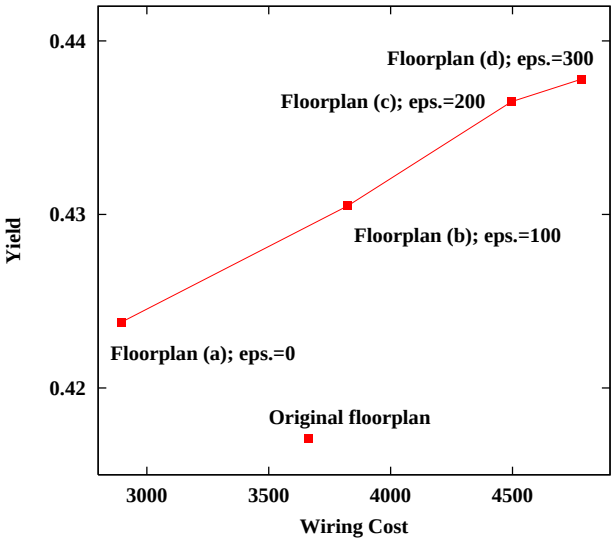

Figure 2: Four yield and wiring cost Pareto-optimal floorplans.

Consequently, a highly suitable way to solve this multi-objective optimization problem is to generate a set of "Pareto-optimal" solutions, so that none of the solutions in the set dominates any of the others, and all are considered equally optimal. The designer can then select one out of these Pareto-optimal floorplans according to the relative significance of the two objectives. Since searching for a floorplan which optimizes either one of these two objectives is, in the general case, NP-complete, a constructive algorithm [29] for generating floorplans with the wiring cost as the primary objective and the yield as the secondary objective has been developed [19]. An example of the set of Pareto-optimal floorplans generated by this constructive algorithm for a microprocessor is shown in Figure 2. The four Pareto-optimal floorplans are depicted in Figure 3. In these floorplans modules 7, 3 and 9 are the ROM, Instruction Cache and Data Cache, respectively, and have the highest device density resulting in the highest sensitivity to defects among all twelve modules. Modules 1, 2, 5 and 6 (random logic units like Instruction Decode) have the lowest device den-

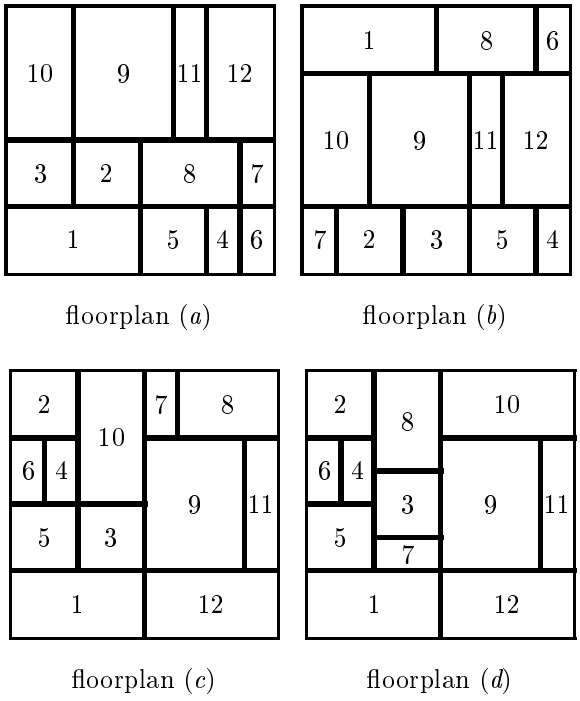

Figure 3: The four Pareto-optimal floorplans.

sity. Notice that in floorplan (a), which has the highest projected yield (see Figure 2), all three most sensitive modules are in the center of the chip. These three modules are at the chip boundaries in floorplan (a).

This and other examples presented in [19] show that even if the wiring length is considered of utmost importance, the yield can still be maximized within the set of floorplans with the minimal wiring length or at least a length very close to it.

5. Conclusions

With the density and size of chips constantly increasing, the importance of high yield is increasing as well. We should no longer limit the efforts to improve yield to the manufacturing stage. Instead, such efforts should be incorporated into the VLSI design steps as well. Techniques for yield enhancement during various steps of the design process have already been developed. We should further improve these techniques and incorporate them into the CAD tools which we use.

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